

HD74LV573A

Octal D-type Transparent Latches with 3-state Outputs

HITACHI

ADE-205-279A (Z)

2nd Edition

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Description

The HD74LV573A has eight D-type latches with three-state outputs in a 20-pin package. When the latch enable input is high, the Q outputs will follow the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- $V_{CC} = 2.0\text{ V}$ to 5.5 V operation
- All inputs $V_{IH}(\text{Max.}) = 5.5\text{ V}$ ($@V_{CC} = 0\text{ V}$ to 5.5 V)
- All outputs $V_O(\text{Max.}) = 5.5\text{ V}$ ($@V_{CC} = 0\text{ V}$)
- Typical V_{OL} ground bounce $< 0.8\text{ V}$ ($@V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.3\text{ V}$ ($@V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Output current $\pm 8\text{ mA}$ ($@V_{CC} = 3.0\text{ V}$ to 3.6 V), $\pm 16\text{ mA}$ ($@V_{CC} = 4.5\text{ V}$ to 5.5 V)

Function Table

Inputs

\overline{OE}	LE	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Note: H: High level

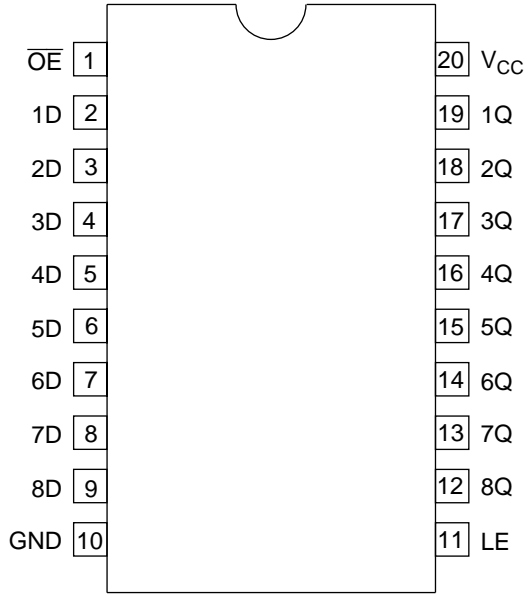
L: Low level

X: Immaterial

Z: High impedance

Q_0 : Output level before the indicated steady state input conditions were established

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range* ¹	V_I	-0.5 to 7.0	V	
Output voltage range* ^{1,2}	V_O	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L V_{CC} : Z or V_{CC} : OFF
Input clamp current	I_{IK}	-20	mA	$V_I < 0$
Output clamp current	I_{OK}	± 50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	± 35	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	± 70	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* ³	P_T	835	mW	SOP
		757		TSSOP
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

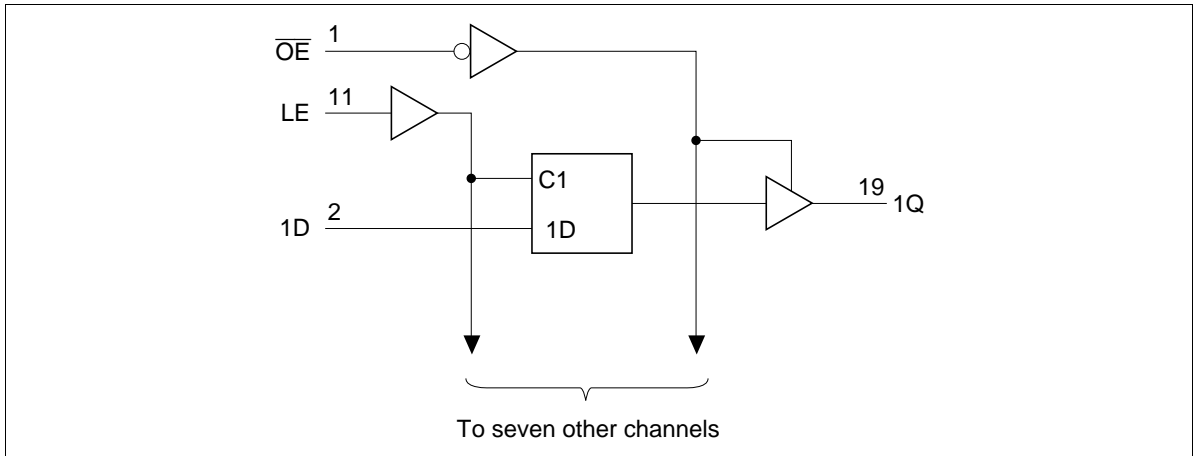
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C .

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
		0	5.5		Output: Z
Output current	I_{OH}	—	-50	μA	$V_{CC} = 2.0 V$
		—	-2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	-8		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	-16	$V_{CC} = 4.5 \text{ to } 5.5 V$	
	I_{OL}	—	50	μA	$V_{CC} = 2.0 V$
		—	2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	8		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	16	$V_{CC} = 4.5 \text{ to } 5.5 V$	
Input transition rise or fall rate	$\Delta t/\Delta v$	0	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 V$
		0	100		$V_{CC} = 3.0 \text{ to } 3.6 V$
		0	20		$V_{CC} = 4.5 \text{ to } 5.5 V$
Operating free-air temperature	T_a	-40	85	$^{\circ}C$	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



DC Electrical Characteristics

- $T_a = -40$ to 85°C

Item	Symbol	V_{CC} (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	$V_{CC} \times 0.7$	—	—		
		3.0 to 3.6	$V_{CC} \times 0.7$	—	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—	—		
	V_{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	$V_{CC} \times 0.3$		
		3.0 to 3.6	—	—	$V_{CC} \times 0.3$		
		4.5 to 5.5	—	—	$V_{CC} \times 0.3$		
Output voltage	V_{OH}	Min to Max	$V_{CC} - 0.1$	—	—	V	$I_{OH} = -50 \mu\text{A}$
		2.3	2.0	—	—		$I_{OH} = -2 \text{ mA}$
		3.0	2.48	—	—		$I_{OH} = -8 \text{ mA}$
		4.5	3.8	—	—		$I_{OH} = -16 \text{ mA}$
	V_{OL}	Min to Max	—	—	0.1		$I_{OL} = 50 \mu\text{A}$
		2.3	—	—	0.4		$I_{OL} = 2 \text{ mA}$
		3.0	—	—	0.44		$I_{OL} = 8 \text{ mA}$
		4.5	—	—	0.55		$I_{OL} = 16 \text{ mA}$
Input current	I_{IN}	0 to 5.5	—	—	± 1	μA	$V_I = 5.5 \text{ V}$ or GND
Off-state output current	I_{OZ}	5.5	—	—	± 5	μA	$V_O = V_{CC}$ or GND
Quiescent supply current	I_{CC}	5.5	—	—	20	μA	$V_I = V_{CC}$ or GND, $I_o = 0$
Output leakage current	I_{OFF}	0	—	—	5	μA	V_I or $V_O = 0 \text{ V}$ to 5.5 V
Input capacitance	C_{IN}	3.3	—	1.8	—	pF	$V_I = V_{CC}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

- $V_{CC} = 2.5 \pm 0.2 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propa- gation delay time	t_{PLH}	—	8.9	15.8	1.0	18.0	ns	$C_L = 15 \text{ pF}$	D	Q
	t_{PHL}	—	9.6	16.2	1.0	19.0			LE	
		—	10.9	18.7	1.0	21.0		$C_L = 50 \text{ pF}$	D	
		—	11.6	19.1	1.0	23.0			LE	
Enable time	t_{ZH}	—	9.3	16.2	1.0	19.0	ns	$C_L = 15 \text{ pF}$	\overline{OE}	Q
	t_{ZL}	—	11.4	19.0	1.0	22.0		$C_L = 50 \text{ pF}$		
Disable time	t_{HZ}	—	6.7	12.6	1.0	15.0	ns	$C_L = 15 \text{ pF}$	\overline{OE}	Q
	t_{LZ}	—	8.6	17.3	1.0	19.0		$C_L = 50 \text{ pF}$		
Setup time	t_{su}	5.0	—	—	5.0	—	ns		Data before LE ↓	
Hold time	t_h	2.0	—	—	2.0	—	ns		Data after LE ↓	
Pulse width	t_w	6.5	—	—	6.5	—	ns		LE "H"	

Switching Characteristics (cont)

- $V_{CC} = 3.3 \pm 0.3 \text{ V}$

Ta = 25°C **Ta = -40 to 85°C**

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM	TO
		Min	Typ	Max	Min	Max			(Input)	(Output)
Propa- gation delay time	t_{PLH}	—	6.2	11.0	1.0	13.0	ns	$C_L = 15 \text{ pF}$	D	Q
	t_{PHL}	—	6.8	11.9	1.0	14.0			LE	
		—	7.7	14.5	1.0	16.5		$C_L = 50 \text{ pF}$	D	
		—	8.2	15.4	1.0	17.5			LE	
Enable time	t_{ZH}	—	6.6	11.5	1.0	13.5	ns	$C_L = 15 \text{ pF}$	\overline{OE}	Q
	t_{ZL}	—	8.0	15.0	1.0	17.0		$C_L = 50 \text{ pF}$		
Disable time	t_{HZ}	—	4.9	11.0	1.0	13.0	ns	$C_L = 15 \text{ pF}$	\overline{OE}	Q
	t_{LZ}	—	6.2	14.5	1.0	16.5		$C_L = 50 \text{ pF}$		
Setup time	t_{su}	3.5	—	—	3.5	—	ns		Data before LE ↓	
Hold time	t_h	1.5	—	—	1.5	—	ns		Data after LE ↓	
Pulse width	t_w	5.0	—	—	5.0	—	ns		LE "H"	

Switching Characteristics (cont)

- $V_{CC} = 5.0 \pm 0.5 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	—	4.3	6.8	1.0	8.0	ns	$C_L = 15 \text{ pF}$	D	Q
	t_{PHL}	—	4.7	7.7	1.0	9.0			LE	
		—	5.3	8.8	1.0	10.0		$C_L = 50 \text{ pF}$	D	
		—	5.7	9.7	1.0	11.0			LE	
Enable time	t_{ZH}	—	4.7	7.7	1.0	9.0	ns	$C_L = 15 \text{ pF}$	\overline{OE}	Q
	t_{ZL}	—	5.7	9.7	1.0	11.0		$C_L = 50 \text{ pF}$		
Disable time	t_{HZ}	—	3.5	7.7	1.0	9.0	ns	$C_L = 15 \text{ pF}$	\overline{OE}	Q
	t_{LZ}	—	4.2	9.7	1.0	11.0		$C_L = 50 \text{ pF}$		
Setup time	t_{su}	3.5	—	—	3.5	—	ns		Data before LE ↓	
Hold time	t_h	1.5	—	—	1.5	—	ns		Data after LE ↓	
Pulse width	t_w	5.0	—	—	5.0	—	ns		LE "H"	

Output-skew Characteristics

Item	Symbol	$V_{CC} \text{ (V)}$	Ta = 25°C			Ta = -40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
Output skew	$t_{sk(O)}$	2.3 to 2.7	—	—	2.0	—	2.0	ns
		3.0 to 3.6	—	—	1.5	—	1.5	
		4.5 to 5.5	—	—	1.0	—	1.0	

Note: Skew between any outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

Operating Characteristics

- $C_L = 50 \text{ pF}$

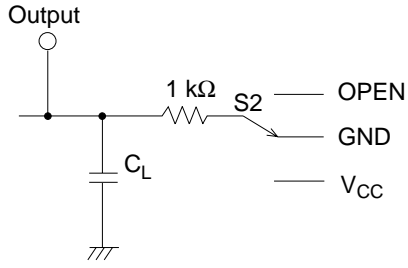
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	3.3	—	16	—	pF	f = 10 MHz
		5.0	—	18	—		

Noise Characteristics

- $C_L = 50 \text{ pF}$

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$	3.3	—	0.6	0.8	V	
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$	3.3	—	-0.5	-0.8		
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$	3.3	—	2.9	—		
High-level dynamic input voltage	$V_{IH(D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL(D)}$	3.3	—	—	0.99		

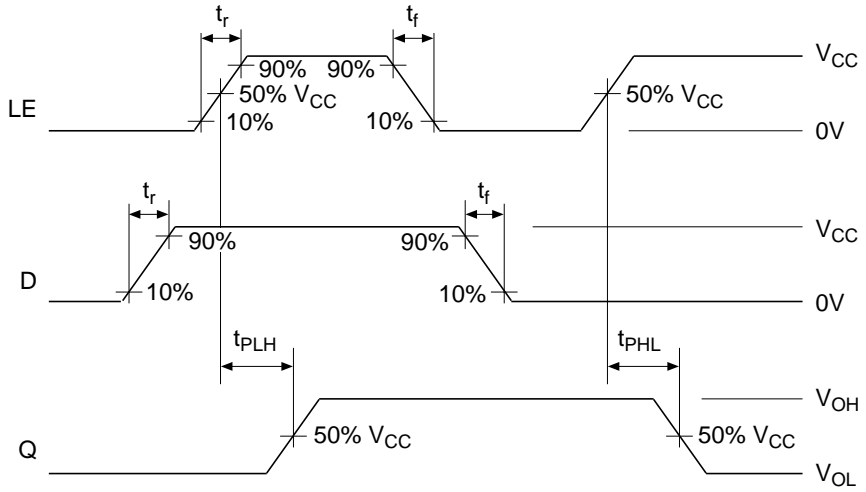
Test Circuit



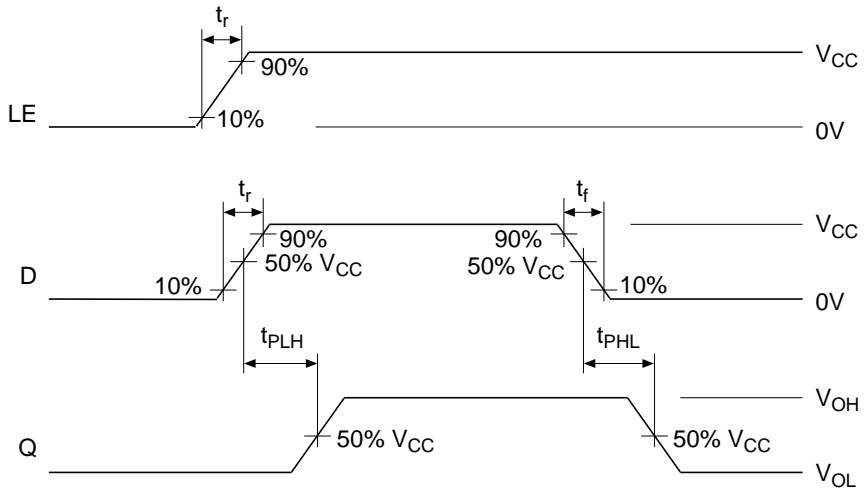
TEST	S2
t_{PLH}/t_{PHL}	OPEN
t_{ZH}/t_{HZ}	GND
t_{ZL}/t_{LZ}	VCC

Note: C_L includes the probe and jig capacitance.

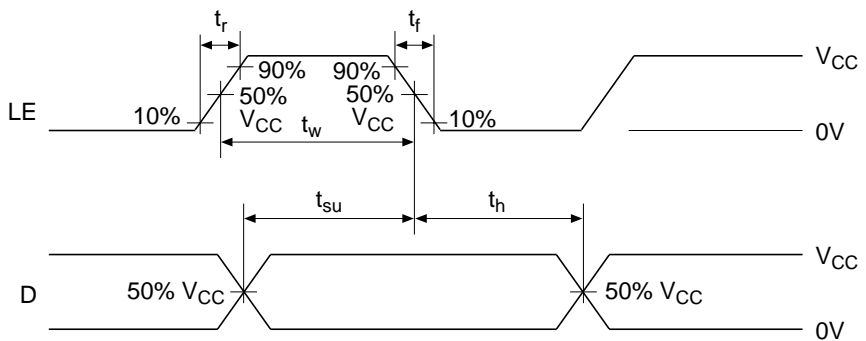
• Waveform – 1



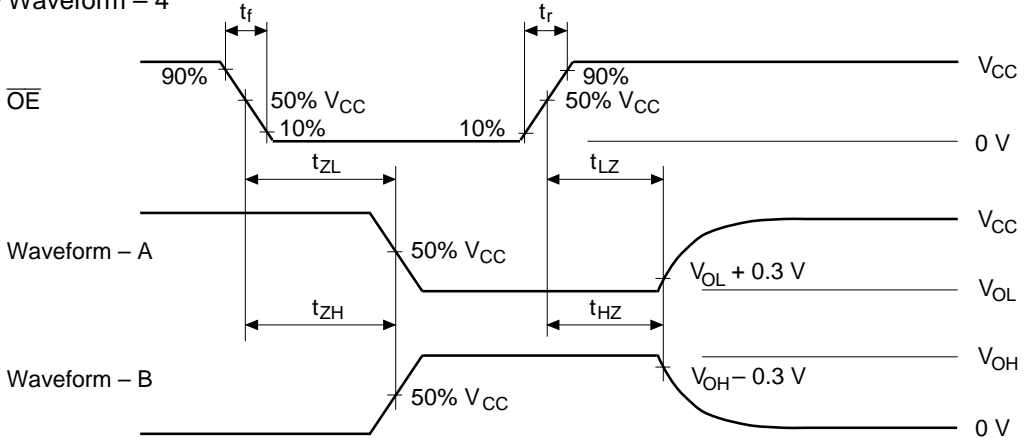
• Waveform – 2



• Waveform – 3



• Waveform – 4



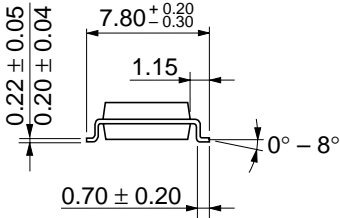
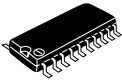
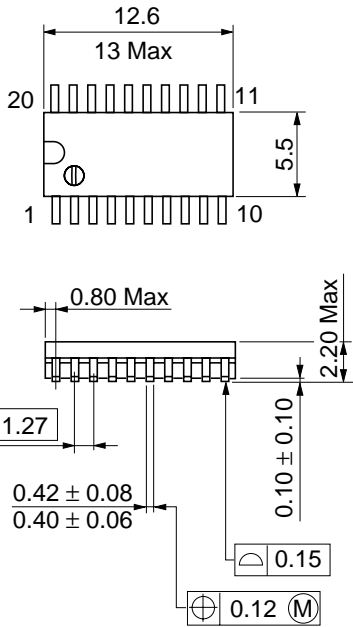
Notes: 1. Input waveform: $PRR \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$

2. Waveform-A is for an output with internal conditions such that the output is low except when disabled by the output control.

3. Waveform-B is for an output with internal conditions such that the output is high except when disabled by the output control.

4. The output is measured one at a time with one transition per measurement.

Package Dimensions

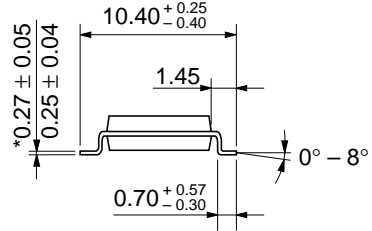
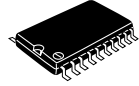
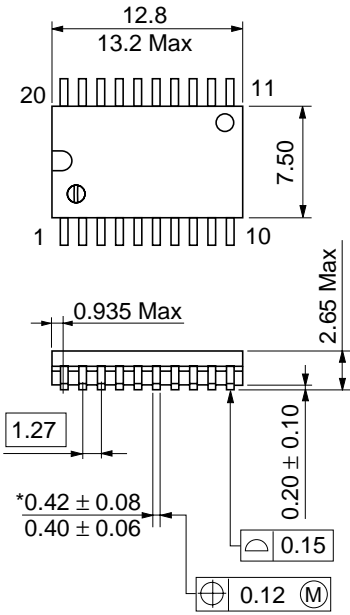


Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g

HD74LV573A

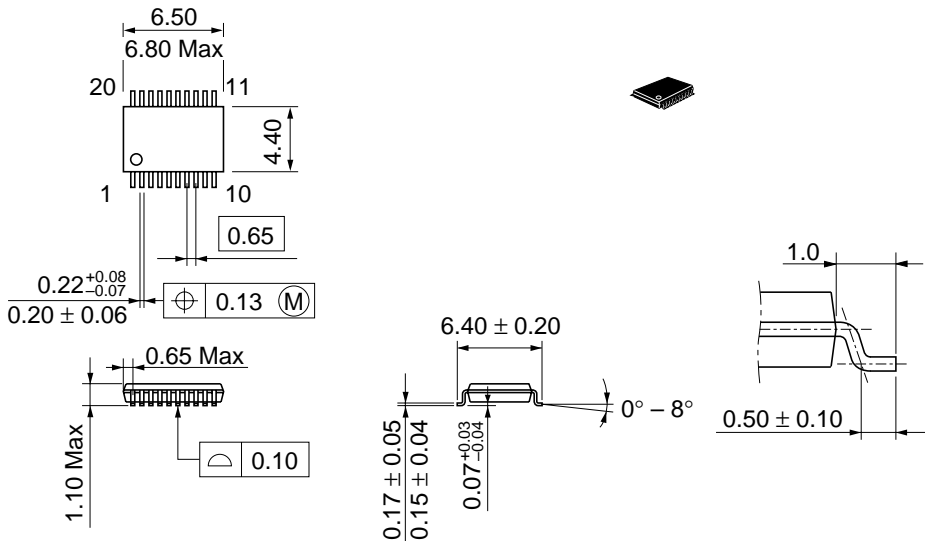
Unit: mm



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

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Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g

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