

# M62354P,FP,GP

## 8-BIT 6CH D-A CONVERTER WITH BUFFER AMPLIFIERS

### DESCRIPTION

The M62354 is an integrated circuit semiconductor of CMOS structure with 6 channels of built-in D-A converters with output buffer operational amplifiers.

The 3-wire serial interface method is used for the transfer format wiring.

It is able to cascading serial use with Do terminal.

The output buffer operational amplifier operates in the whole voltage range from power supply to ground for both input/output.

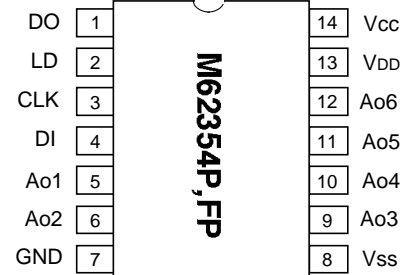
### FEATURES

- 12bit serial data input(3-wire serial data transfer method)
- Highly stable output buffer operational amplifier allow operation in the all voltage range from power supply to ground.

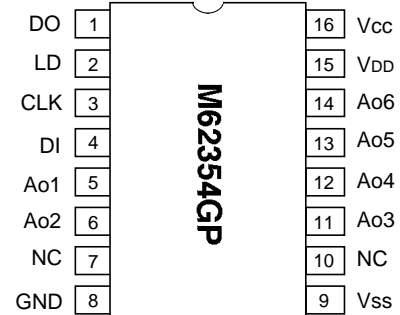
### APPLICATION

Adjustment/control of industrial or home-use electronic equipment,such as VTR camera,VTR set,TV,and CRT display.

### PIN CONFIGURATION (TOP VIEW)



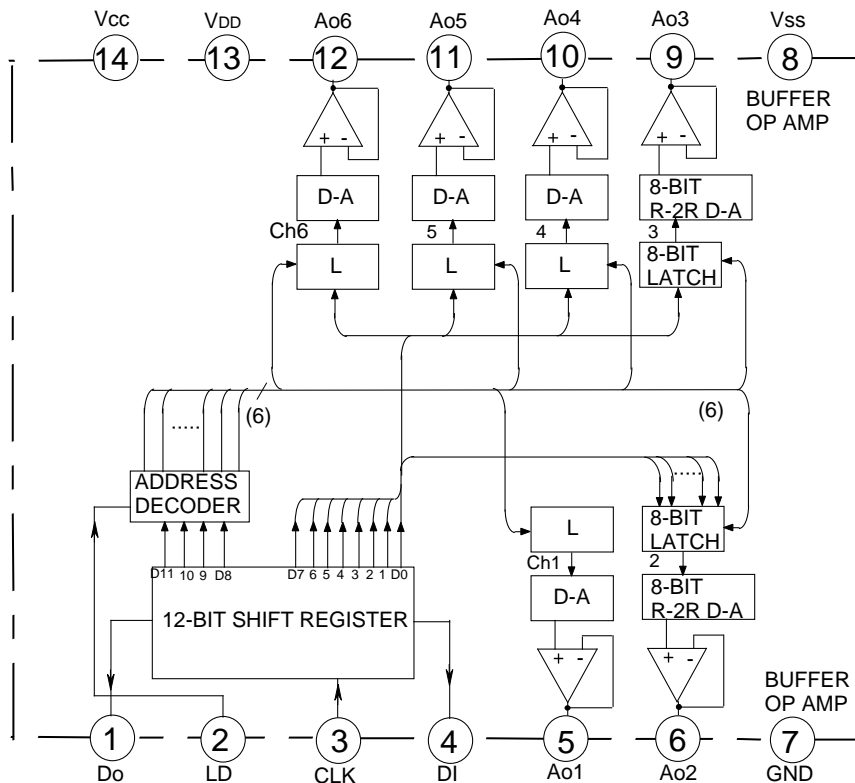
Outline 14P4(P)  
14P2N-A(FP)



Outline 16P2E-A(GP)

NC:NO CONNECTION

### BLOCK DIAGRAM



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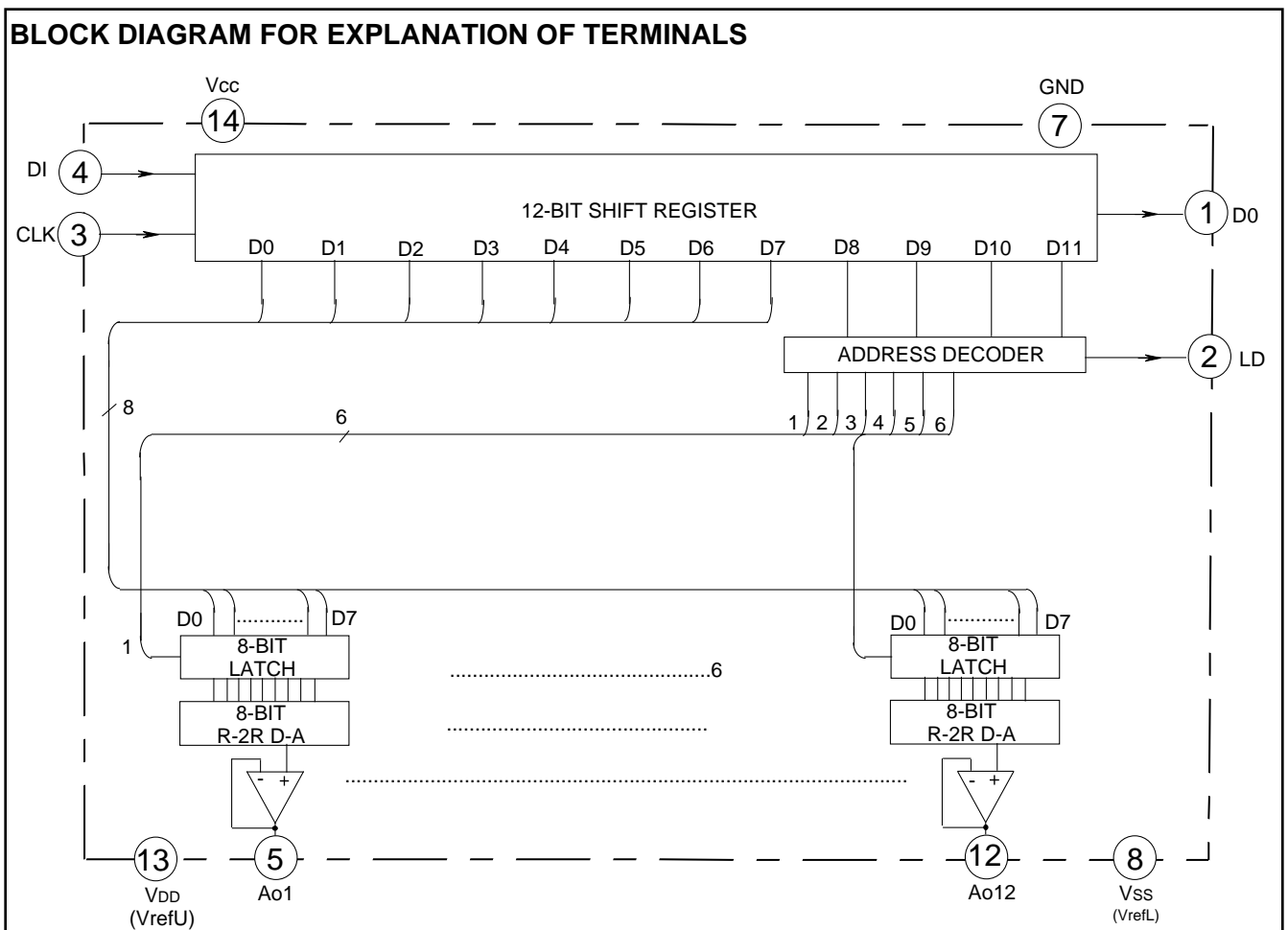
## 8-BIT 6CH D-A CONVERTER WITH BUFFER AMPLIFIERS

### EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
④ (④)*	DI	Serial data input terminal
① (①)	DO	Serial data output terminal
③ (③)	CLK	Serial clock input terminal
② (②)	LD	LD terminal input high level than latch circuit data load
⑤ (⑤)	Ao1	8-bit D-A converter output terminal
⑥ (⑥)	Ao2	
⑨ (⑪)	Ao3	
⑩ (⑫)	Ao4	
⑪ (⑬)	Ao5	
⑫ (⑭)	Ao6	
⑭ (⑯)	Vcc	Power supply terminal
⑦ (⑧)	GND	Digital and analog common GND
⑬ (⑮)	VDD	D-A converter upper reference voltage input terminal
⑧ (⑨)	Vss	D-A converter lower reference voltage input terminal

\*( ):16P2E

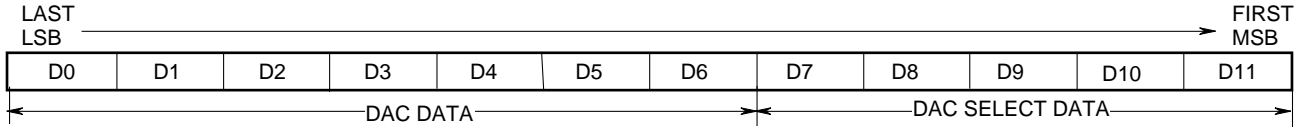
### BLOCK DIAGRAM FOR EXPLANATION OF TERMINALS



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### DIGITAL DATA FORMAT

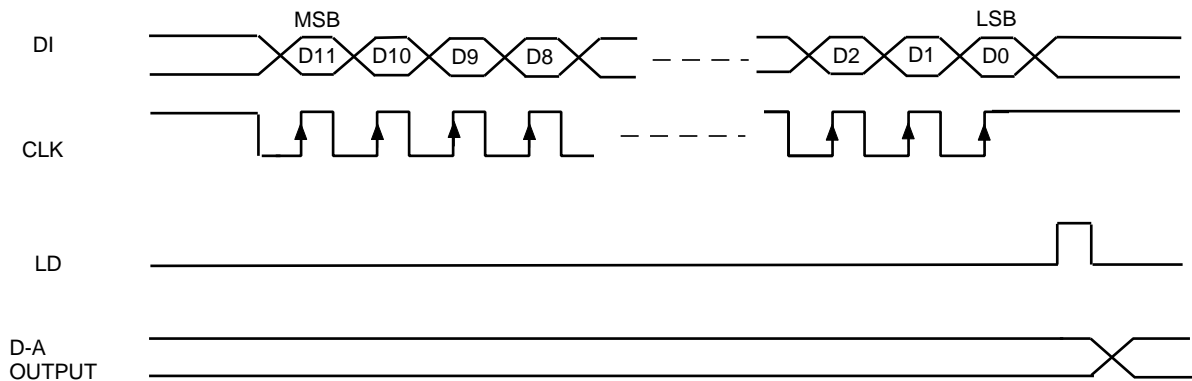


D0	D1	D2	D3	D4	D5	D6	D7	D-A output
0	0	0	0	0	0	0	0	$(V_{refU}-V_{refL})/256 \times 1 + V_{refL}$
1	0	0	0	0	0	0	0	$(V_{refU}-V_{refL})/256 \times 2 + V_{refL}$
0	1	0	0	0	0	0	0	$(V_{refU}-V_{refL})/256 \times 3 + V_{refL}$
1	1	0	0	0	0	0	0	$(V_{refU}-V_{refL})/256 \times 4 + V_{refL}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	$(V_{refU}-V_{refL})/256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	$V_{refU}$

D8	D9	D10	D11	DAC selection
0	0	0	0	Don't care
0	0	0	1	Ao1 selection
0	0	1	0	Ao2
0	0	1	1	Ao3
0	1	0	0	Ao4
0	1	0	1	Ao5
0	1	1	0	Ao6
0	1	1	1	Ao7
1	0	0	0	Ao8
1	0	0	1	Ao9
1	0	1	0	Ao10
1	0	1	1	Ao11
1	1	0	0	Ao12
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

\* $V_{refU}=V_{DD}$   
 $V_{refL}=V_{SS}$

### TIMING CHART (MODEL)



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## 8-BIT 6CH D-A CONVERTER WITH BUFFER AMPLIFIERS

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage		-0.3~7.0	V
V <sub>DD</sub>	D-A converter upper reference voltage		-0.3~7.0	V
V <sub>IN</sub>	Input voltage		-0.3~V <sub>CC</sub> +0.3	V
V <sub>O</sub>	Output voltage		-0.3~V <sub>CC</sub> +0.3	V
P <sub>d</sub>	Power dissipation		440(P)/250(FP)/150(GP)	mW
T <sub>opr</sub>	Operating temperature		-20~+85	°C
T <sub>stg</sub>	Storage temperature		-55~+125	°C

### ELECTRICAL CHARACTERISTICS

**Digital part**(V<sub>CC</sub>,V<sub>refU</sub>=+5V±10%,V<sub>CC</sub> V<sub>refU</sub>,G<sub>ND</sub>,V<sub>refL</sub>=0V,T<sub>a</sub>=-20°C~+85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V <sub>CC</sub>	Supply voltage		4.5	5.0	5.5	V
I <sub>CC</sub>	Circuit current	CLK=1MHz operation I <sub>OA</sub> =0μA		1.6	3.2	mA
I <sub>ILK</sub>	Input leak current	V <sub>IN</sub> =0~V <sub>CC</sub>	-10		10	μA
V <sub>IL</sub>	Input low voltage				0.2V <sub>CC</sub>	V
V <sub>IH</sub>	Input high voltage		0.8V <sub>CC</sub>			V
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> =2.5mA			0.4	V
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> =-400μA		V <sub>CC</sub> -0.4		V

**Analog part**(V<sub>CC</sub>,V<sub>refU</sub>=+5V±10%,V<sub>CC</sub> V<sub>refU</sub>,T<sub>a</sub>=-20°C~+85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I <sub>DD</sub>	Current dissipation	V <sub>refU</sub> =5V,V <sub>refL</sub> =0V Data condition;at maximum current		0.7	1.3	mA
V <sub>DD</sub>	D-A converter upper reference voltage range	The output dose not necessarily be the value within the reference voltage setting range. The output value is determined by the buffer amplifier output voltage range(V <sub>AO</sub> )	3.5		V <sub>CC</sub>	V
V <sub>SS</sub>	D-A converter lower reference voltage range		GND		V <sub>CC</sub> -3.5	V
V <sub>AO</sub>	Buffer amplifier output voltage range	I <sub>OA</sub> =±100μA	0.1		V <sub>CC</sub> -0.1	V
		I <sub>OA</sub> =±500μA	0.2		V <sub>CC</sub> -0.2	
I <sub>AO</sub>	Buffer amplifier output drive range	Upper side saturation voltage=0.3V Lower side saturation voltage=0.2V	-1		1	mA
SDL	Differential nonlinearity error	V <sub>refU</sub> =4.79V	-1.0		1.0	LSB
SL	Nonlinearity error	V <sub>refL</sub> =0.95V	-1.5		1.5	LSB
SZERO	Zero code error	V <sub>CC</sub> =5.5V(15mV/LSB)	-2		2	LSB
SFULL	Full scale error	Without load(I <sub>OA</sub> =±0)	-2		2	LSB
C <sub>O</sub>	Output capacitive load				0.1	μF
R <sub>O</sub>	Buffer amplifier output impedance			5		

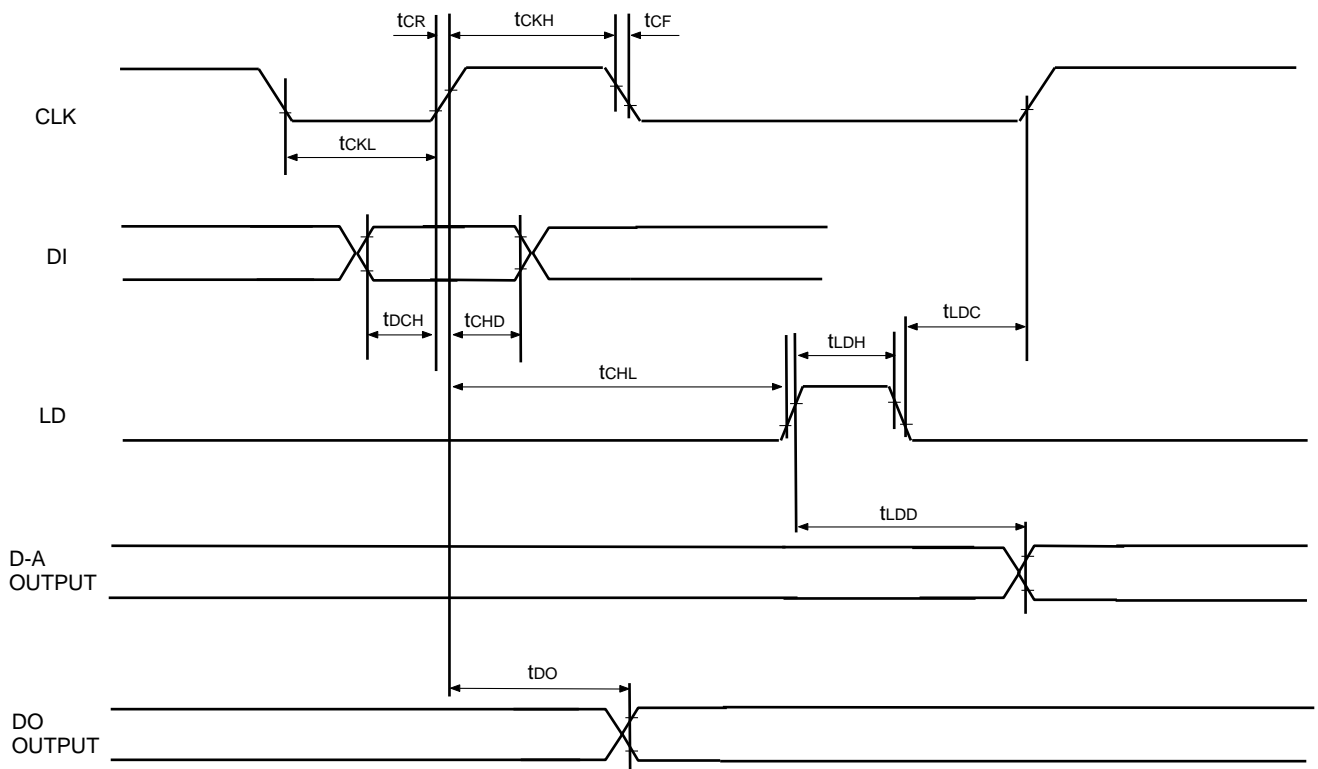
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**AC CHARACTERISTICS**( $V_{cc}, V_{refU}=+5V \pm 10\%, V_{cc} \ V_{refU}, GND, V_{refL}=0V, T_a=-20 \sim +85^\circ C$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
tCLK	Clock "L" pulse width		200			ns
tCKH	Clock "H" pulse width		200			ns
tCR	Clock rise time				200	ns
tCF	Clock fall time				200	ns
tdCH	Data setup time		30			ns
tCHD	Data hold time		60			ns
tCHL	LD setup time		200			ns
tLDC	LD hold time		100			ns
tLDH	LD "H" pulse width		100			ns
tDO	Data output delay time	CL 100pF	70		350	ns
tLDD	D-A output setting time	CL 100pF $V_{AQ}: 0.5 \rightarrow 4.5V$ The time until the output becomes the final value of 1/2 LSB			300	$\mu s$

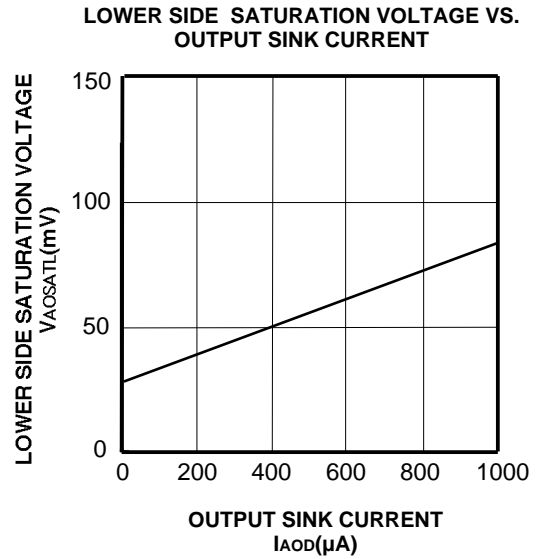
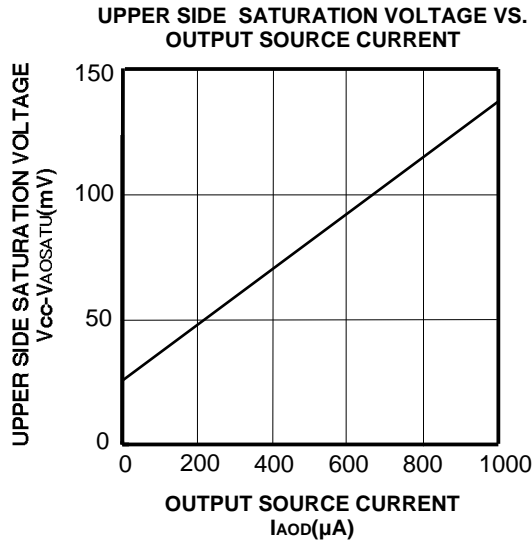
### TIMING CHART



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### TYPICAL CHARACTERISTICS



SATURATION VOLTAGE VS.OUTPUT CURRENT