SIEMENS

ICs for Consumer Electronics

VPS-Decoder

SDA 5642-6/X

Data Sheet 02.97

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Previous Version:		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)

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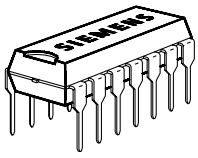
VPS-Decoder **SDA 5642-6/X**

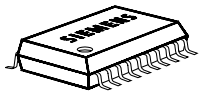
MOS

1 General Description

The SDA 5642-6 VPS decoder chip receives all VPS data.



P-DIP-14-1



P-DSO-20-1

1.1 Features

- **On chip data slicer**
- **Low external component count**
- **I^2C-Bus interface**
  communication with external microcontroller
- **5 V supply voltage**
- **Video input signal level: 0.7 Vpp to 2.0 Vpp**
- **Technology: CMOS**
- **P-DIP-14-1 and P-DSO-20-1 package**

Type	Ordering Code	Package
SDA 5642-6	Q67100-H5182	P-DIP-14-1
SDA 5642-6X	Q67106-H5183	P-DSO-20-1 (SMD)

1.2 Pin Configurations

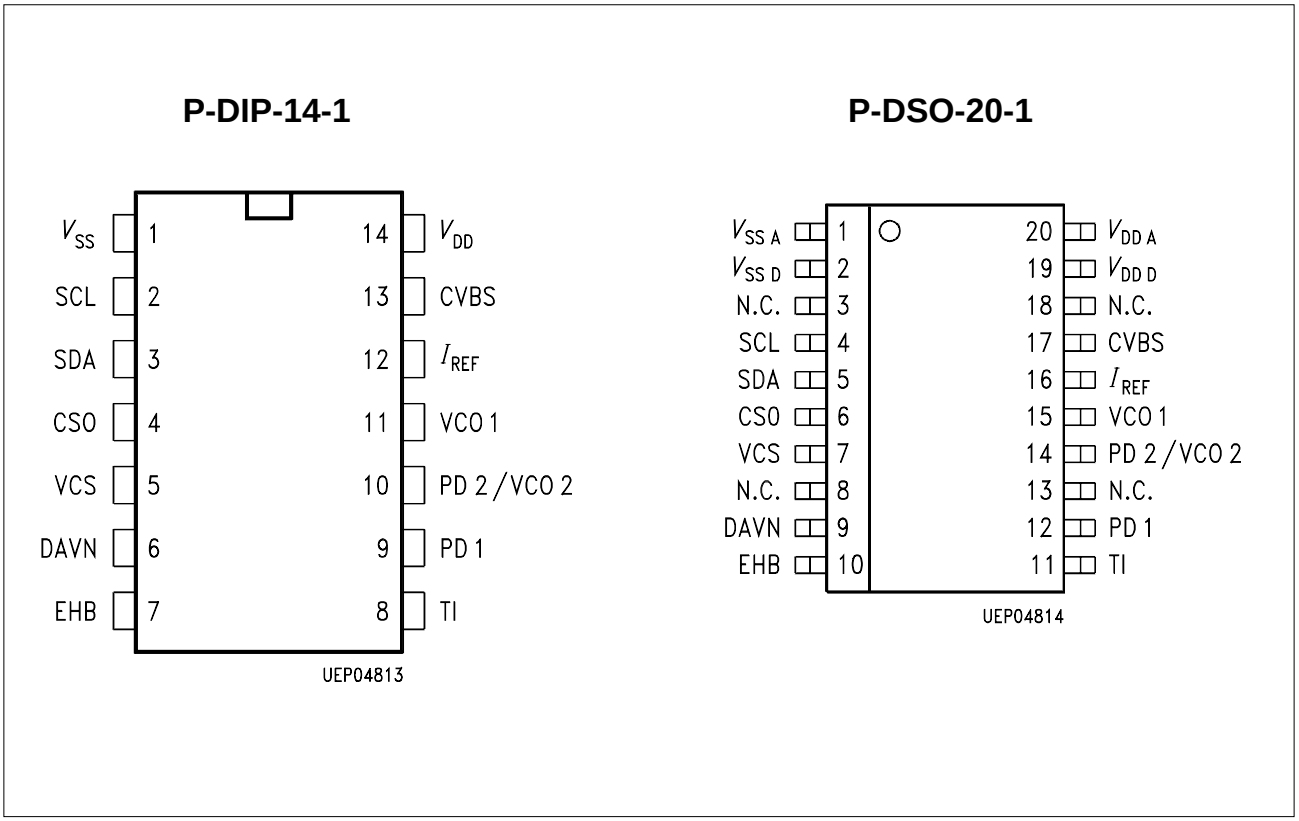


Figure 1

1.3 Pin Description

Pin No.		Symbol	Function
P-DIP-14-1	P-DSO-20-1		
1		V_{SS}	Ground (0 V)
	1	V_{SSA}	Analog ground (0 V)
	2	V_{SSD}	Digital ground (0 V)
	3, 8, 13, 18	N.C.	Not connected
2	4	SCL	Serial clock input of I^2C Bus.
3	5	SDA	Serial data input of I^2C Bus.
4	6	CS0	Chip select input determining the I^2C-Bus addresses: 20_H / 21_H, when pulled low 22_H / 23_H, when pulled high.
5	7	VCS	Video Composite Sync output from sync slicer used for PLL based clock generation.
6	9	DAVN	Data available output active low, when VPS data is received.
7	10	EHB	Output signaling the presence of the first field active high.
8	11	TI	Test input; activates test mode when pulled high. Connect to ground for operating mode.
9	12	PD1	Phase detector/charge pump output of data PLL (DAPLL).
10	14	PD2/ VCO2	Connector of the loop filter for the SYSPLL.
11	15	VCO1	Input to the voltage controlled oscillator #1 of the DAPLL.
12	16	I_{REF}	Reference current input for the on-chip analog circuit.
13	17	CVBS	Composite video signal input.
14		V_{DD}	Positive supply voltage (+ 5 V nom.).
	19	V_{DDD}	Positive supply voltage for the digital circuits (+ 5 V nom.).
	20	V_{DDA}	Positive supply voltage for the analog circuits (+ 5 V nom.).

1.4 Block Diagram

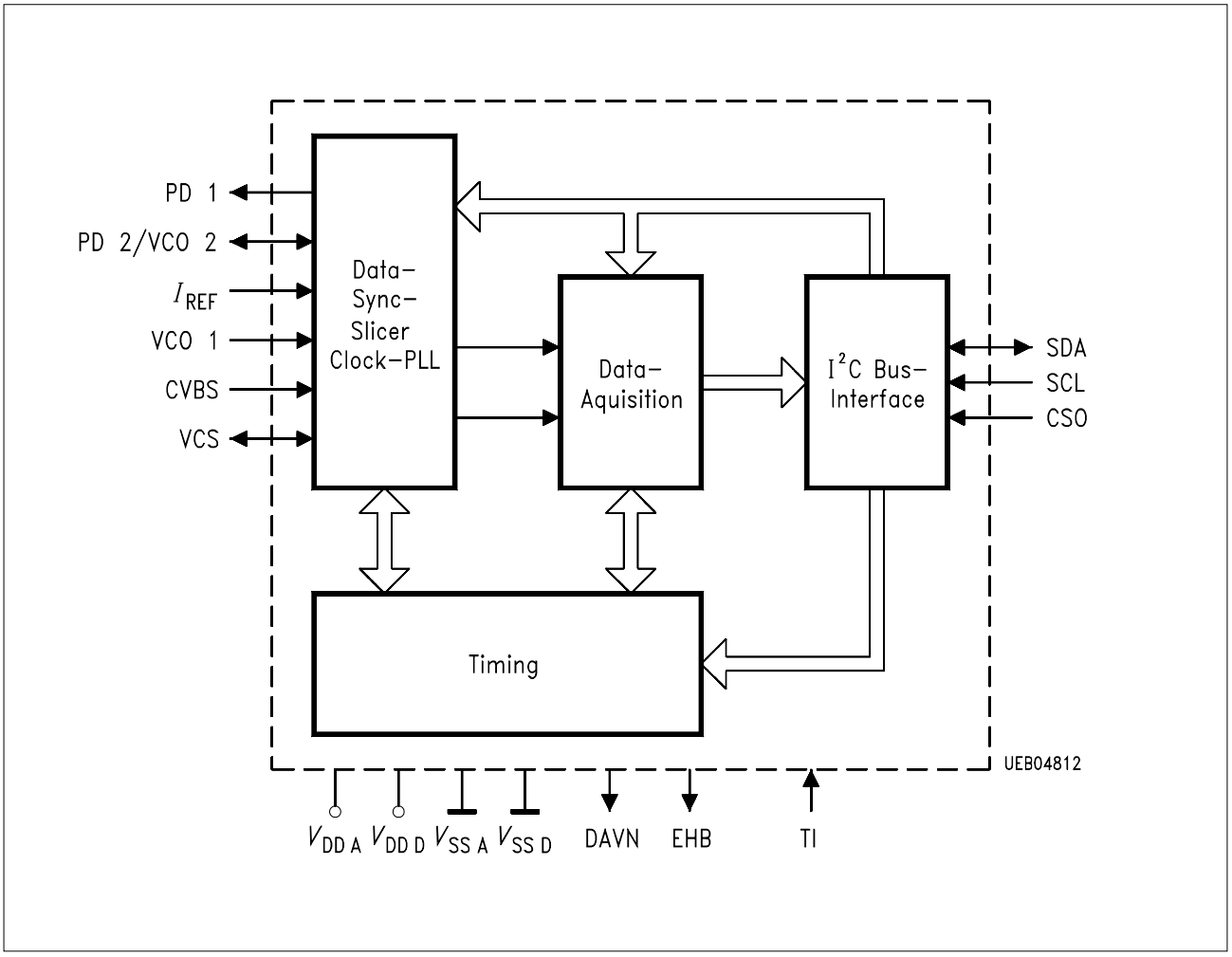


Figure 2

2 System Description

2.1 Functions

Referring to the functional block diagram of the VPS decoder, the composite video signal with negative going sync pulses is coupled to the pin CVBS through a capacitor which is used for clamping the bottom of the sync pulses to an internally fixed level. The signal is passed on to the slicer, an analogue circuitry separating the sync and the data parts of the CVBS signal, thus yielding the digital composite sync signal VCS and a digital data signal for further processing by comparing those signals to internally generated slicing levels.

The output of the sync separator is forwarded, on one hand, to the output pin VCS, and on the other hand, to the clock generator and the timing block. The VCS signal represents a key signal that is used for deriving a system clock signal by means of a PLL and all other timing signal.

The data slicer separates the data signal from the CVBS signal by comparing the video voltage to an internally generated slicing level which is found by averaging the data signal during TV line no. 16.

The clock generator delivers the system clock needed for the basic timing as well as for the regeneraton of the dataclock. It is based on two phase locked loops (PLL's) all parts of which are integrated on chip with the exception of the loop filter components. Each of the PLL's is composed of a voltage controlled relaxation oscillator (VCO), a phase/ frequency detector (PFD), and a charge pump which converts the digital output signals of the PFD to an analogue current. That current is transformed to a control voltage for the VCO by the off-chip loop filter. The generated VCO frequency is 10 MHz.

All signals necessary for the control of sync and data slicing as well as for the data acquisition are generated by the Timing block.

The extracted data bits of TV line no. 16 are checked for biphase errors. With no biphase errors encountered, the acquired bytes are stored in the transfer register to the I^2C Bus. That transfer is signalled by a H/L transition of the DAVN output.

Data are updated when a new data line has been received, provided that the chip is not accessed via the I^2C Bus at the same time.

A micro controller can read the stored bytes via the I^2C-Bus interface at any time. However, one must be aware that the storage of new data from the acquisition interface is inhibited as long as the VPS decoder is being accessed via the I^2C Bus.

2.2 I^2C Bus

2.2.1 General Information

The I^2C-Bus interface implemented on the VPS decoder is a slave transmitter/receiver, i.e., both reading from and writing to the VPS decoder is possible. The clock line SCL is controlled only by the bus master usually being a micro controller, whereas the SDA line is controlled either by the master or by the slave. A data transfer can only be initiated by the bus master when the bus is free, i.e., both SDA and SCL lines are in a high state. As a general rule for the I^2C Bus, the SDA line changes state only when the SCL line is low. The only exception to that rule are the Start Condition and the Stop Condition. Further Details are given below. The following abbreviations are used:

START: Start Condition generated by master
AS: Acknowledge by slave
AM: Acknowledge by master
NAM: No Acknowledge by master
STOP: Stop condition generated by master

2.2.2 Chip Address

There are two pairs of chip addresses, which are selected by the CS0-input pin according to the following table:

CS0 Input	Write Mode	Read Mode
Low	20 (hex)	21 (hex)
High	22 (hex)	23 (hex)

2.2.3 Write Mode

For writing to the VPS decoder, the following format has to be used:

Start	Chipaddress and Write Mode	AS	Byte to set Control Register	AS	Stop

Description of Data Transfer (Write Mode)

Step1: In order to start a data transfer the master generates a Start Condition on the bus by pulling the SDA line low while the SCL line is held high.

Step 2: The bus master puts the chip address on the SDA line during the next eight SCL pulses.

Step 3: The master releases the SDA line during the ninth clock pulse. Thus the slave can generate an acknowledge (AS) by pulling the SDA line to a low level.

Step 4: The controller transmits the data byte to set the Control register

Step 5: The slave acknowledges the reception of the byte.

Step 6: The master concludes the data communication by generating a Stop Condition.

The write mode is used to set the I^2C-Bus control register which determines the operating mode:

Control Register:

Bit Number:	7	6	5	4	3	2	1	0
	T7	T6	T5	T4	T3	T2	T1	T0

Default: All bits are set to 0 on power-up.

The bits T4 through T7 are used for test purposes and must not be changed for normal operation by user software! (0 = normal operation)

You may write 00_H, 01_H, 02_H, 03_H, 04_H, 05_H, 06_H, 07_H, 08_H, 09_H, $0A_H$, $0B_H$, $0C_H$, $0D_H$, $0E_H$, $0F_H$ to the register without efect. This enables the SDA 5642-6 to be used for VPS decoding instead of the SDA 5050 or SDA 5649 without software problems.

2.2.4 Read Mode

For reading from the VPS decoder, the following format has to be used

Start	Chipaddress Read Mode	AS	1st Byte	AM	.....	Last Byte	NAM	Stop

:

The contents of up to 16 registers (bytes) can be read starting with byte 1 bit 7 (refer to the table **Order of Data Output on the I^2C Bus and...**) depending on the selected operating mode.

Description of Data Transfer (Read Mode)

Step1: To start a data transfer the master generates a Start Condition on the bus by pulling the SDA line low while the SCL line is held high. The byte address counter in the decoder is reset and points to the first byte to be output.

Step 2: The bus master puts the chip address on the SDA line during the next eight SCL pulses.

Step 3: The master releases the SDA line during the ninth clock pulse. Thus the slave can generate an acknowledge (AS) by pulling the SDA line to a low level. At this moment, the slave switches to transmitting mode.

Step 4: During the next eight clock pulses the slave puts the addressed data byte onto the SDA line.

Step 5: The reception of the byte is acknowledged by the master device which, in turn, pulls down the SDA line during the next SCL clock pulse. By acknowledging a byte, the master prompts the slave to increment its internal address counter and to provide the output of the next data byte.

Step 6: Steps no. 4 and no. 5 are repeated, until the desired amount of bytes have been read.

Step 7: The last byte is output by the slave since it will not be acknowledged by the master.

Step 8: To conclude the read operation, the master doesn’t acknowledge the last byte to be received. A No Acknowledge by the master (NAM) causes the slave to switch from transmitting to receiving mode. Note that the master can prematurely cease any reading operation by not acknowledging a byte.

Step 9: The master gains control over the SDA line and concludes the data transfer by generating a Stop Condition on the bus, i. e., by producing a low/high transition on the SDA line while the SCL line is in a high state. With the SDA and the SCL lines being both in a high state, the I^2C Bus is free and ready for another data transfer to be started.

2.3 Order of Data Output on the I²C Bus and Bit Allocation

t ↓

I²C Bus			VPS Mode		
Byte 1	bit	7	byte 11	bit	0[1)]
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 2	bit	7	byte 12	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 3	bit	7	byte 13	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 4	bit	7	byte 14	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7

1) Transmission bit number

2.3 Order of Data Output on the I^2C Bus and Bit Allocation (cont'd)

I^2C Bus			VPS Mode		
Byte 5	bit	7	byte 5	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 6	bit	7	byte 15	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 7	bit	7	– set to "1"		
		6	– set to "1"		
		5	– set to "1"		
		4	– set to "1"		
		3	– set to "1"		
		2	– set to "1"		
		1	– set to "1"		
		0	– set to "1"		

[1] Transmission bit number

2.4 Description of DAVN and EHB Outputs

DAVN (Data Valid active low)
EHB (First Field active high)

Signal Output	VPS Mode
DAVN	
H/L-transition (set low)	in line 16 when valid VPS data is received
L/H-transition (set high)	at the start of line 16
always set high	on power-up or during I^2C-Bus accesses when the bus master doesn't acknowledge in order to generate the stop condition
EHB	
L/H-transition	at the beginning of the first field
H/L-transition	at the beginning of the second field

In test mode (i.e. TI = high), both DAVN and EHB are controlled by the CS0 pin and reproduce the state of the CS0 input.

3 Electrical Characteristics

Absolute Maximum Ratings

T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Ambient temperature	T_A	0		70	°C	in operation
Storage temperature	T_{stg}	– 40		125	°C	by storage
Total power dissipation	P_{tot}			300	mW	
Power dissipation per output	P_{DQ}			10	mW	
Input voltage	V_{IM}	– 0.3		6	V	
Supply voltage	V_{DD}	– 0.3		6	V	
Thermal resistance	$R_{th\ SU}$			80	K/W	

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Operating Range

Supply voltage	V_{DD}	4.5	5	5.5	V	
Supply current	I_{DD}		5	15	mA	
Ambient temperature range	T_A	0		70	°C	

Note: In the operating range the functions given in the circuit description are fulfilled.

Electrical Characteristics

T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input Signals SDA, SCL, CS0						
H-input voltage	V_{IH}	$0.7 \times V_{DD}$		V_{DD}	V	
L-input voltage	V_{IL}	0		$0.3 \times V_{DD}$	V	
Input capacitance	C_I			10	pF	
Input current	I_{IM}			10	µA	
Input Signal TI						
H-input voltage	V_{IH}	$0.9 \times V_{DD}$		V_{DD}	V	
L-input voltage	V_{IL}	0		$0.1 \times V_{DD}$	V	
Input capacitance	C_I			10	pF	
Input current	I_{IM}			10	µA	
Input Signals CVBS (pos. Video, neg. Sync)						
Video input signal level	V_{CVBS}	0.7	1.0	2.0	V	2 Vpp with 0.8 V V_{SYNC} and 1.2 V V_{DAT}
Synchron signal amplitude	V_{SYNC}	0.15	0.3	0.8 (1.0)	V	1.0 V only related to VCS signal generation
Data amplitude	V_{DAT}	0.25 $1.5 \times V_{SYNC}$	0.5	1.2	V	
Coupling capacitor	C_C		33		nF	
H-input current	I_{IH}			10	µA	V_I = 5 V
L-input current	I_{IL}	– 1000	– 400	– 100	µA	V_I = 0 V
Source impedance	R_S			250	Ω	
Leakage resistance at coupling capacitor	R_C	0.91	1	1.2	MΩ	

Electrical Characteristics (cont'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Signals DAVN, EHB, VCS						
H-output voltage	V_{QH}	V_{DD} – 0.5			V	I_Q = – 100 µA
L-output voltage	V_{QL}			0.4	V	I_Q = 1.6 mA
Output Signals SDA (Open-Drain-Stage)						
L-output voltage	V_{QL}			0.4	V	I_Q = 3.0 mA
Permissible output voltage				5.5	V	
PLL-Loop Filter Components (see application circuit)						
Resistance at PD2/ VCO2	R_1		6.8		kΩ	
Resistance at VCO1	R_2		1200		kΩ	
Attenuation resistance	R_3		6.8		kΩ	
Resistance at PD2/ VCO2	R_5		1200		kΩ	
Integration capacitor	C_1		2.2		nF	
Integration capacitor	C_3		33		nF	
VCO – Frequence Range Adjustment						
Resistance at IREF (for bias current adjustment)	R_4		100		kΩ	

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

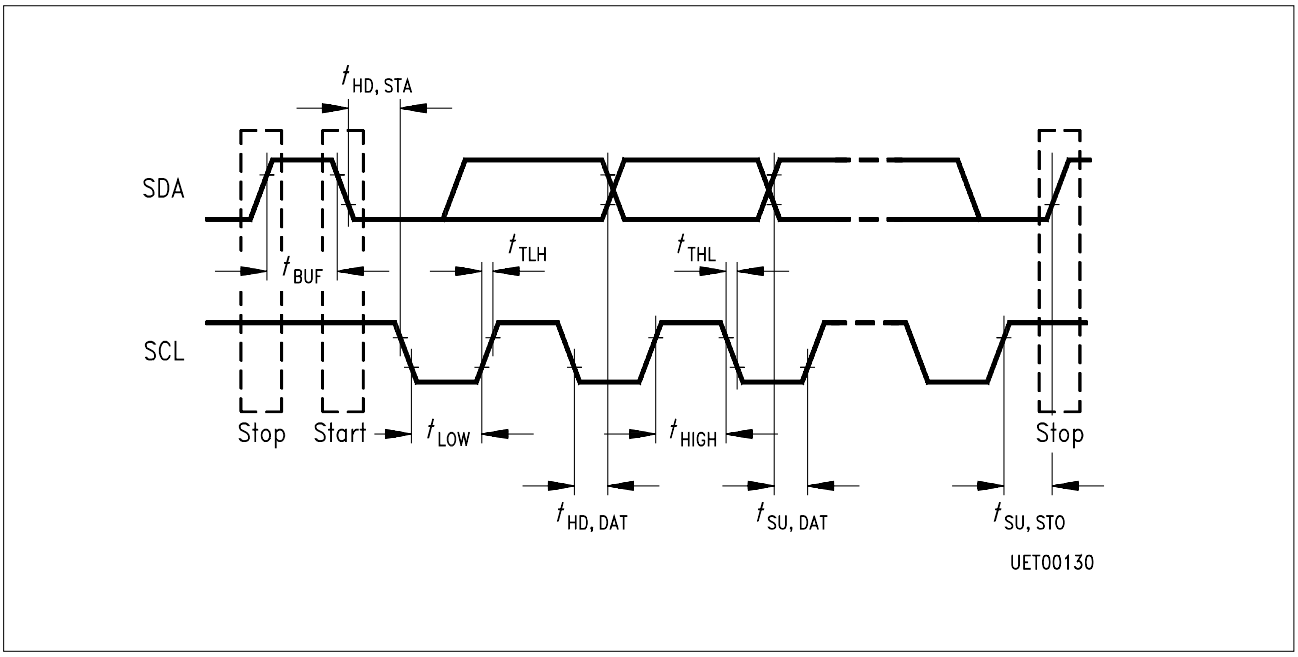


Figure 3
I²C-Bus Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency	f_{SCL}	0	100	kHz
Inactive time prior to new transmission start-up	t_{BUF}	4.7		µs
Hold time during start condition	$t_{HD; STA}$	4.0		µs
Low-period of clock	t_{LOW}	4.7		µs
High-period of clock	t_{HIGH}	4.0		µs
Set-up time for data	$t_{SU;DAT}$	250		ns
Rise time for SDA and SCL signal	t_{TLH}		1	µs
Fall time for SDA and SCL signal	t_{THL}		300	ns
Set-up time for SCL clock during stop condition	$t_{SU; STO}$	4.7		µs

All values referred to V_{IH} and V_{IL} levels.

4 VPS-Receiver

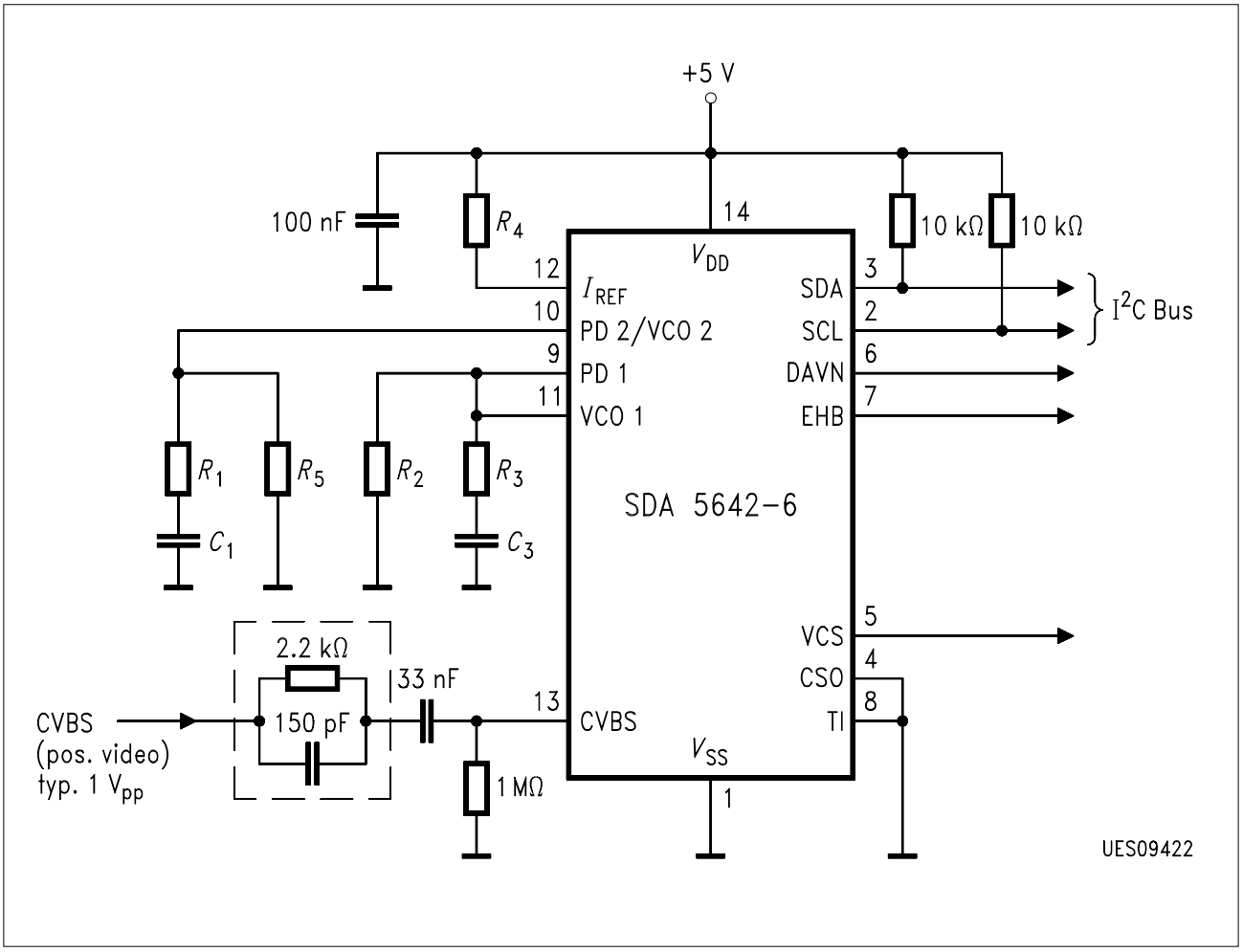


Figure 4

5 Appendix

5.1 Control Register Write (I^2C-Bus Write)

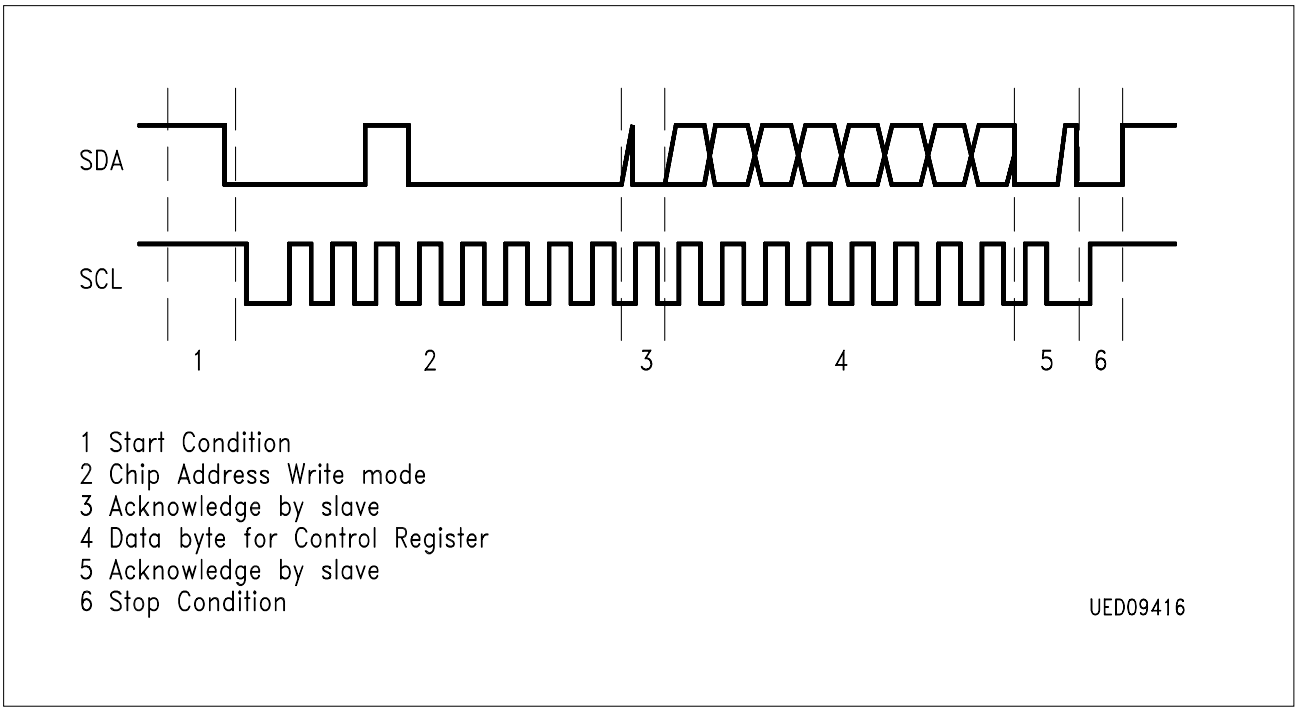


Figure 5

5.2 Data Register Read (I^2C-Bus Read)

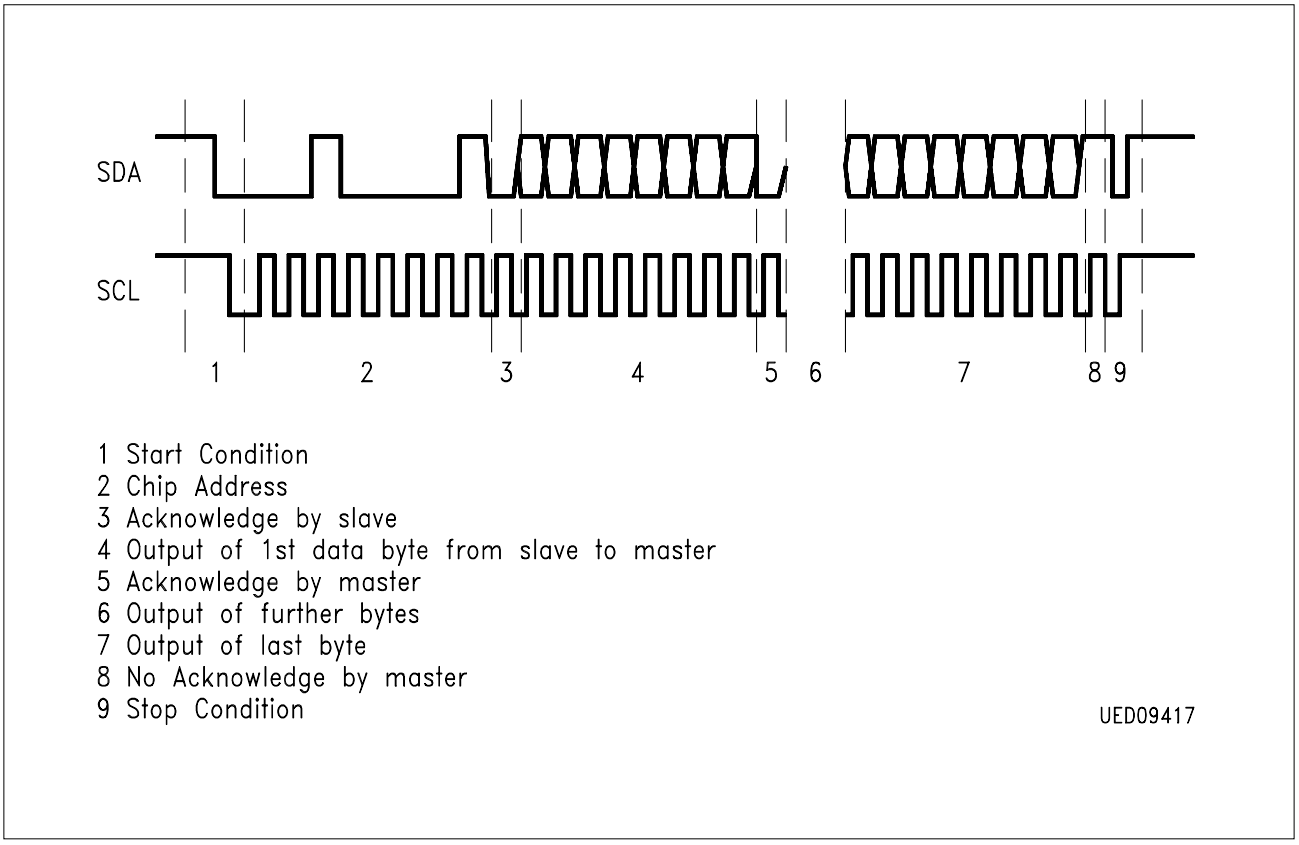


Figure 6

5.3 DAVN and EHB Timing

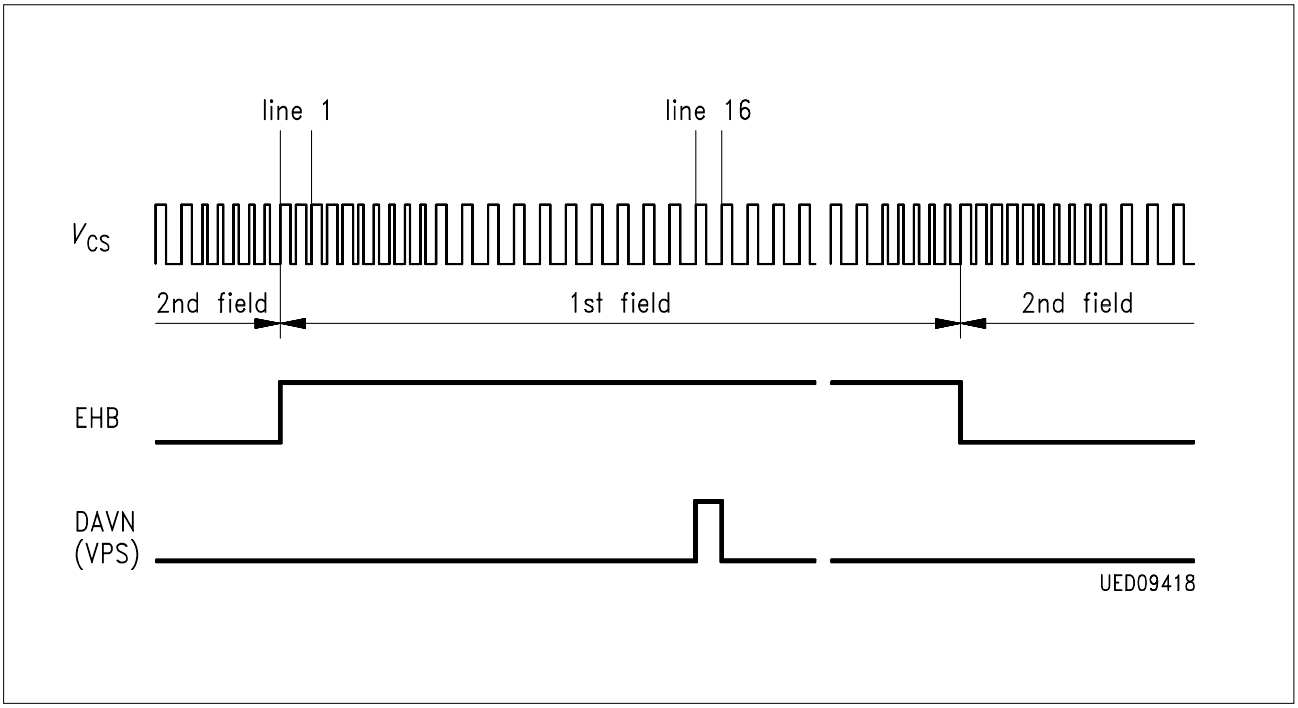


Figure 7

5.4 Position of VPS Data Lines within the Vertical Blanking Interval

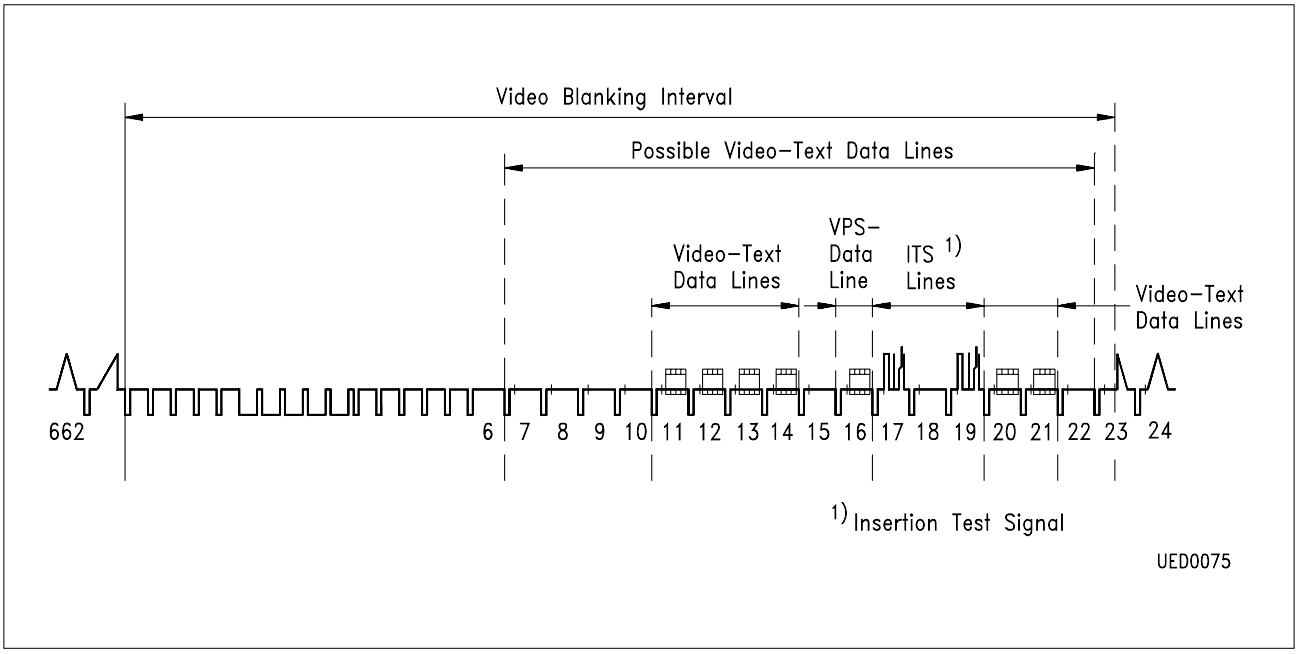


Figure 8

1) (shown for first field)

5.5 Definition of Voltage Levels for VPS Data Line

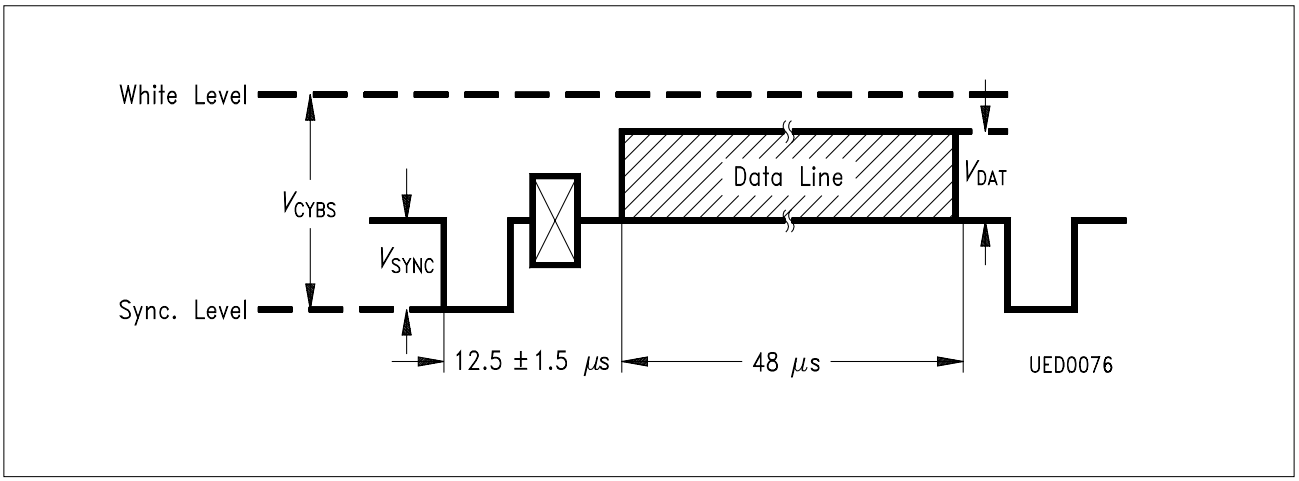


Figure 9

5.6 Data Format of Programme Delivery Data in the Dedicated TV Line (VPS)

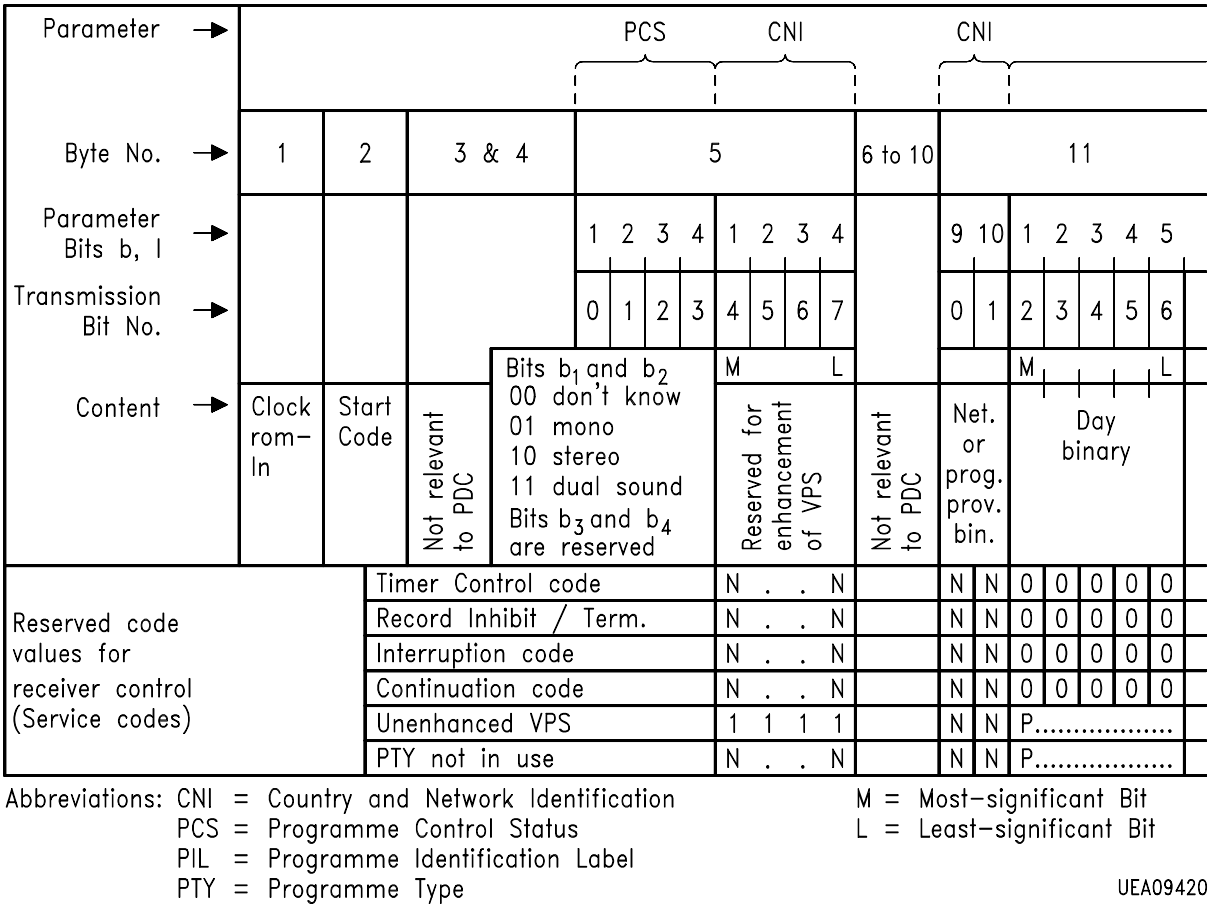
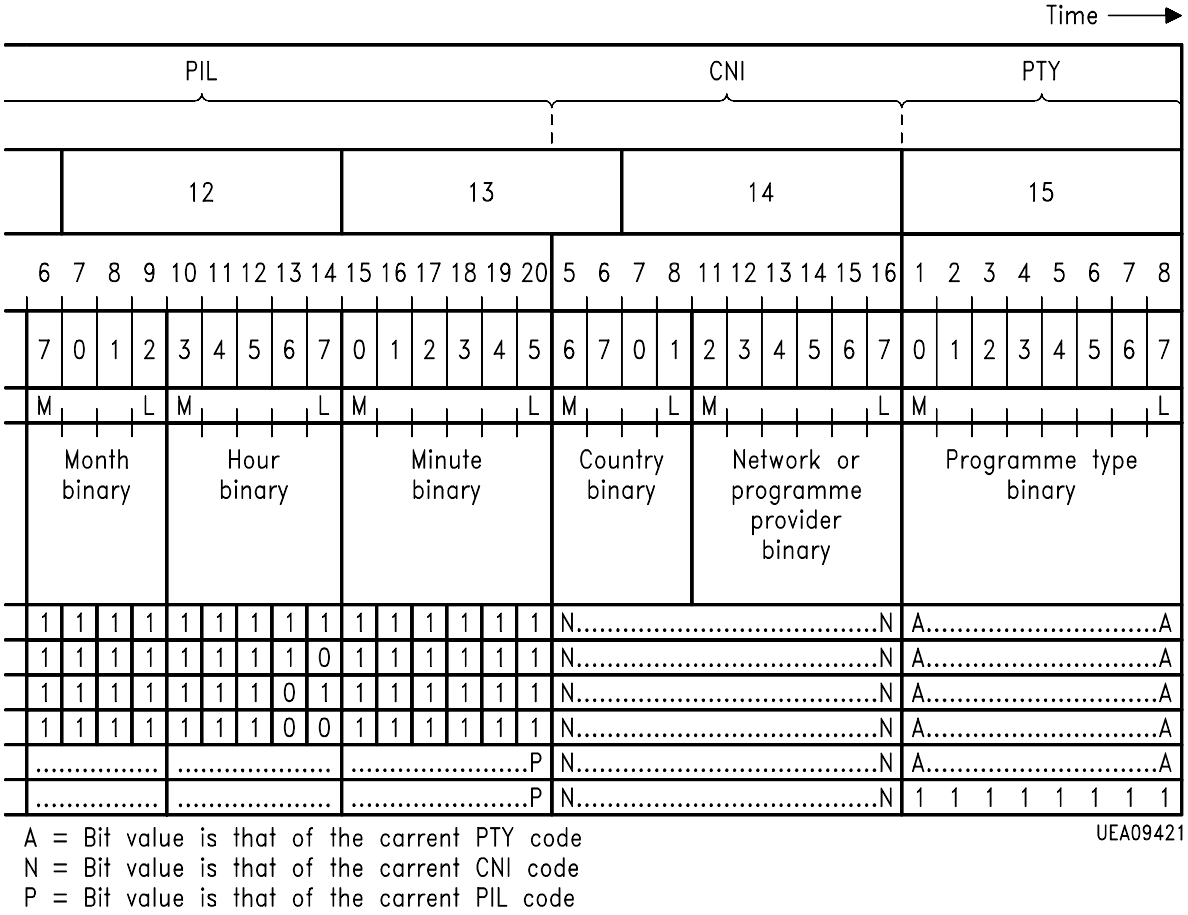


Figure 10

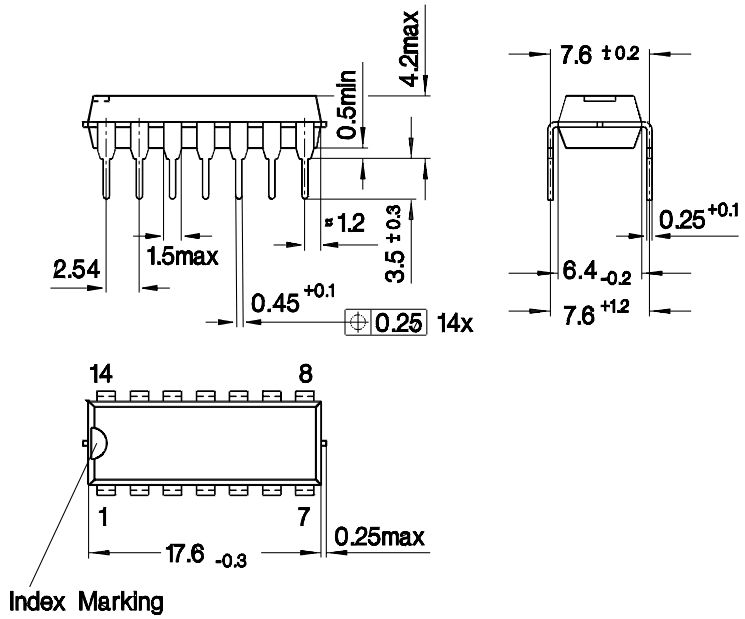


A = Bit value is that of the carrent PTY code
N = Bit value is that of the carrent CNI code
P = Bit value is that of the carrent PIL code

Figure 11

6 Package Outlines

P-DIP-14-1
(Plastic Dual In-line Package)

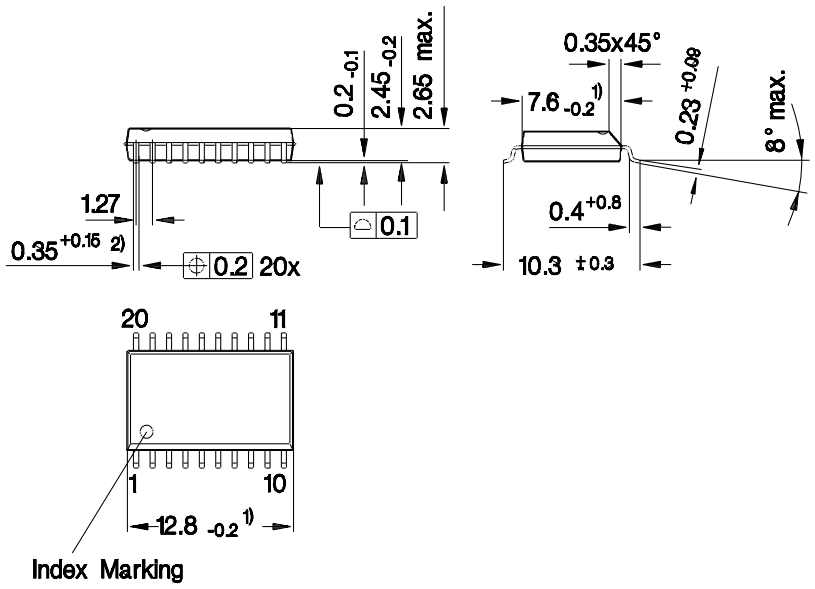


GPD05005

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

Dimensions in mm

P-DSO-20-1
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

GPS05094

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm