

QUAD/OCTAL 6BIT D/A CONVERTER  
CMOS LSI

DESCRIPTION

$\mu$ PD6325 Serie are 6 bit D/A Converter for control volumn, brightness, contrast, color or tone of TV set. The data are transferring serially from micro-computer.

| $\mu$ PD6325 Serie Line-up                       | QUAD D/A             | OCTAL D/A     |
|--|----------------------|---------------|
| D/A output is consist of Emitter follower buffer | $\mu$ PD6325C, 6325G | $\mu$ PD6326C |
| Non buffer output                                | $\mu$ PD6335C, 6335G | $\mu$ PD6336C |

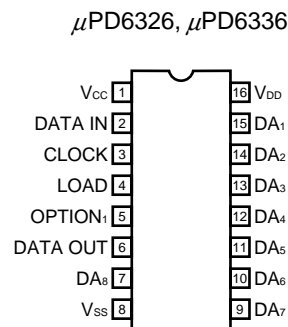
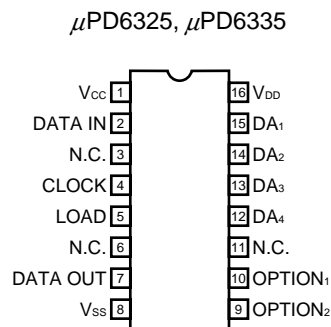
FEATURES

- R-2R ladder D/A
- Serial Data input (DATA IN, CLOCK, LOAD)
- Power supply voltage of interface is 5 V (Vcc) and D/A reference voltage is free (Vcc to 15 V).

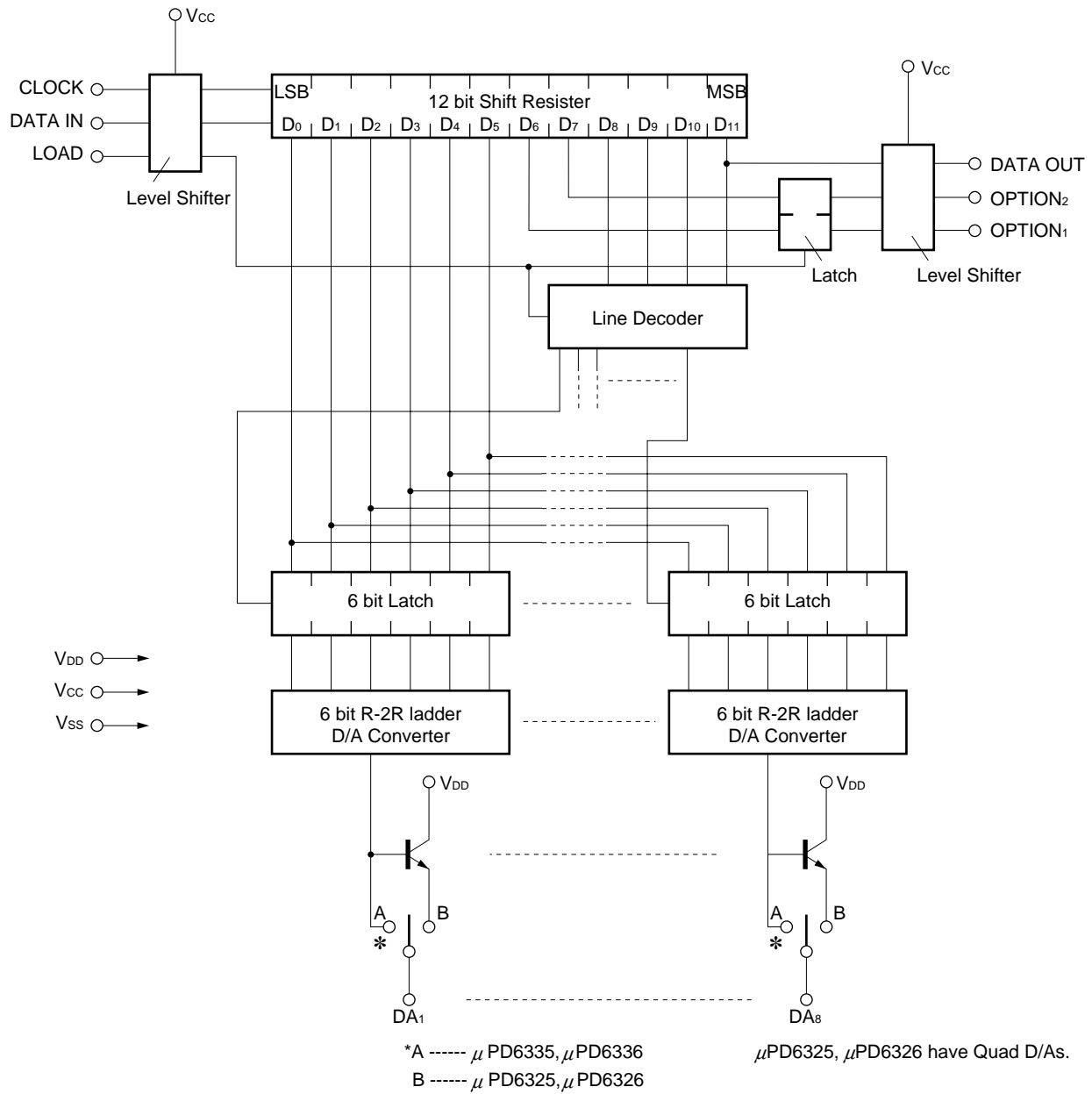
ORDERING INFORMATION

| Part No.      | Package                      |
|---------------|------------------------------|
| $\mu$ PD6325C | 16-pin plastic DIP (300 mil) |
| $\mu$ PD6325G | 16-pin plastic SOP (300 mil) |
| $\mu$ PD6326C | 16-pin plastic DIP (300 mil) |
| $\mu$ PD6335C | 16-pin plastic DIP (300 mil) |
| $\mu$ PD6335G | 16-pin plastic SOP (300 mil) |
| $\mu$ PD6336C | 16-pin plastic DIP (300 mil) |

PIN CONNECTION DIAGRAM (Top View)



BLOCK DIAGRAM



PIN CONFIGURATION

| Pin No.          |                  | Symbol              | Pin Name                | Function   |
|------------------|------------------|---------------------|-------------------------|--|
| μPD 6325<br>6335 | μPD 6326<br>6336 |                     |                         |  |
| 1                | 1                | V <sub>CC</sub>     | Interface Power Supply  | This pin is used to interface with the control IC (ex. micro processor). Supply the voltage high level of the control IC.                              |
| 2                | 2                | DATA IN             | Serial Data Input       | Control data input terminal. Data is read in synchronization with the clocks input to the CLOCK terminal.  |
| 4                | 3                | CLOCK               | Shift Clock Input       | Data read clock input terminal. The Data input to the DATA IN terminal is read at the leading edge of the clock.                                       |
| 5                | 4                | LOAD                | Load Pulse Input        | This terminal is used to input Load signals after inputting serial data. 12 bit data is read after leading edge of a pulse input to the LOAD terminal. |
| 7                | 6                | DATA OUT            | Serial Data Output      | Serial data output terminal. The final stage data of 12 bit shift register appears on this terminal in synchronization with shift clock.               |
| 8                | 8                | V <sub>SS</sub>     | Ground                  | System ground.   |
| 9                | –                | OPTION <sub>2</sub> | Expansion Output Port   | D <sub>7</sub> the data of the shift register appears on this terminal. (Only μPD6325 and μPD6335)   |
| 10               | 5                | OPTION <sub>1</sub> | Expansion Output Port   | D <sub>6</sub> the data of the shift register appears on this terminal.  |
| –                | 7                | DA <sub>8</sub>     | Analog Output Channel 8 | Analog Output  |
| –                | 9                | DA <sub>7</sub>     | Analog Output Channel 7 | Analog Output  |
| –                | 10               | DA <sub>6</sub>     | Analog Output Channel 6 | Analog Output  |
| –                | 11               | DA <sub>5</sub>     | Analog Output Channel 5 | Analog Output  |
| 12               | 12               | DA <sub>4</sub>     | Analog Output Channel 4 | Analog Output  |
| 13               | 13               | DA <sub>3</sub>     | Analog Output Channel 3 | Analog Output  |
| 14               | 14               | DA <sub>2</sub>     | Analog Output Channel 2 | Analog Output  |
| 15               | 15               | DA <sub>1</sub>     | Analog Output Channel 1 | Analog Output  |
| 16               | 16               | V <sub>DD</sub>     | Power Supply            | Reference Voltage for D/A converters. Analog output voltage range is GND to V <sub>DD</sub> .  |

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C)**

|                          |                                   |  |    |
|--------------------------|-----------------------------------|--|----|
| Supply Voltage           | V <sub>DD</sub> , V <sub>CC</sub> | -0.5 to +18, V <sub>CC</sub> ≤ V <sub>DD</sub> | V  |
| Output Voltage           | V <sub>OUT</sub>                  | -0.5 to V <sub>DD</sub> +0.5                   | V  |
| Input Voltage            | V <sub>IN</sub>                   | -0.5 to V <sub>CC</sub> +0.5                   | V  |
| Input Current            | I <sub>IN</sub>                   | 10   | mA |
| Emitter Follower Current | I <sub>OE</sub>                   | 10   | mA |
| Power Dissipation        | P <sub>D</sub>                    | 500*/200**                                     | mW |
| Operating Temperature    | T <sub>A</sub>                    | -40 to +85                                     | °C |
| Storage Temperature      | T <sub>stg</sub>                  | -65 to +125                                    | °C |

\*DIP

\*\*SOP

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER   | SYMBOL               | MIN.            | TYP. | MAX. | UNIT | CONDITION  |
|---|----------------------|-----------------|------|------|------|--|
| Supply Voltage  | V <sub>DD</sub>      | V <sub>CC</sub> |      | 15   | V    | V <sub>CC</sub> ≤ V <sub>DD</sub>                  |
| Supply Voltage of Interface   | V <sub>CC</sub>      | 4.5             | 5.0  | 5.5  | V    | V <sub>CC</sub> ≤ V <sub>DD</sub>                  |
| Low Level Input Voltage   | V <sub>IL</sub>      |                 |      | 0.8  | V    | V <sub>CC</sub> = 5 V, V <sub>DD</sub> = 5 to 15 V |
| High Level Input Voltage  | V <sub>IH</sub>      | 3.5             |      |      | V    | V <sub>CC</sub> = 5 V, V <sub>DD</sub> = 5 to 15 V |
| Only μPD6325 & μPD6326  |                      |                 |      |      |      |  |
| Emitter Follower Power Dissipation 1  | P <sub>E</sub> /unit |                 |      | 5    | mW   | T <sub>A</sub> = 85 °C                             |
| Emitter Follower Power Dissipation 2  | P <sub>E</sub> /unit |                 |      | 15   | mW   | T <sub>A</sub> = 70 °C                             |
| Emitter Follower Power Dissipation 3  | P <sub>E</sub> total |                 |      | 25   | mW   | T <sub>A</sub> = 85 °C                             |
| Emitter Follower Power Dissipation 4  | P <sub>E</sub> total |                 |      | 75   | mW   | T <sub>A</sub> = 70 °C                             |
| TIMING CONDITIONS (T <sub>A</sub> = -40 to +85 °C, V <sub>SS</sub> = 0 V, V <sub>CC</sub> = 5 V, V <sub>DD</sub> = V <sub>CC</sub> to 15 V) |                      |                 |      |      |      |  |
| CLOCK High Level Width  | t <sub>CH</sub>      | 4.0             |      |      | μS   |  |
| CLOCK Low Level Width   | t <sub>CL</sub>      | 10.0            |      |      | μS   |  |
| CLOCK Rise Time   | t <sub>cr</sub>      |                 |      | 1.0  | μS   |  |
| CLOCK Fall Time   | t <sub>cf</sub>      |                 |      | 1.0  | μS   |  |
| DATA IN Setup Time  | t <sub>Dsetup</sub>  | 2               |      |      | μS   |  |
| DATA IN Hold Time   | t <sub>Dhold</sub>   | 10              |      |      | μS   |  |
| Pulse Width, LOAD High  | t <sub>W(LOAD)</sub> | 4               |      |      | μS   |  |
| LOAD Lead Time  | t <sub>Lead</sub>    | 10              |      |      | μS   |  |
| LOAD Lag Time   | t <sub>Llag</sub>    | 10              |      |      | μS   |  |

## ELECTRICAL CHARACTERISTICS

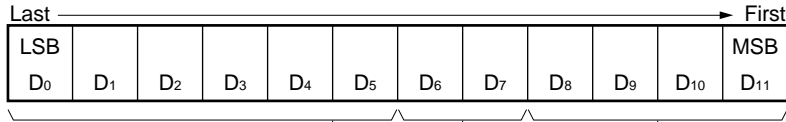
(T<sub>A</sub> = -40 to +85°C, V<sub>SS</sub> = 0 V, V<sub>CC</sub> = 4.5 to 5.5 V, V<sub>DD</sub> = V<sub>CC</sub> to 15 V)

| PARAMETER                             | SYMBOL                        | MIN. | TYP. | MAX.    | UNIT    | CONDITION  |
|---------------------------------------|-------------------------------|------|------|---------|---------|--|
| Current Consumption                   | I <sub>DD</sub>               |      |      | 15      | mA      | No Load, for $\mu$ PD6326, 6336                      |
| Current Consumption                   | I <sub>DD</sub>               |      |      | 10      | mA      | No Load, for $\mu$ PD6325, 6335                      |
| Current Consumption of Interface      | I <sub>CC</sub>               |      |      | 10      | $\mu$ A | No Load of DATA OUT,<br>Static Consumption           |
| Input Leak Current                    | I <sub>I<sub>LEAK</sub></sub> |      |      | $\pm 1$ | $\mu$ A | V <sub>IN</sub> = V <sub>CC</sub> or V <sub>SS</sub> |
| DATA OUT High Level<br>Output Voltage | I <sub>OH</sub>               | -100 |      |         | $\mu$ A | V <sub>OH</sub> = V <sub>DD</sub> - 0.5 V            |
| DATA OUT Low Level<br>Output Voltage  | I <sub>OL</sub>               | 100  |      |         | $\mu$ A | V <sub>OL</sub> = 0.5 V                              |
| Emitter Follower Leak Current         | I <sub>OLEAK</sub>            |      |      | 20      | $\mu$ A | for $\mu$ PD6325, 6326                               |
| Settling Time                         | t <sub>DA set</sub>           |      |      | 10      | $\mu$ s | <b>Note</b>  |

**Note**  $\mu$ PD6325, 6326: R<sub>L</sub> = 20 k $\Omega$ , C<sub>L</sub> = 50 pF  
 $\mu$ PD6335, 6336: No Load.

DATA CONFIGURATION

Data Length is 12 bit.



D/A output CONTROL BIT

| D11 | D10 | D9 | D8 | Select D/A      | Target device                  |
|-----|-----|----|----|-----------------|--------------------------------|
| 0   | 0   | 0  | 0  | Don't Care      | μPD6325, 6326<br>μPD6335, 6336 |
| 0   | 0   | 0  | 1  | DA <sub>1</sub> | μPD6325, 6326<br>μPD6335, 6336 |
| 0   | 0   | 1  | 0  | DA <sub>2</sub> | μPD6325, 6326<br>μPD6335, 6336 |
| 0   | 0   | 1  | 1  | DA <sub>3</sub> | μPD6325, 6326<br>μPD6335, 6336 |
| 0   | 1   | 0  | 0  | DA <sub>4</sub> | μPD6325, 6326<br>μPD6335, 6336 |
| 0   | 1   | 0  | 1  | DA <sub>5</sub> | μPD6326<br>μPD6336             |
| 0   | 1   | 1  | 0  | DA <sub>6</sub> | μPD6326<br>μPD6336             |
| 0   | 1   | 1  | 1  | DA <sub>7</sub> | μPD6326<br>μPD6336             |
| 1   | 0   | 0  | 0  | DA <sub>8</sub> | μPD6326<br>μPD6336             |
| 1   | ×   | ×  | ×  | Don't Care      | μPD6325, 6326<br>μPD6335, 6336 |

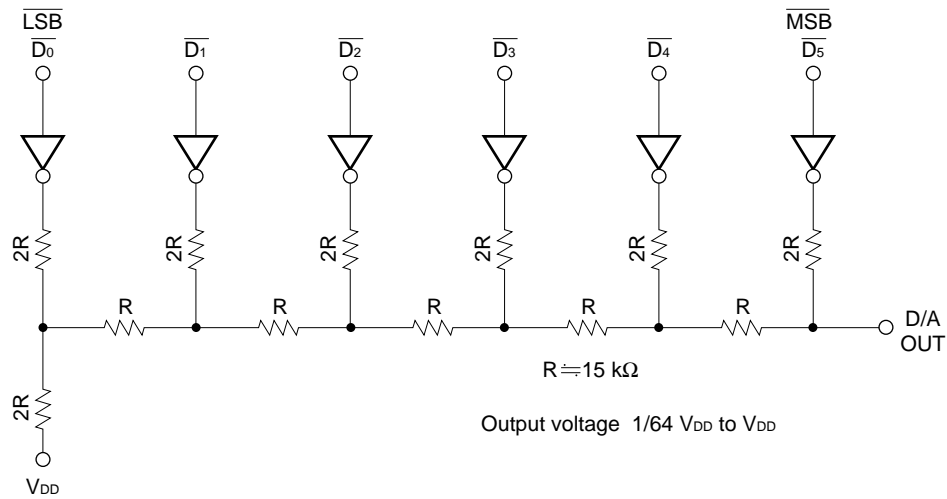
OPTION output CONTROL BIT

| D7 | D6 | OPTION <sub>1</sub><br>out. | OPTION <sub>2</sub><br>out. | Note                             |
|----|----|-----------------------------|-----------------------------|----------------------------------|
| 0  | 0  | L                           | L                           | OPTION2 is only<br>μPD6325, 6326 |
| 0  | 1  | H                           | L                           | OPTION2 is only<br>μPD6325, 6326 |
| 1  | 0  | L                           | H                           | OPTION2 is only<br>μPD6325, 6326 |
| 1  | 1  | H                           | H                           | OPTION2 is only<br>μPD6325, 6326 |

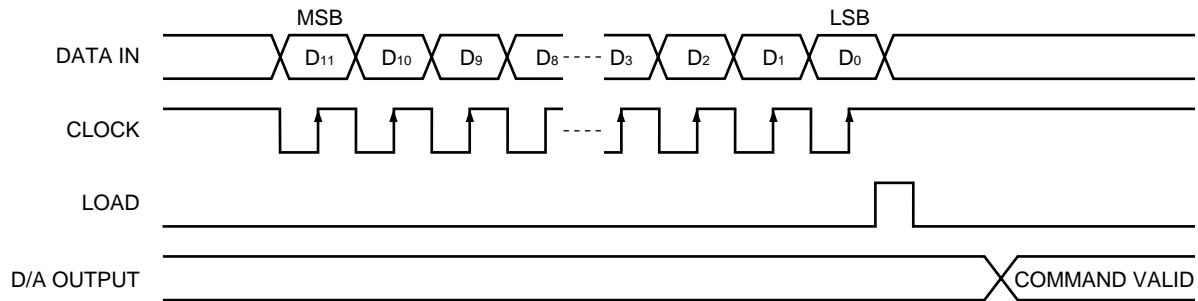
D/A Output Voltage CONTROL BIT

| D5 | D4 | D3 | D2 | D1 | D0 | Output Voltage             |
|----|----|----|----|----|----|----------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | ≡ V <sub>DD</sub> /64      |
| 0  | 0  | 0  | 0  | 0  | 1  | ≡ 2 x V <sub>DD</sub> /64  |
| 0  | 0  | 0  | 0  | 1  | 0  | ≡ 3 x V <sub>DD</sub> /64  |
| 0  | 0  | 0  | 0  | 1  | 1  | ≡ 4 x V <sub>DD</sub> /64  |
| ⋮  | ⋮  | ⋮  | ⋮  | ⋮  | ⋮  | ⋮                          |
| 1  | 1  | 1  | 1  | 1  | 0  | ≡ 63 x V <sub>DD</sub> /64 |
| 1  | 1  | 1  | 1  | 1  | 1  | ≡ V <sub>DD</sub>          |

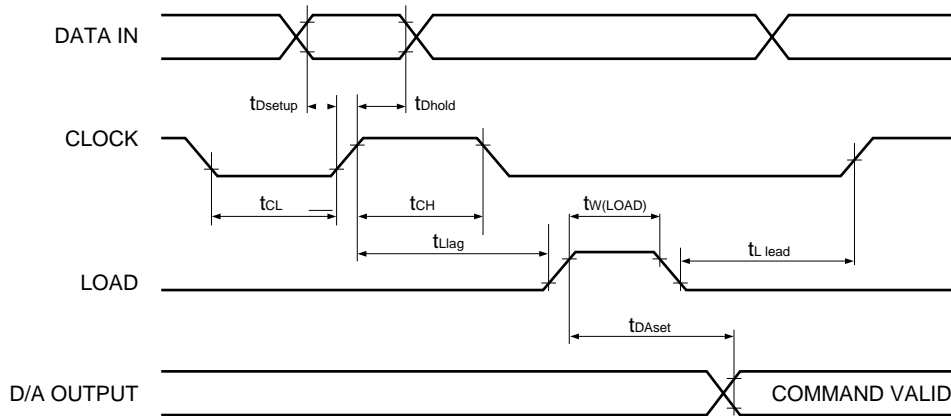
EQUIVALENT CIRCUIT OF 6 bit D/A



TIMING CHART

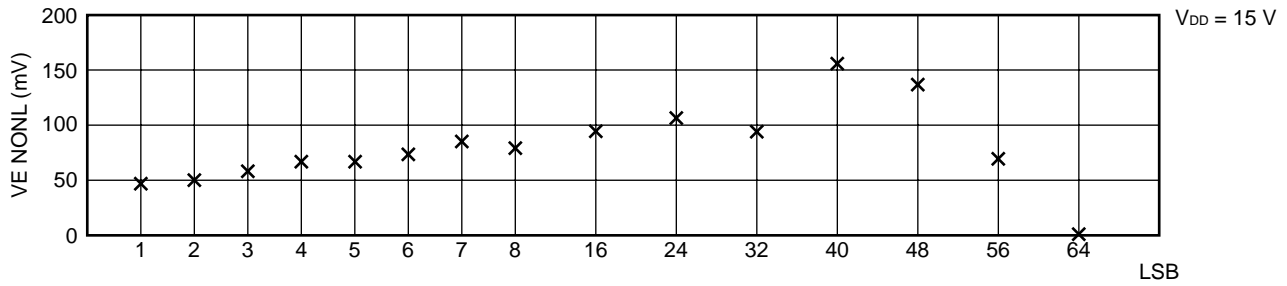
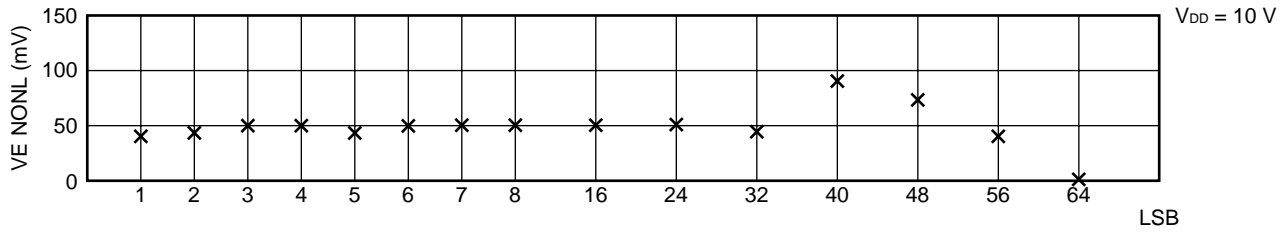
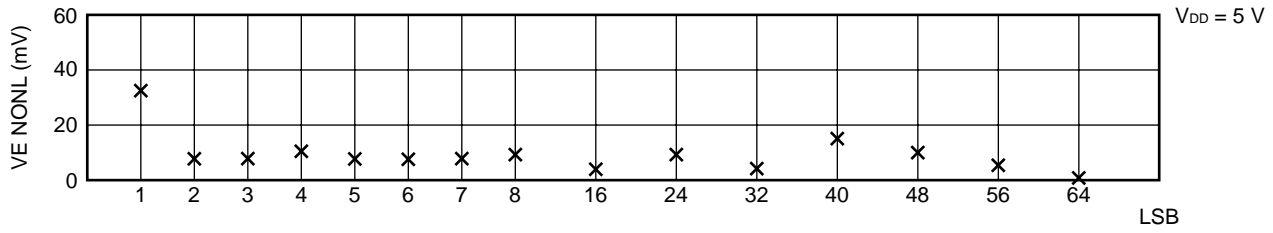


Data is loaded when LOAD is high level.

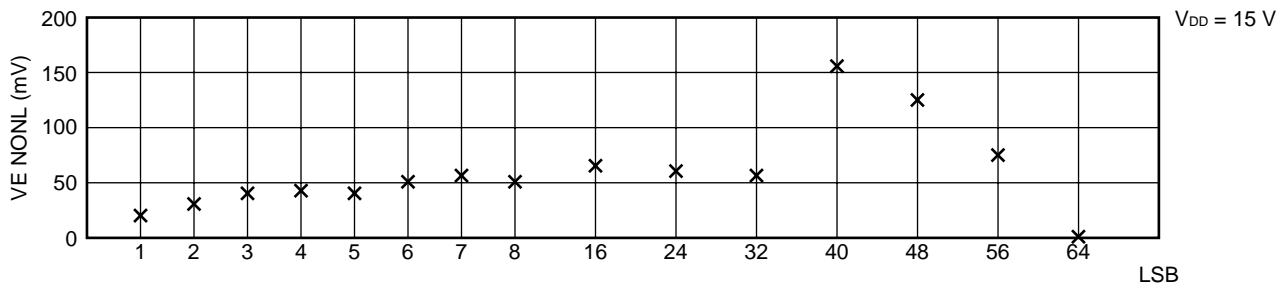
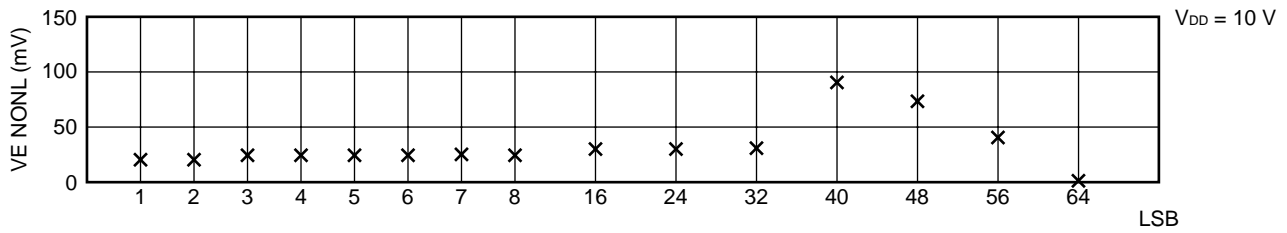
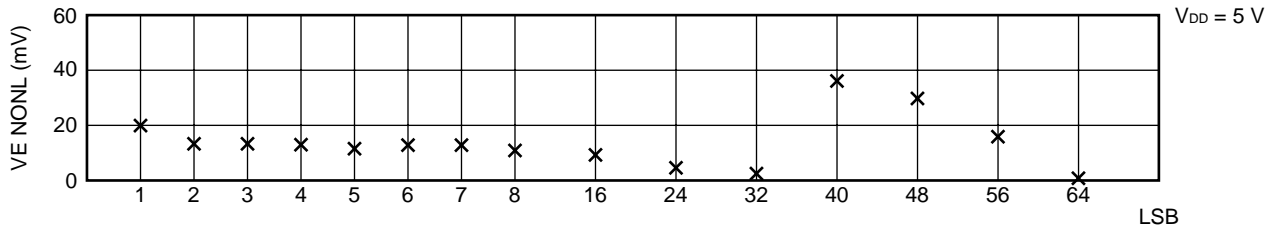


LINIARITY OF D/A OUTPUT ( $\mu$ PD6335, 6336) (TYP.)

• $T_A = -40\text{ }^\circ\text{C}$

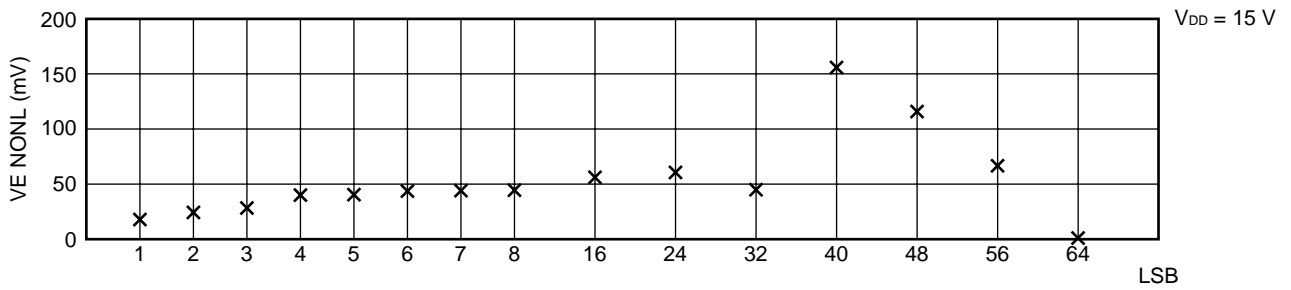
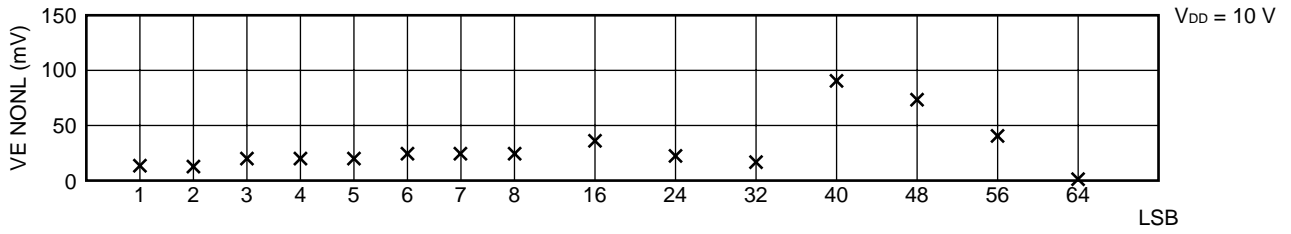
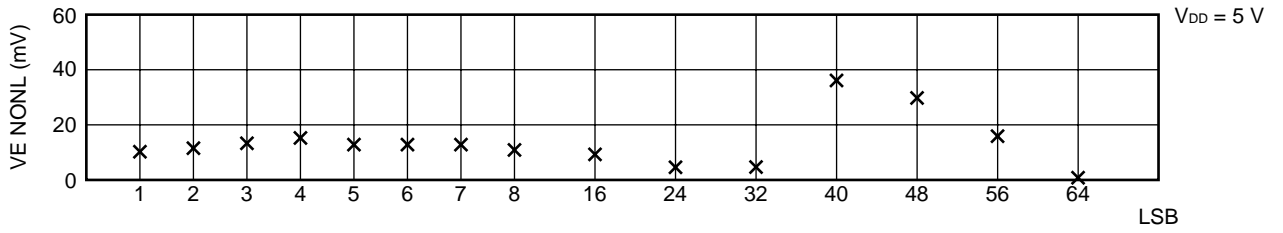


• $T_A = 25\text{ }^\circ\text{C}$





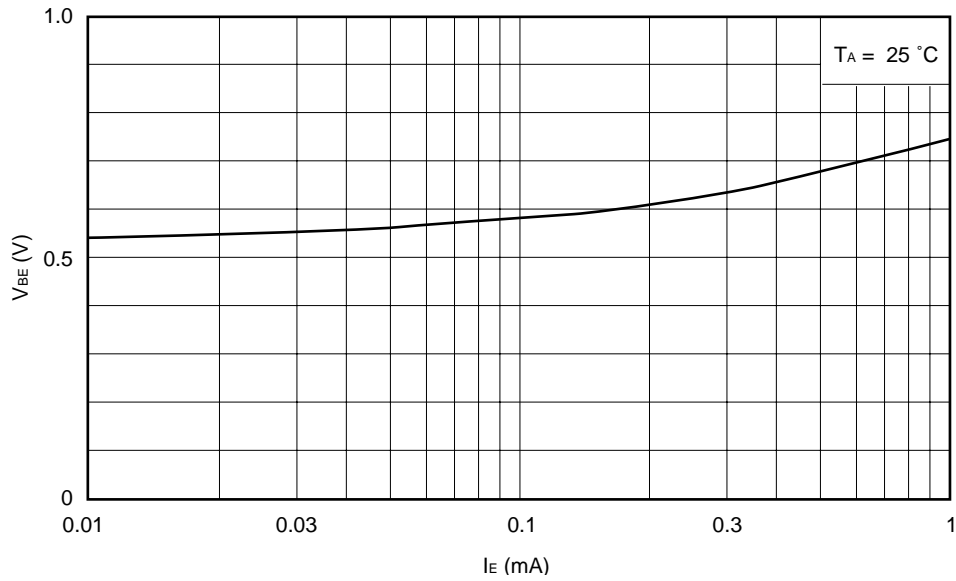
• $T_A = 85\text{ }^\circ\text{C}$



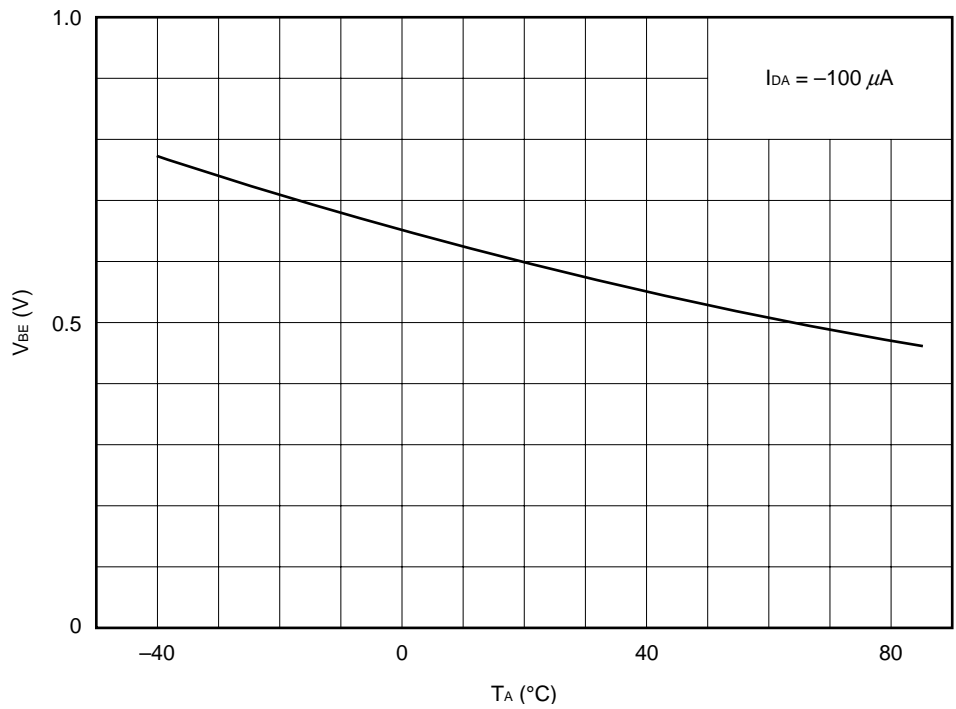
\*  $VE\ NONL = (MEASUREMENT\ VALUE) - (IDEAL\ VALUE)$

Characteristics of Emitter follower buffer ( $\mu$ PD6325, 6326)

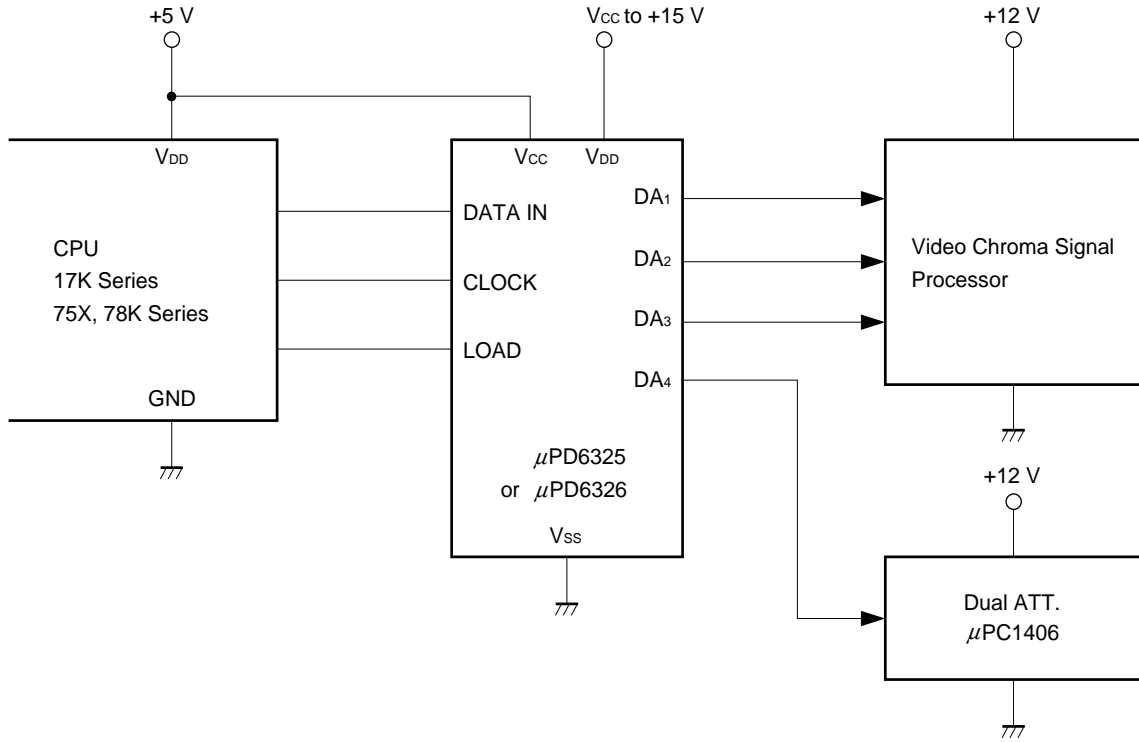
(1)  $V_{BE} - I_E$  (including R-2R's resistor)



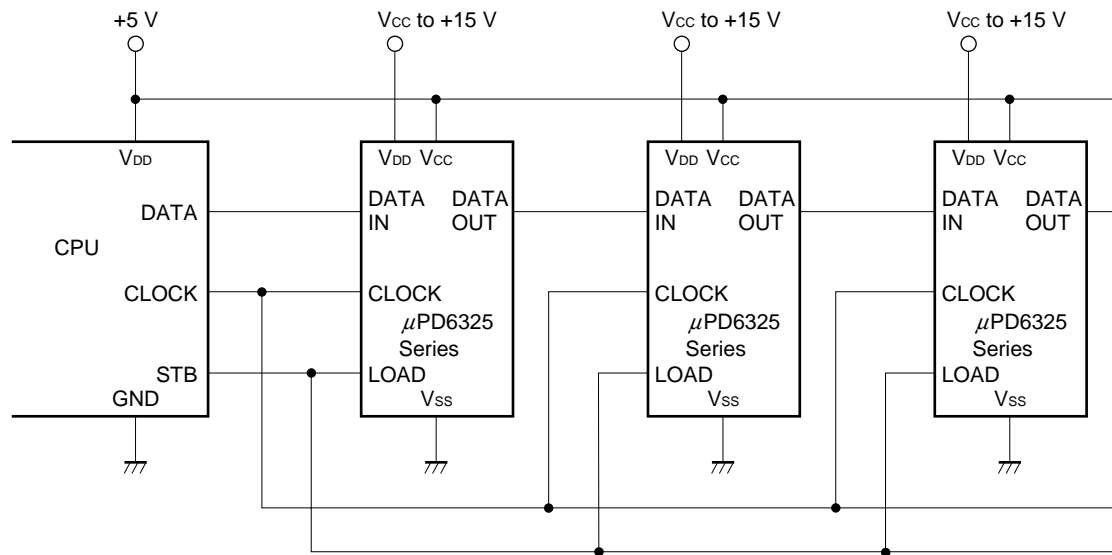
(2)  $V_{BE} - T_A$



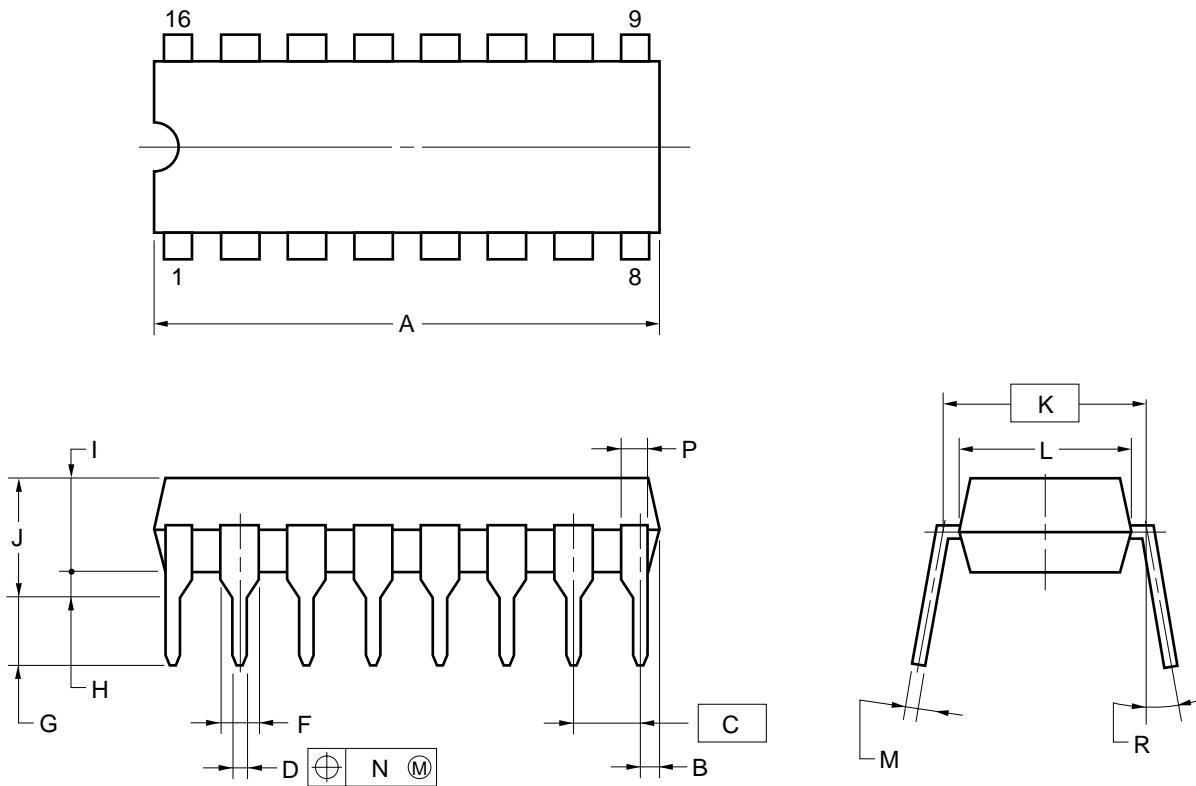
APPLICATION FOR TV SET



APPLICATION FOR CASCADE CONNECTING



16PIN PLASTIC DIP (300 mil)



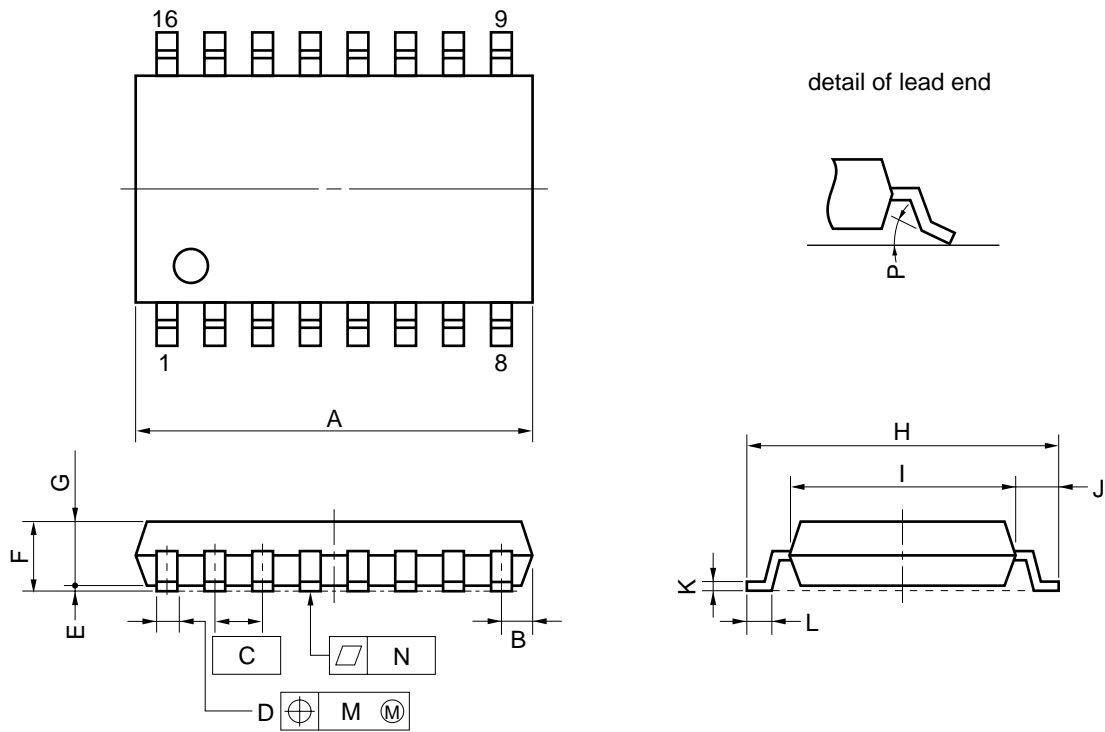
NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS                            | INCHES                                    |
|------|--|---|
| A    | 20.32 MAX.                             | 0.800 MAX.                                |
| B    | 1.27 MAX.                              | 0.050 MAX.                                |
| C    | 2.54 (T.P.)                            | 0.100 (T.P.)                              |
| D    | 0.50±0.10                              | 0.020 <sup>+0.004</sup> <sub>-0.005</sub> |
| F    | 1.2 MIN.                               | 0.047 MIN.                                |
| G    | 3.5±0.3                                | 0.138±0.012                               |
| H    | 0.51 MIN.                              | 0.020 MIN.                                |
| I    | 4.31 MAX.                              | 0.170 MAX.                                |
| J    | 5.08 MAX.                              | 0.200 MAX.                                |
| K    | 7.62 (T.P.)                            | 0.300 (T.P.)                              |
| L    | 6.4                                    | 0.252                                     |
| M    | 0.25 <sup>+0.10</sup> <sub>-0.05</sub> | 0.010 <sup>+0.004</sup> <sub>-0.003</sub> |
| N    | 0.25                                   | 0.01                                      |
| P    | 1.0 MIN.                               | 0.039 MIN.                                |
| R    | 0~15°                                  | 0~15°                                     |

P16C-100-300A,C-1

16 PIN PLASTIC SOP (300 mil)



**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS                            | INCHES                                    |
|------|--|---|
| A    | 10.46 MAX.                             | 0.412 MAX.                                |
| B    | 0.78 MAX.                              | 0.031 MAX.                                |
| C    | 1.27 (T.P.)                            | 0.050 (T.P.)                              |
| D    | 0.40 <sup>+0.10</sup> <sub>-0.05</sub> | 0.016 <sup>+0.004</sup> <sub>-0.003</sub> |
| E    | 0.1±0.1                                | 0.004±0.004                               |
| F    | 1.8 MAX.                               | 0.071 MAX.                                |
| G    | 1.55                                   | 0.061                                     |
| H    | 7.7±0.3                                | 0.303±0.012                               |
| I    | 5.6                                    | 0.220                                     |
| J    | 1.1                                    | 0.043                                     |
| K    | 0.20 <sup>+0.10</sup> <sub>-0.05</sub> | 0.008 <sup>+0.004</sup> <sub>-0.002</sub> |
| L    | 0.6±0.2                                | 0.024 <sup>+0.008</sup> <sub>-0.009</sub> |
| M    | 0.12                                   | 0.005                                     |
| N    | 0.10                                   | 0.004                                     |
| P    | 3° <sup>+7°</sup> <sub>-3°</sub>       | 3° <sup>+7°</sup> <sub>-3°</sub>          |

P16GM-50-300B-4

## REFERENCE

| Document Name   | Document No. |
|---|--------------|
| NEC semiconductor device reliability/quality control system | IEI-1212     |
| Quality grade on NEC semiconductor devices                  | C11531E      |
| Semiconductor device mounting technology manual             | C10535E      |
| Semiconductor device package manual                         | C10943X      |
| Guide to quality assurance for semiconductor devices        | MEI-1202     |
| Semiconductor selection guide                               | X10679E      |

[MEMO]

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