μPD9903 ANALOG SUBSCRIBER LINE LSI (DIGITAL CODEC)

The μPD9903 is a digital CODEC that can be used in analog subscriber circuits such as private branch exchangers (PBXs) and switching equipment for central offices. It features three of the functions required for analog subscriber circuits: 2W/4W conversion, CODEC supervision, and subscriber line supervision.

Use of the μPD9903 in combination with a BS-SLIC (μPC7073) can reduce the number of components required in analog subscriber circuits.

FEATURES

- Single-chip monolithic LSI (CMOS)
- PCM CODEC $\rightarrow$ oversampling-type A/D and D/A converters
- Programmable functions
  - Termination impedance
  - Hybrid balance network
  - Feed resistance
  - Feed current
  - PAD control
  - A-law and μ-law
- Digital gain set function
- Ring-Trip function
- Single power supply (+5 V)
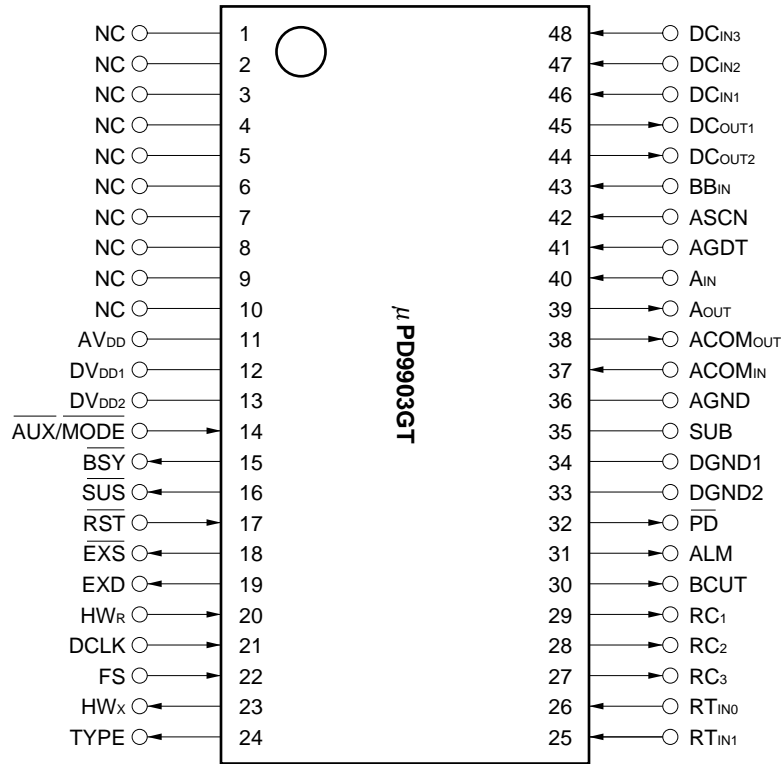- Low power consumption during standby mode: 20 mW (TYP.)

ORDERING INFORMATION

Part Number	Package
μPD9903GT	48-pin plastic shrink SOP (375 mil)

The mark ★ shows major revised points.

PIN CONFIGURATION (Top View)

48-pin plastic shrink SOP (375 mil)

Left pins		Right pins	
NC	1	48	DC_{IN3}
NC	2	47	DC_{IN2}
NC	3	46	DC_{IN1}
NC	4	45	DC_{OUT1}
NC	5	44	DC_{OUT2}
NC	6	43	BB_{IN}
NC	7	42	ASCN
NC	8	41	AGDT
NC	9	40	A_{IN}
NC	10	39	A_{OUT}
AV_{DD}	11	38	$ACOM_{OUT}$
DV_{DD1}	12	37	$ACOM_{IN}$
DV_{DD2}	13	36	AGND
$\overline{AUX}$/MODE	14	35	SUB
$\overline{BSY}$	15	34	DGND1
$\overline{SUS}$	16	33	DGND2
$\overline{RST}$	17	32	$\overline{PD}$
$\overline{EXS}$	18	31	ALM
EXD	19	30	BCUT
HW_R	20	29	RC_1
DCLK	21	28	RC_2
FS	22	27	RC_3
HW_X	23	26	RT_{IN0}
TYPE	24	25	RT_{IN1}

Device marking: μ**PD9903GT**

$ACOM_{IN}$	: ANALOG COMMON VOLTAGE IN	DGND1, DGND2	: DIGITAL GROUND
$ACOM_{OUT}$	: ANALOG COMMON VOLTAGE OUT	DV_{DD1}, DV_{DD2}	: DIGITAL POSITIVE POWER SUPPLY
AGDT	: ANALOG GROUND DETECTION SIGNAL IN	EXD	: EXPANSION PORT DATA
AGND	: ANALOG GROUND	$\overline{EXS}$	: EXPANSION PORT SYNCHRONIZATION
A_{IN}	: ANALOG SIGNAL IN	FS	: FRAME SYNCHRONOUS CLOCK IN
ALM	: ALARM OUT	HW_R	: RECEIVE HIGHWAY DATA IN
A_{OUT}	: ANALOG SIGNAL OUT	HW_X	: TRANSMIT HIGHWAY DATA OUT
ASCN	: ANALOG LOOP DETECTION SIGNAL IN	NC	: NO CONNECTION
$\overline{AUX}$/MODE	: EXTERNAL SIGNAL IN/MODE CONTROL SET	$\overline{PD}$	: POWER DOWN CONTROL OUT
AV_{DD}	: ANALOG POSITIVE POWER SUPPLY	RC_1 - RC_3	: RELAY CONTROL OUT
BB_{IN}	: V_{BB} VOLTAGE INFORMATION IN	$\overline{RST}$	: RESET IN
BCUT	: BATTERY FEED CUT SIGNAL OUT	RT_{IN0}, RT_{IN1}	: RING TRIP SIGNAL IN
$\overline{BSY}$	: BUSY SIGNAL OUT	SUB	: SUB GROUND
DC_{IN1} - DC_{IN3}	: DC FEEDBACK CONTROL IN	$\overline{SUS}$	: SUSPEND SIGNAL OUT
DCLK	: DATA CLOCK IN	TYPE	: TYPE SIGNAL OUT
DC_{OUT1}, DC_{OUT2}	: DC FEEDBACK CONTROL OUT		

BLOCK DIAGRAM

CONTENTS

1. PIN FUNCTIONS

Number	Pin Name	I/O	Function
1-10	NC	–	Leave this pin open.
11	AV$_{DD}$	–	+5 V power supply (analog)
12	DV$_{DD1}$	–	+5 V power supply (digital)
13	DV$_{DD2}$	–	+5 V power supply (digital)
14	$\overline{\text{AUX/MODE}}$	I	External signaling input
15	$\overline{\text{BSY}}$	O	BUSY LED driver output
16	$\overline{\text{SUS}}$	O	SUS LED driver output
17	$\overline{\text{RST}}$	I	Pin for reset input and power-on reset H: HW$_X$ valid, L: HW$_X$ output's internal F/F clear status
18	$\overline{\text{EXS}}$	O	SIPO sync signal output for expansion port Note 1
19	EXD	O	SIPO serial data output for expansion port Note 1
20	HW$_R$	I	Reception highway input [PCM data (8-bit) + CTL data (8-bit)]
21	DCLK	I	Clock input (2.048 MHz)

22	FS	I	8-kHz sync input Rising: HW$_R$ PCM data input start
			                      Rising: HW$_X$ PCM data output start
			                      Falling: HW$_R$ CTL data input start
			                      Falling: HW$_X$ SCN data output start

23	HW$_X$	O	Transmission highway output [PCM data (8-bit) + SCN data (8-bit)]
24	TYPE	O	HW$_X$ data enable
25	RT$_{IN1}$	I	Ring-Trip signal input 2
26	RT$_{IN0}$	I	Ring-Trip signal input 1
27	RC$_3$	O	Relay control for network testing [to the μPC7073's pin 22]
28	RC$_2$	O	Relay control for line testing [to the μPC7073's pin 21]
29	RC$_1$	O	Relay control for ringer transmit [to the μPC7073's pin 20]
30	BCUT	O	High and wet control output [to the μPC7073's pin 19]
31	ALM	O	Control output for ground-fault/power line contact protection mode [to the μPC7073's pin 18]
32	$\overline{\text{PD}}$	O	Power-down control output [to the μPC7073's pin 17]
33	DGND2	–	Digital ground 2 Note 2
34	DGND1	–	Digital ground 1 Note 2
35	SUB	–	Substrate ground Note 2
36	AGND	–	Analog ground Note 2
37	ACOM$_{IN}$	I	Signal ground input Note 3 [to the μPC7073's pin 11]
38	ACOM$_{OUT}$	O	Signal ground output Note 3 [to the μPC7073's pin 11]
39	A$_{OUT}$	O	Analog signal output for receive side [to the μPC7073's pin 10]
40	A$_{IN}$	I	Analog signal input for transmit side [to the μPC7073's pin 9]
41	AGDT	I	Tip-Ring sum current detection input [to the μPC7073's pin 8]
42	ASCN	I	Tip-Ring difference current detection input [to the μPC7073's pin 7]
43	BB$_{IN}$	I	V$_{BB}$ voltage information input [to the μPC7073's pin 6]

Notes 1. SIPO: Serial In Parallel Out

      2. Short AGND, DGND1, DGND2, and SUB directly under the IC and connect them to an analog ground.

      3. Short ACOM$_{IN}$ and ACOM$_{OUT}$ directly under the IC.

Number	Pin Name	I/O	Function	
44	DC$_{OUT2}$	O	DC feedback bias voltage output	[to the μPC7073's pin 5]
45	DC$_{OUT1}$	O	DC feedback control output	[to the μPC7073's pin 4]
46	DC$_{IN1}$	I	DC feedback control input 1	[to the μPC7073's pin 3]
47	DC$_{IN2}$	I	DC feedback control input 2	[to the μPC7073's pin 2]
48	DC$_{IN3}$	I	DC feedback control input 3	[to the μPC7073's pin 1]

2. USE CAUTIONS

(1) Combined characteristics of the μPC9903 and μPD7073

- The μPD9903 is designed to be used in combination with the μPC7073. Therefore, the first half of the electrical specifications described below are ratings for the μPD9903 as a discrete unit while the second half are combined ratings with the μPC7073.

- Subscriber circuit constants that are determined by factors such as termination impedance are configured to enable setting by external order parameters. Consequently, input of an order that is not suitable for the target impedance may result in failure to obtain the required characteristics.

(2) Absolute maximum ratings
Application of voltage or current in excess of the absolute maximum ratings may result in damage. Be especially cautious about surges, etc.

(3) Load of by-pass capacitor
Because the μPC7073 and μPD9903 use several internal high-frequency operational amplifiers, high power supply impedance can cause instability in these internal operational amplifiers (such as oscillation). To suppress such instability and eliminate power supply noise, connect by-pass capacitors (C_{ACOM} = approximate 0.1 μF) having superior high frequency characteristics as close as possible to the μPC7073's power supply pins (V_{BB} and V_{CC}) and the μPD9903's power supply pins (AV_{DD} and DV_{DD}).

(4) Addition of ACOM pin connection capacitor
The voltage of the ACOM pin between the μPC7073 and μPD9903 is the reference voltage of the signal source between the μPC9903 and μPC7073. Superposing of noise on this pin may have adverse effects on transmission characteristics. Therefore, make the wires between the ACOM pins of the two LSIs as short as possible, and connect capacitors (C_{ACOM} = approximate 0.1 μF) having superior high frequency characteristics as close as possible to the pins.

3. ELECTRICAL SPECIFICATIONS

3.1 Discrete unit Ratings

Absolute maximum ratings (T$_A$ = +25 $^\circ$C)

Parameter	Symbol	Conditions	Rating	Units
Power supply voltage	V$_{DD}$	AV$_{DD}$, DV$_{DD1}$, DV$_{DD2}$	−0.3 to +7.0	V
Analog input voltage	V$_{AIN}$	A$_{IN}$, ASCN, AGDT, ACOM$_{IN}$, BB$_{IN}$, DC$_{IN1}$, DC$_{IN2}$, and DC$_{IN3}$ pins	−0.3 to V$_{DD}$ + 0.3	
Digital input voltage	V$_{DIN}$	HW$_R$, DCLK, FS, RST, $\overline{AUX}$/$\overline{MODE}$, RT$_{IN0}$, and RT$_{IN1}$ pins	−0.3 to V$_{DD}$ + 0.3	
Applied voltage to analog output pin	V$_{AOUT}$	A$_{OUT}$, DC$_{OUT1}$, DC$_{OUT2}$, and ACOM$_{OUT}$ pins	−0.3 to V$_{DD}$ + 0.3	
Applied voltage to digital output pin	V$_{DOUT}$	HW$_X$, $\overline{BSY}$, $\overline{SUS}$, RC$_1$, RC$_2$, RC$_3$, $\overline{EXS}$, EXD, BCUT, ALM, $\overline{PD}$, and TYPE pins	−0.3 to V$_{DD}$ + 0.3	
Power dissipation	P$_T$		500	mW
Ambient operating temperature	T$_A$		0 to +70	$^\circ$C
Storage temperature	T$_{stg}$		−65 to +150	

Caution If the absolute maximum rating for any of the above parameters is exceeded even momentarily, it may adversely affect the quality of this product. In other words, these absolute maximum ratings have been set to prevent physical damage to the product. Do not use the product in such a way as to exceed any of these ratings.

Recommended operating conditions (T$_A$ = 0 to 70 $^\circ$C, V$_{DD}$ = 5 V $\pm$ 5 %, GND = 0 V)

(1) DC conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Ambient operating temperature	T$_A$		0	25	70	$^\circ$C
Power supply voltage	V$_{DD}$		4.75	5.0	5.25	V
Analog input voltage	V$_{AI}$	ASCN, and AGDT pins	0		V$_{DD}$	
Analog input driving resistance	R$_{LA1}$	ASCN, and AGDT pins			20	kΩ
Analog output load resistance	R$_{LOAD}$	A$_{OUT}$ pin	100			
Analog output load capacitance	C$_{LOAD}$				100	pF
Low level input voltage	V$_{IL1}$	FS, DCLK, HW$_R$, and $\overline{AUX}$/$\overline{MODE}$ pins	0		0.8	V
	V$_{IL2}$	$\overline{RST}$, RT$_{IN0}$, and RT$_{IN1}$ pins	0		0.2 $\times$ V$_{DD}$	
High level input voltage	V$_{IH1}$	FS, DCLK, HW$_R$, and $\overline{AUX}$/$\overline{MODE}$ pins	2.0		V$_{DD}$	
	V$_{IH2}$	$\overline{RST}$, RT$_{IN0}$, and RT$_{IN1}$ pins	0.8 $\times$ V$_{DD}$		V$_{DD}$	

(2) AC conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Data clock frequency	f_{DCLK}	(= 1/t_{CY}) ± 50 ppm		2048		kHz
Data clock pulse width	t_{DCLK}		200			ns
Frame sync clock frequency	f_S	± 50 ppm		8.0		kHz
High level frame sync pulse width	t_{WHS}		$t_{CY} \times 8$			ns
Low level frame sync pulse width	t_{WLS}		$t_{CY} \times 8$			ns
Clock rise time	t_R				30	ns
Clock fall time	t_F				30	ns
Float in sync timing	t_{CSD1}				100	ns
	t_{CSD2}		40			ns
High level width of frame sync clock and data clock	t_{WHSC}		100			ns
HW$_R$ set-up time	t_{DSR}	**Note 1**	65			ns
HW$_R$ hold time	t_{DHR}	**Note 1**	120			ns
Minimum width of reset pulse	PW$_{RST}$	$\overline{RST}$ pin **Note 2**	10			μs

Notes 1. During timing measurement, use 5 ns as the rise time and fall time for the digital input wave form and clock signal.

2. The μPD9903 is initialized when high level input is applied to the $\overline{RST}$ pin after applying low level input for several clock widths. (However, use of the $\overline{RST}$ pin is not guaranteed during low level input. Also, low level input alone does not initialize the μPD9903.)

DC Characteristics (T$_A$ = 0 to 70 °C, V$_{DD}$ = 5 V $\pm$ 0.25 V, V$_{DG}$ = V$_{AG}$ = 0 V, f$_{DCLK}$ = 2048 kHz, all output pins are unloaded)

(1) Current consumption

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Circuit current	I$_{DD}$	During normal mode		15	21	mA
Power-down circuit current	I$_{DDPD}$	During power-down mode		46	6	

(2) Digital interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Digital input current	I$_{ID}$	0 $\leq$ V$_{DIN}$ $\leq$ V$_{DD}$ for FS, DCLK, $\overline{\text{HW}_R}$, RT$_{IN0}$, RT$_{IN1}$, and $\overline{\text{RST}}$ pins	−10		+10	μA
Digital input pull-up current	I$_{IL}$	V$_{DIN}$ = 0 V for $\overline{\text{AUX}}/\overline{\text{MODE}}$ pin	−50	−7	−0.5	
3-state leakage current	I$_L$	0 $\leq$ V$_{DIN}$ $\leq$ V$_{DD}$ for HW$_X$ pin	−10		+10	
Low level output voltage	V$_{OL1}$	I$_{OL}$ = 3.4 mA for HW$_X$ pin			0.4	V
	V$_{OL2}$	I$_{OL}$ = 0.2 mA for RC$_1$, RC$_2$, RC$_3$, BCUT, ALM, $\overline{\text{PD}}$, $\overline{\text{EXS}}$, and EXD pins			0.4	
	V$_{OL3}$	I$_{OL}$ = 5 mA for $\overline{\text{BSY}}$ and $\overline{\text{SUS}}$ pins			1.1	
High level output voltage	V$_{OH1}$	I$_{OH}$ = −0.6 mA for HW$_X$ and TYPE pins	2.4			
	V$_{OH2}$	I$_{OH}$ = −2.0 mA for RC$_1$, RC$_2$, RC$_3$, BCUT, ALM, $\overline{\text{PD}}$, $\overline{\text{EXS}}$, and EXD pins	2.4			
	V$_{OH3}$	I$_{OH}$ = 0 mA for $\overline{\text{BSY}}$ and $\overline{\text{SUS}}$ pins	V$_{DD}$ − 0.5			
Output capacitance of digital output pin	C$_{OD}$	f = 1 MHz, unmeasured pins returned to 0 V			15	pF
Input capacitance of digital input pin	C$_{ID}$	f = 1 MHz, unmeasured pins returned to 0 V			10	

(3) A$_{IN}$ pin

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Input bias current	I$_B$	Input voltage:	−10		+10	μA
Input resistance	R$_{IN}$		1			MΩ
Input capacitance	C$_{IN}$				10	pF

(4) A$_{OUT}$ pin

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Output offset voltage	V$_{OA}$	$\overline{\text{HW}_R}$ PCM data: zero PCM code, referenced to V$_{ACOM}$	−100		+100	mV
Output resistance	R$_{OUT}$	I/O current: −100 to +100 μA			50	Ω

(5) ASCN and AGDT output pins

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Input bias current	I_B	Input voltage: 0 to V_{DD}	−10		+10	μA
Input resistance	R_{IN}		1			MΩ

(6) ACOM$_{OUT}$ pin

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Output voltage	V_{ACOM}	I/O current: −0.1 to +0.1 mA	2380		2420	mV

AC characteristics (T$_A$ = 0 to 70 °C, V$_{DD}$ = 5 V $\pm$ 0.25 V, V$_{DG}$ = V$_{AG}$ = 0, f$_{DCLK}$ = 2048 kHz)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Data enable delay time	t$_{DZX1}$	HW$_X$ and TYPE pins, when FS is delayed longer than DCLK			170	ns
	t$_{DZX2}$	HW$_X$ and TYPE pins, when DCLK is delayed longer than FS			170	ns
Data delay time	t$_{DDX}$	HW$_X$ pin			180	ns
Data hold time	t$_{HZX}$	HW$_X$ and TYPE pins	30		200	ns
Delay time to $\overline{\text{EXS}}$ falling edge	t$_{DEXSf}$	$\overline{\text{EXS}}$ pin			120	ns
Delay time to $\overline{\text{EXS}}$ rising edge	t$_{DEXSr}$	$\overline{\text{EXS}}$ pin			120	ns
EXD data delay time	t$_{DEXD}$	EXD pin			120	ns
Signaling bit set-up delay time	t$_{DSIG}$				2	μs
Status bit set-up delay time	t$_{DST}$				2	μs
LED driver set-up delay time	t$_{DLED}$	$\overline{\text{BSY}}$ and $\overline{\text{SUS}}$ pins			2	μs
Delay time to rising edge	t$_{THL}$				100	ns
Delay time to falling edge	t$_{TLH}$				100	ns
Transmit delay time to external bit	t$_{DAUX}$	$\overline{\text{AUX}}$ pin			125	μs

Timing charts

(1) PCM data transmission timing (HWx pin)

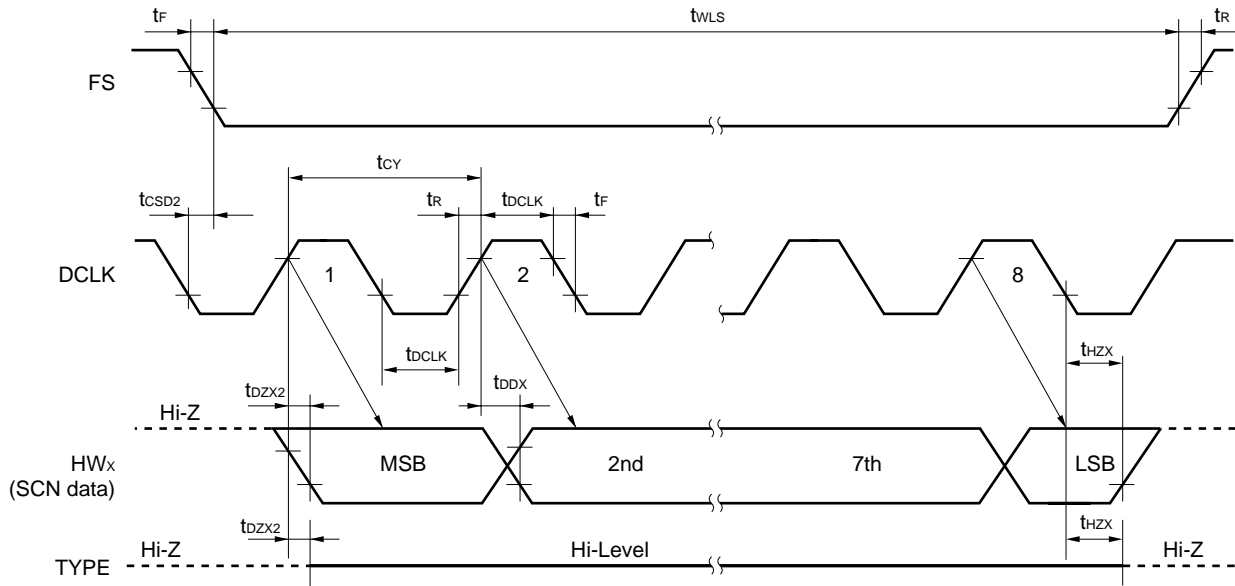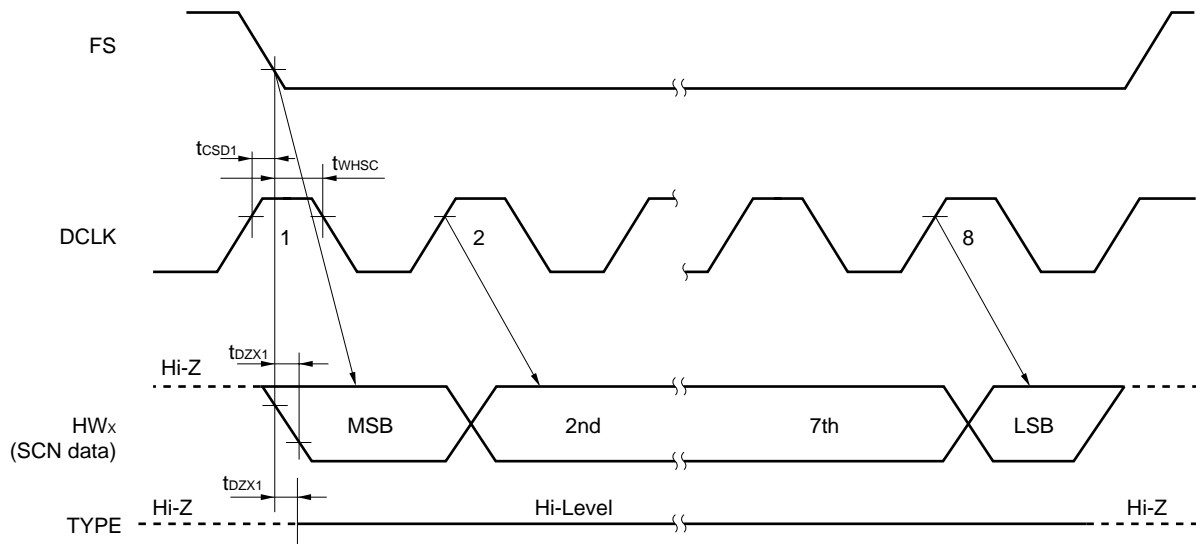**(a) DCLK is later than FS**
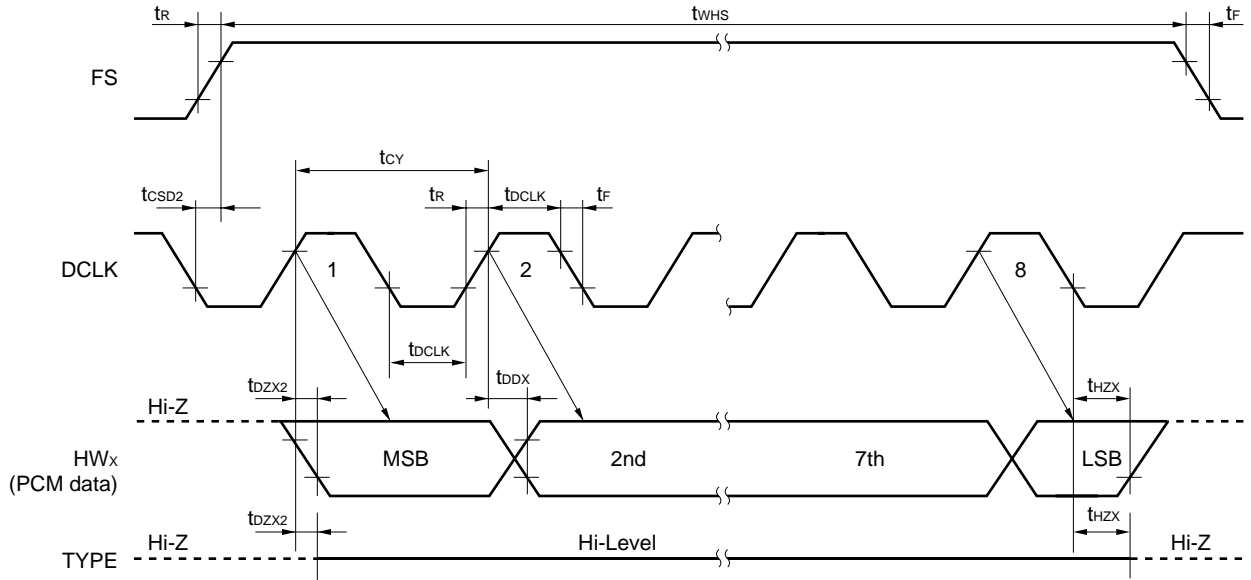
(b) FS is later than DCLK
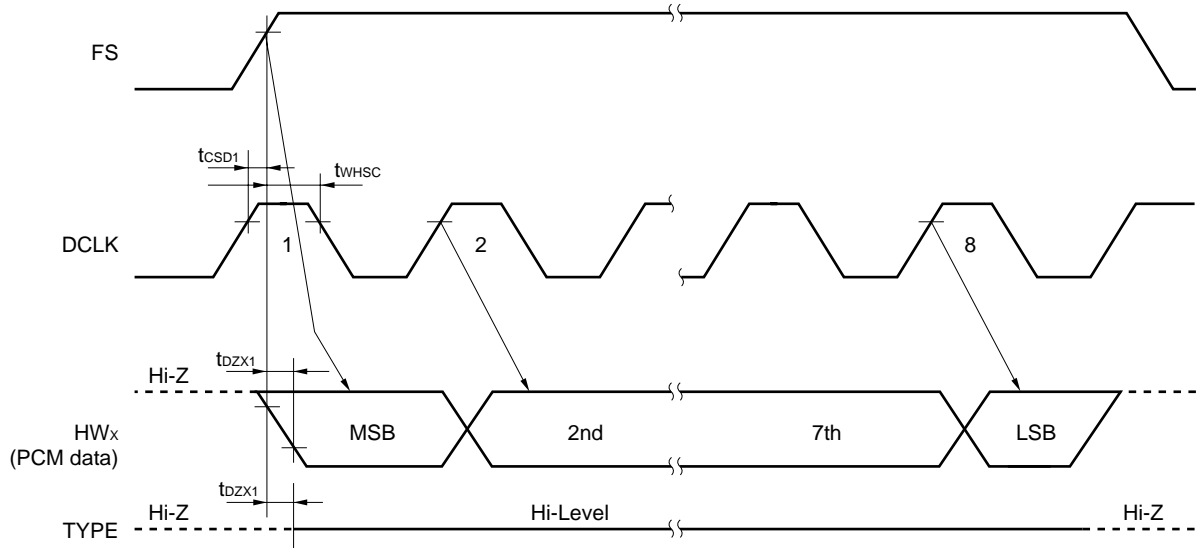
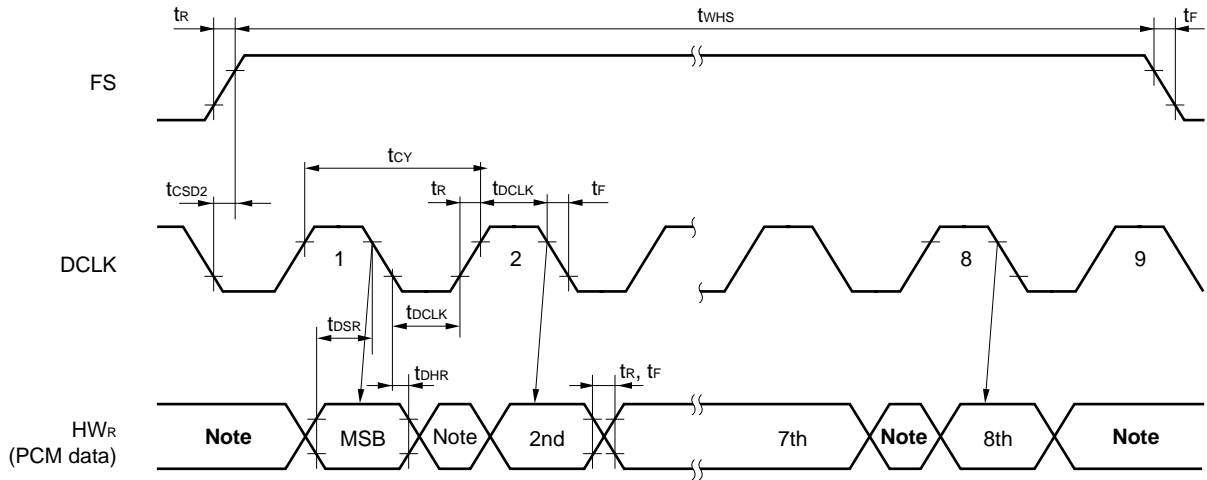**(2) SCN data transmission timing (HWx pin)**

(a) DCLK is later than FS
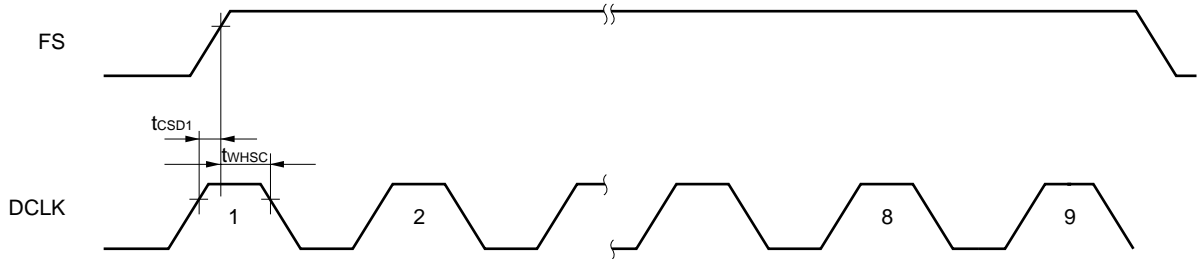

(b) FS is later than DCLK

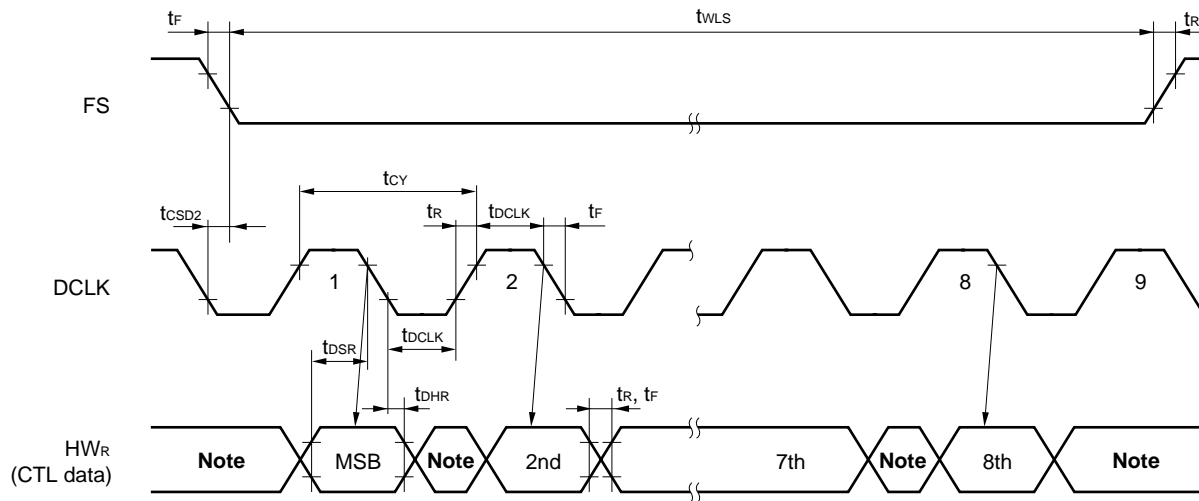**(3) PCM data reception timing (HW$_R$ pin)**

(a) DCLK is later than FS
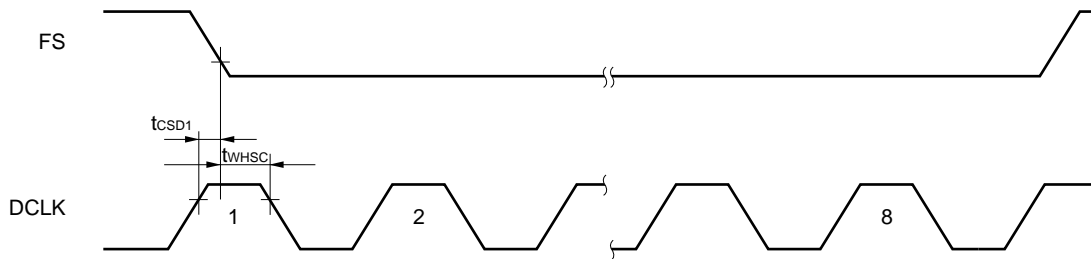

Note Don't care

(b) FS is later than DCLK

(4) CTL data reception timing (HWR pin)

(a) DCLK is later than FS

Note Don't care

(b) FS is later than DCLK

3.2 Combined Specifications with the μPC7073

DC characteristics

μ**PC7073 (V_{BB} = −42 to −58 V, V_{CC} = 5 V $\pm$ 0.25 V, T_A = 0 to 70 °C, 18 $\leq$ I_L $\leq$ I_{LMAX} (mA))**

μ**PD9903 (T_A = 0 to 70 °C, V_{DD} = 5 V $\pm$ 0.25 V, V_{DG} = V_{AG} = 0 V, f_{DCLK} = 2048 kHz)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Units
DC feed resistance	R_{BF}	200 Ω feed		180	200	220	Ω
		400 Ω feed		360	400	440	
Minimum loop current	I_{LMIN}	V_{BB} = −51 V	200 Ω feed	21.7	22.2	22.6	mA
		R_L = 1900 Ω	400 Ω feed	18.2	18.8	19.3	
Maximum current setting value	I_{LMAX}	I_{LMAX} = 76 mA setting	200 Ω feed	70	76	82	mA
			400 Ω feed	50	55	60	
		I_{LMAX} = 45 mA setting		40	45	50	
		I_{LMAX} = 35 mA setting		31	35	39	
Pin voltage during on-hook	V_{TS}	Normal on-hook, between Tip and GND, V_{BB} = −48 V		2.25	2.55	2.85	V
	V_{RS}	Normal on-hook, between Ring and V_{BB}, V_{BB} = −48 V		3.05	3.35	3.65	
	V_{TS}	On-hook transmission, between Tip and GND, V_{BB} = −48 V		2.25	2.55	2.85	
	V_{RS}	On-hook transmission, between Ring and V_{BB}, V_{BB} = −48 V		3.05	3.35	3.65	
Voltage between lines during on-hook	V_{TS}	V_{BB} = −48 V		V_{BB} − 7.0	V_{BB} − 5.9	V_{BB} − 5.0	V
Supervisory control – V_{BB} abnormal voltage	V_{BBF}			32	35	38	V

Parameter[Note]	Symbol	Conditions		MIN.	TYP.	MAX.	Units
Loop detection operating resistance (during normal transmission)	R_{ON1}	Includes termination resistance	200 Ω feed 400 Ω feed			2500 2100	Ω
Loop detection non-operating resistance (during normal transmission)			200 Ω feed 400 Ω feed	3900 3500			
Loop detection operating resistance (during on hook transmission)	R_{ON2}	Includes termination resistance	200 Ω feed 400 Ω feed			1900 1500	Ω
Loop detection non-operating resistance (during on hook transmission)			200 Ω feed 400 Ω feed	2840 2440			
Loop release non-operating resistance	R_{ON3}	Includes termination resistance	200 Ω feed 400 Ω feed			2960 2560	Ω
Loop release operating resistance			200 Ω feed 400 Ω feed	4540 4140			
Ground detection 1 (C/O) operating resistance	R_{ON4}	Includes termination resistance				5.2	kΩ
Ground detection 1 (C/O) non-operating resistance				20			
Ground-fault/power line contact detection operating resistance	R_{ON6}	Includes termination resistance Off-hook state	I_{LMAX} = 45/76 mA			340	Ω
			I_{LMAX} = 35 mA			480	
Ground-fault/power line contact detection non-operating resistance		Includes termination resistance	I_{LMAX} = 45/76 mA	870			Ω
			I_{LMAX} = 35 mA	1130			
Ground-fault/power line contact release non-operating resistance	R_{ON7}	Includes termination resistance				1.4	kΩ
Ground-fault/power line contact release operating resistance				10			

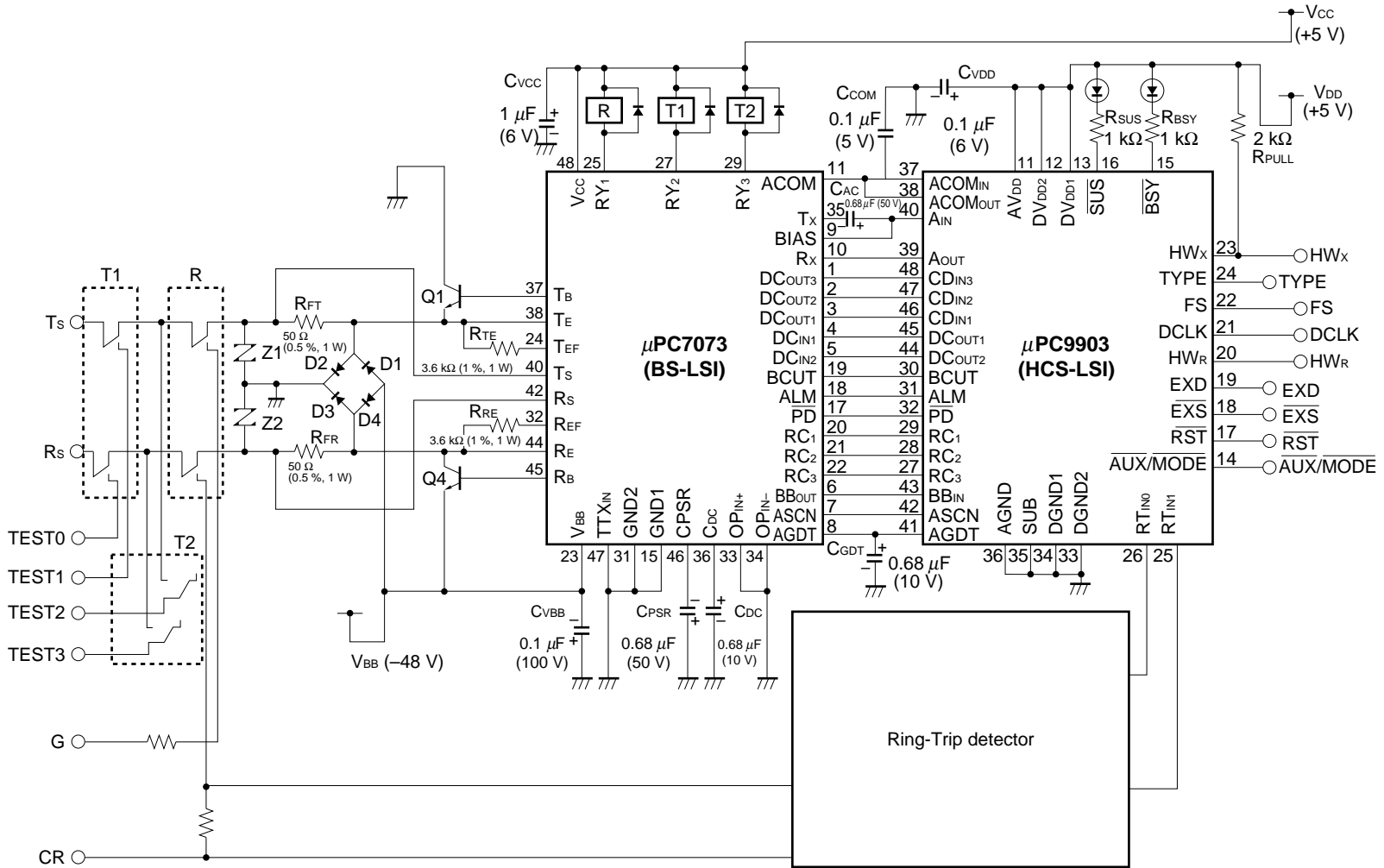**Note** The above values are resistance-converted values.

Transmission characteristics

μ**PC7073 (V_{BB} = –42 to –58 V, V_{CC} = 5 V $\pm$ 0.25 V, T_A = 0 to 70 °C, 18 $\leq$ I_L $\leq$ I_{LMAX} (mA))**

μ**PD9903 (T_A = 0 to 70 °C, V_{DD} = 5 V $\pm$ 0.25 V, V_{DG}= V_{AG} = 0 V, f_{DCLK} = 2048 kHz)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Units
Insertion loss	IL	A-D input signal 0 dBm0 1 kHz		–0.45	0.0	+0.45	dB
		D-A input signal 0 dBm0 1 kHz		–0.45	0.0	+0.45	
Transfer loss frequency characteristics	F_{RX}	A-D Reference input signal 1015 Hz 0 dBm0	60 Hz 200 Hz 300 Hz 400 to 3000 Hz 3200 Hz 3400 Hz	24.0 0.6 –0.15 –0.15 –0.15 0.2		– 2.0 +0.21 +0.15 +0.65 0.8	dB
	F_{RR}	D-A Reference input signal 1015 Hz 0 dBm0	60 Hz 200 Hz 300 Hz 400 to 3000 Hz 3200 Hz 3400 Hz	0.2 0.1 –0.15 –0.15 –0.15 0.2		4.0 1.0 +0.25 +0.15 +0.65 0.8	
Gain tracking (tone method)	GT_X	A-D Reference input signal –10 dBm0 f = 700 to 1100 Hz	+3 to –40 dBm0 –50 dBm0 –55 dBm0	–0.2 –0.5 –1.0		+0.2 +0.5 +1.0	dB
	GT_R	D-A Reference input signal –10 dBm0 f = 700 to 1100 Hz	+3 to –40 dBm0 –50 dBm0 –55 dBm0	–0.2 –0.4 –0.8		+0.2 +0.4 +0.8	
Return loss	RL	Input signal 0 dBm0 Z_T = 600 Ω + 2.16 μF	300 Hz 500 to 2000 Hz 2000 to 3400 Hz	16 20 16			dB
Echo attenuation	TBRL	Input signal 0 dBm0 Z_T = 600 Ω + 2.16 μF	300 Hz 500 to 2500 Hz 3400 Hz	18 22 18			dB
Transmit channel total power distortion factor (tone method)	SD_X	A-D Input signal f = 700 to 1100 Hz	+3 to –30 dBm0 –40 dBm0 –45 dBm0	36 30 25			dB
	SD_R	D-A Input signal f = 700 to 1100 Hz	+3 to –30 dBm0 –40 dBm0 –45 dBm0	36 30 25			

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Units
Absolute delay characteristics	D_A	A-A Input signal 0 dBm0					540	μs
Absolute delay distortion frequency characteristics	D_O	A-A	500 Hz 600 HZ 1000 to 2600 Hz 2800 Hz				1400 700 200 1400	

Intermodulation (2 Tone)	IMD	A-D Input signal
		  f1, f2: 300 to 3400 Hz
		        −4 to −21 dBm0
		  Measurement signal: 2 × f1 − f2
		  level (2 × f1 − f2) vs level (f1, f2)
					44.0			dB

		D-A Input signal
		  f1, f2: 300 to 3400 Hz
		        −4 to −21 dBm0
		  Measurement signal: 2 × f1 − f2
		  level (2 × f1 − f2) vs level (f1, f2)
					44.0			

Single frequency noise	N_{SF}	D-A
		  PAD level set at 0 dB
		  Measurement signal up to f = 256 kHz
							−54	dBm0

Deviation in gain setting for transmission channel	ΔDGS_X	A-D Difference from reference set value
		  Setting value: +7.5 to +3.0 dB
		                +3.0 to −3.5 dB
					−0.2
					−0.1
							+0.2
							+0.1
								dB

Deviation in gain setting for reception chanel	ΔDGS_R	D-A Difference from reference set value
		  Setting value: 0.0 to −5.0 dB
		                −5.0 to −8.5 dB
					−0.1
					−0.2
							+0.1
							+0.2	

Idle circuit noise	IDN_{24}	2W-4W	A-law	Psophometric weighted			−67	dBm0p
			μ-law	C message weighted			23	dBrnc0
	IDN_{42}	4W-2W	A-law	Psophometric weighted			−76	dBm0p
			μ-law	C message weighted			14	dBrnc0
Line to ground balance attenuation	LCL	$R_F = 50\ \Omega$ f = 300 to 600 Hz Relative accuracy = 0.5 % f = 600 to 3400 Hz			42 48			dB
AC induction noise resistance	LFI	$I_L = 0$ mA $V_{IN} = 6\ V_{rms}$					43	dBrnc
		$I_L = 20$ mA $V_{IN} = 15\ V_{rms}$					20	

V_{CC} (+5 V)

C_{VCC} 1 μF (6 V)

R   T1   T2

48 25   27   29

V_{CC} RY_1 RY_2 RY_3 ACOM

C_{COM} 0.1 μF (5 V)

C_{VDD} 0.1 μF (6 V)

V_{DD} (+5 V)

R_{SUS} 1 kΩ R_{BSY} 1 kΩ 2 kΩ R_{PULL}

11 37 $ACOM_{IN}$ AV_{DD} DV_{DD2} DV_{DD1} SUS $\overline{BSY}$
C_{AC} 38 $ACOM_{OUT}$
35 40 0.68 μF (50 V) A_{IN}
T_X 9
BIAS 10
R_X
       39 A_{OUT}
1   48 DC_{OUT3} CD_{IN3}
2   47 DC_{OUT2} CD_{IN2}
3   46 DC_{OUT1} CD_{IN1}
4   45 DC_{IN1} DC_{OUT1}
5   44 DC_{IN2} DC_{OUT2}
19 30 BCUT   BCUT
18 31 $\overline{ALM}$ $\overline{ALM}$
17 32 PD   PD
20 29 RC_1 RC_1
21 28 RC_2 RC_2
22 27 RC_3 RC_3
6   43 BB_{OUT} BB_{IN}
7   42 ASCN   ASCN
8   41 AGDT   AGDT

μPC7073 (BS-LSI)

μPC9903 (HCS-LSI)

13 16   15

HW_X 23 — HW_X
TYPE 24 — TYPE
FS 22 — FS
DCLK 21 — DCLK
HW_R 20 — HW_R
EXD 19 — EXD
$\overline{EXS}$ 18 — $\overline{EXS}$
$\overline{RST}$ 17 — $\overline{RST}$
$\overline{AUX}/\overline{MODE}$ 14 — $\overline{AUX}/\overline{MODE}$

T1   R

T_S

R_{FT} 50 Ω (0.5 %, 1 W)

Q1

Z1   D2   D1
Z2   D3   D4

R_{FR} 50 Ω (0.5 %, 1 W)

Q4

37 T_B
38 T_E
24 T_{EF} R_{TE} 3.6 kΩ (1 %, 1 W)
40 T_S
42 R_S
32 R_{EF} R_{RE} 3.6 kΩ (1 %, 1 W)
44 R_E
45 R_B

V_{BB} TTX_{IN} GND2 GND1 CPSR C_{DC} OP_{IN+} OP_{IN-} AGDT

AGND SUB DGND1 DGND2 RT_{IN0} RT_{IN1}

23 47 31 15 46 36 33 34

36 35 34 33   26 25

C_{GDT} 0.68 μF (10 V)

TEST0
TEST1   T2
TEST2
TEST3

V_{BB} (−48 V)

C_{VBB} 0.1 μF (100 V)

C_{PSR} 0.68 μF (50 V)

C_{DC} 0.68 μF (10 V)

G

Ring-Trip detector

CR

5. PACKAGE DRAWING

48 PIN PLASTIC SHRINK SOP (375 mil)

detail of lead end

$3°^{+7°}_{-3°}$
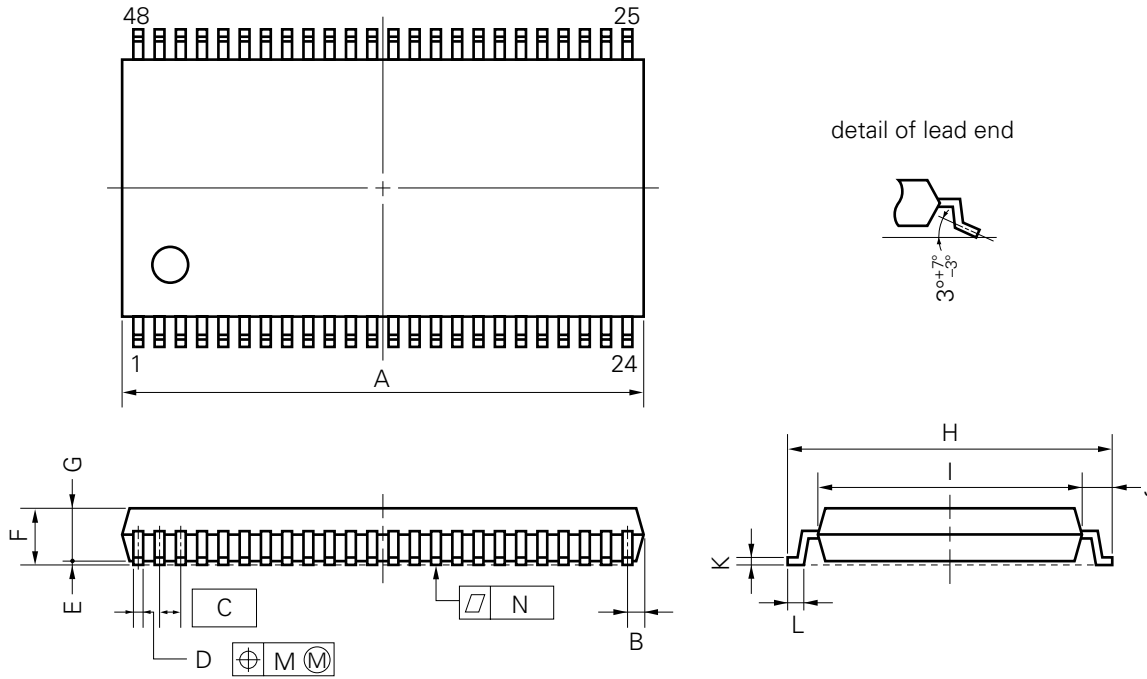
P48GT-65-375B-1

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.21 MAX.	0.639 MAX.
B	0.63 MAX.	0.025 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	0.30±0.10	$0.012^{+0.004}_{-0.005}$
E	0.125±0.075	0.005±0.003
F	2.0 MAX.	0.079 MAX.
G	1.7±0.1	0.067±0.004
H	10.0±0.3	$0.394^{+0.012}_{-0.013}$
I	8.0±0.2	0.315±0.008
J	1.0±0.2	$0.039^{+0.009}_{-0.008}$
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	0.10	0.004
N	0.10	0.004

6. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

SURFACE MOUNT TYPE

μ**PC9903GT: 48-pin plastic shrink SOP (375 mil)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared ray reflow	Package peak temperature: 235 ˚C Reflow time: 30 sec. max. (210 ˚C or above) Number of times: 1 time	IR35-00-1
Partial heating method	Pin temperature: 300 ˚C max. Heat time: 3 sec. max. (per each side of the device)	–

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

M4 96.5