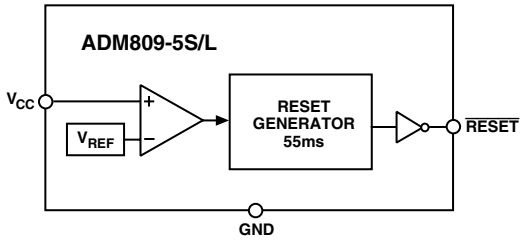
Microprocessor Supervisory Circuit

ADM809-5S/L

FEATURES
Specified Over Temperature
Low Power Consumption (17 μA)
Precision Voltage Monitor: 3 V, 5 V Options
Reset Assertion Down to 1 V V_{CC}
30 ms min Power-On Reset
Logic Low $\overline{\text{RESET}}$ Output

APPLICATIONS
Microprocessor Systems
Computers
Controllers
Intelligent Instruments
Automotive Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM809-5S/L supervisory circuits monitor the power supply voltage in microprocessor systems. It provides a reset output during power-up, power-down and brownout conditions. On power-up, an internal timer holds reset asserted for 55 ms. This holds the microprocessor in a reset state until conditions have stabilized. The $\overline{\text{RESET}}$ output remains operational with V_{CC} as low as 1 V. The ADM809-5S/L provides an active low reset signal ($\overline{\text{RESET}}$).

The reset comparator features built-in glitch immunity, making it immune to fast transients on V_{CC}.

The ADM809-5S/L consumes only 17 μA, making it suitable for low power portable equipment.

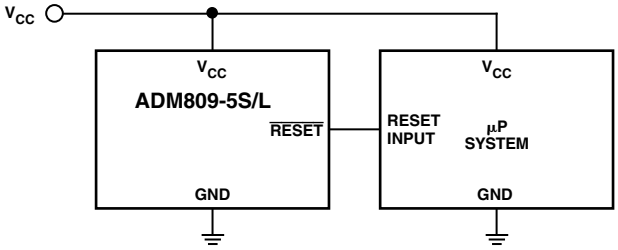


Figure 1. Typical Operating Circuit

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

ADM809-5S/L–SPECIFICATIONS (V_{CC} = Full Operating Range, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} typ = 5 V for L, 3.3 V for S Models unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
V_{CC} Operating Voltage Range	1.0	3.3	5.5	V	T_A = 0°C to +150°C with 100 kΩ Pull-Down on Output (Figure 3)
	1.2	3.3	5.5	V	T_A = –40°C to +150°C with 22 kΩ External Pull-Up on Output (Figure 6)
Supply Current		24	60	µA	V_{CC} < 5.5 V, ADM8_L, T_A = –40°C to +85°C
		17	50	µA	V_{CC} < 3.6 V, ADM8_S, T_A = –40°C to +85°C
			100	µA	V_{CC} < 5.5 V, ADM8_L, T_A = +85°C to +150°C
			100	µA	V_{CC} < 3.6 V, ADM8_S, T_A = +85°C to +150°C
RESET THRESHOLD					
Reset Voltage Threshold					
ADM809-5L	4.5		4.75	V	T_A = –40°C to +85°C
ADM809-5L	4.40		4.86	V	T_A = +85°C to +150°C
ADM809-5S	2.85		3.00	V	T_A = –40°C to +85°C
ADM809-5S	2.78		3.08	V	T_A = +85°C to +150°C
Reset Threshold Temperature Coefficient		30		ppm/°C	
V_{CC} to Reset Delay		20		µs	V_{CC} = V_{TH} to (V_{TH} –100 mV)
Reset Active Timeout Period	30	55	80	ms	T_A = –40°C to +150°C
$\overline{\text{RESET}}$ Output Voltage Low			0.3	V	V_{CC} = V_{TH} min, I_{SINK} = 1.2 mA, ADM809-5S
			0.4	V	V_{CC} = V_{TH} min, I_{SINK} = 3.2 mA, ADM809-5L
			0.3	V	V_{CC} >1.0 V, I_{SINK} = 50 µA, T_A = 0°C to +150°C
					V_{CC} >1.2 V, I_{SINK} = 50 µA, T_A = –40°C to +150°C
$\overline{\text{RESET}}$ Output Voltage High	0.8 V_{CC}			V	V_{CC} > V_{TH} max, I_{SOURCE} = 500 µA
	V_{CC} – 1.5			V	V_{CC} > V_{TH} max, I_{SOURCE} = 800 µA
JUNCTION TEMPERATURE	–40		+150	°C	

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{CC} . . . . . –0.3 V to +6 V
RESET, $\overline{\text{RESET}}$ . . . . . –0.3 V to V_{CC} + 0.5 V
Input Current
V_{CC} . . . . . 20 mA
Output Current
RESET, $\overline{\text{RESET}}$ . . . . . 20 mA
Rate of Rise, V_{CC} . . . . . 100 V/µs
Power Dissipation, RT-3 SOT-23
Derate by 4 mW/°C above 70°C . . . . . 320 mW
θ_{JA} Thermal Impedance . . . . . 333°C/W
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C
Storage Temperature Range . . . . . –65°C to +150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

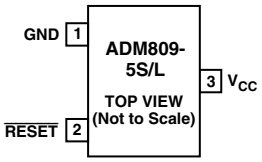
CAUTION

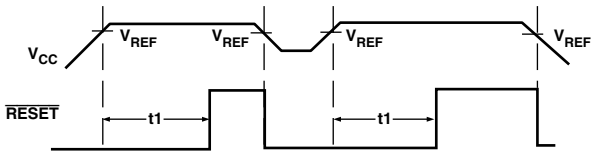
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM809-5S/L features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Function
1	GND	0 V. Ground reference for all signals.
2	$\overline{\text{RESET}}$	Active Low Logic Output. $\overline{\text{RESET}}$ remains low while V_{CC} is below the reset threshold, and remains low for 55 ms (typ) after V_{CC} rises above the reset threshold
3	V_{CC}	Supply voltage being monitored.

PIN CONFIGURATION





t1 = $\overline{\text{RESET}}$ TIME = 55ms TYP.
V_{REF} = $\overline{\text{RESET}}$ VOLTAGE THRESHOLD

Figure 2. Power Fail $\overline{\text{Reset}}$ Timing

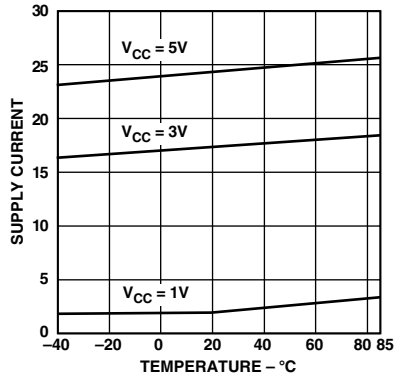
Table I. $\overline{\text{RESET}}$ Threshold Options

Model	$\overline{\text{RESET}}$ Threshold
ADM809-5LART	4.63 V
ADM809-5SART	2.93 V

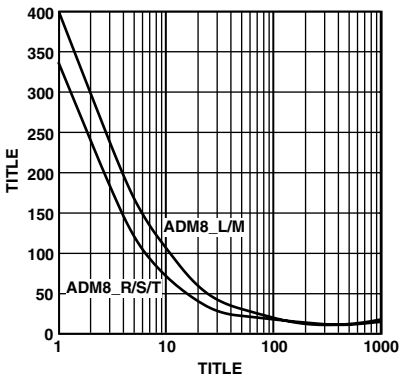
ORDERING GUIDE

Model	Reset Threshold	Temperature Range	Branding Information	Quantity
ADM809-5LART-REEL	4.63 V	–40°C to +150°C	M9L	10K
ADM809-5LART-REEL-7	4.63 V	–40°C to +150°C	M9L	3K
ADM809-5SART-REEL	2.93 V	–40°C to +150°C	M9S	10K
ADM809-5SART-REEL-7	2.93 V	–40°C to +150°C	M9S	3K
ADM809-5SCHIPS	2.93 V	–40°C to +150°C	NA	1 Wafer

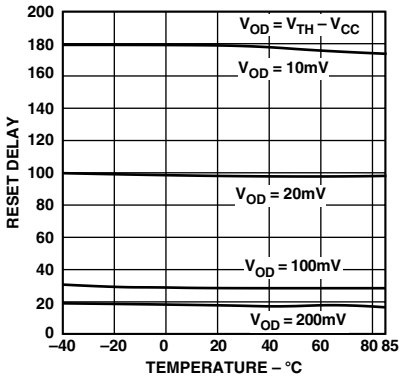
ADM809-5S/L –Typical Performance Characteristics



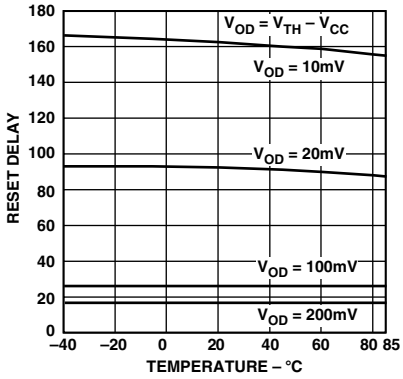
TPC 1. Supply Current vs. Temperature (No Load)



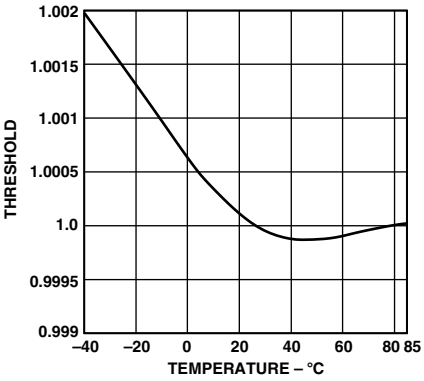
TPC 2. Maximum Transient Duration Without Causing a RESET Pulse vs. RESET Comparator Overdrive



TPC 3. Power-Down RESET Delay vs. Temperature ADM809-5L



TPC 4. Power-Down RESET Delay vs. Temperature ADM809-5S



TPC 5. Normalized RESET Voltage Threshold vs. Temperature

INTERFACING TO OTHER DEVICES OUTPUT

The ADM809-5S/L is designed to integrate with as many devices as possible and therefore has an output dependant on V_{CC}. Because of this design approach, interfacing this device to other devices is simplified.

ENSURING A VALID RESET OUTPUT DOWN TO V_{CC} = 0 V

When V_{CC} falls below 0.8 V, ADM809-5S/L's $\overline{RESET}$ no longer sinks current. A high impedance CMOS logic input connected to $\overline{RESET}$ may, therefore, drift to undetermined logic levels. To eliminate this problem a 100 kΩ resistor should be connected from $\overline{RESET}$ to ground.

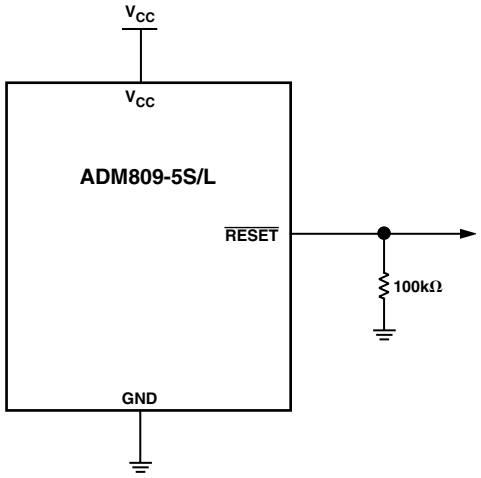


Figure 3. Ensuring a Valid $\overline{RESET}$ Output Down to V_{CC} = 0 V

THE BENEFITS OF A VERY ACCURATE $\overline{RESET}$ THRESHOLD

In other microprocessor supervisory circuits, tolerances in supply voltages lead to an overall increase in $\overline{RESET}$ tolerance levels due to the deterioration of the microprocessor $\overline{RESET}$ circuit's power supply. The possibility of a malfunction during a power failure is greatly reduced because the ADM809-5S/L series can operate effectively even when there are large degradations of the supply voltages. Another advantage of the ADM809-5S/L series is its very accurate internal voltage reference circuit. These benefits combine to produce an exceptionally reliable Voltage Monitor Circuit.

INTERFACING TO MICROPROCESSORS WITH MULTIPLE INTERRUPTS

In a number of cases it is necessary to interface many interrupts from different devices (i.e., thermal, attitude, and velocity sensors). The ADM809-5S/L can easily be integrated into existing interrupt-handling circuits (Figure 6) or used as a stand-alone device.

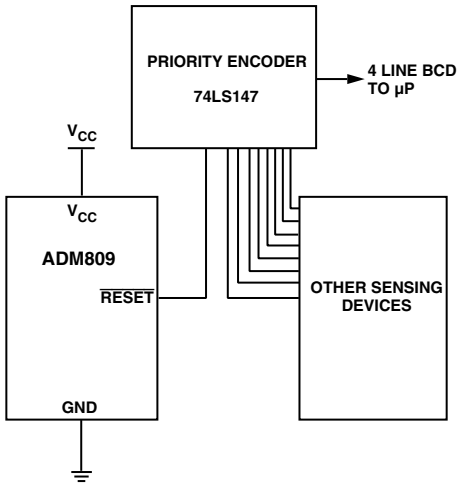


Figure 4. Interfacing to µPs with Multiple Interrupts

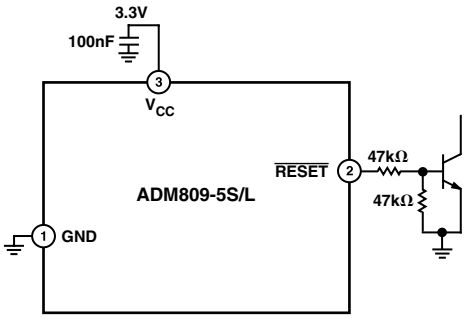


Figure 5. Alternative Application Circuit with Extra Decoupling

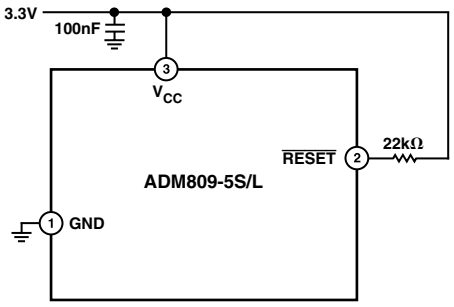
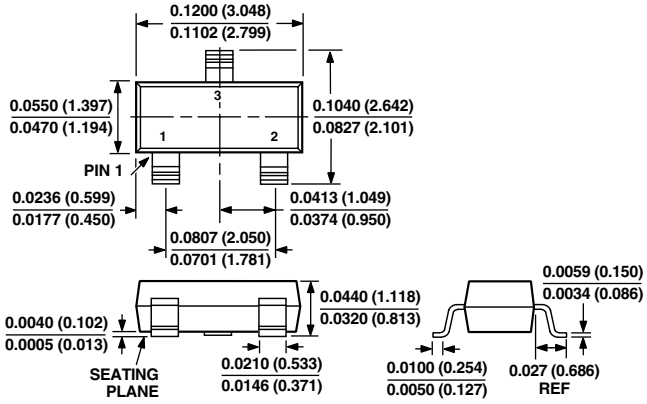


Figure 6. Additional Decoupling Can Be Achieved Using a 100 nF Capacitor Between V_{CC} and Ground

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Surface Mount Package
RT-3



C00090–2.5–9/00 (rev. 0)

PRINTED IN U.S.A.