Sync Detector

Monolithic IC MM1069

Outline

This IC is a sync detection circuit for obtaining the best reception state on VCR and TV channel selection systems. A system with high detection precision and no adjustment required can be configured due to the PLL format using a ceramic resonator. It can also be used in OSD circuits for blue-back switching and the like.

Features

- 1. Can be used in VCR and TV channel selection systems, and also for blue-back, etc.
- 2. High precision due to use of PPL format
- 3. Ceramic resonator means no adjustment required
- 4. Ceramic resonator can be selected for use in either PAL or NTSC
- 5. Power supply voltage Vcc=5V

Package

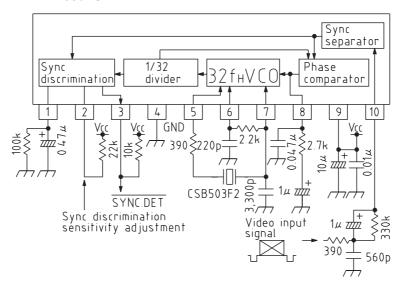
SIP-10A (MM1069XS)

Applications

- 1. TV
- 2. VCR
- 3. Other video equipment

Block Diagram

MM1069XS



Pin Description

1	CR	<u> </u>	Pin no.	VIDEO IN	,
		220 220			10k
2	GAIN	430	7	OSC IN1	220 12k
3	SYNC.DET		8	OSC IN2	10k 200
4	GND		9	LPF	
5	OSC OUT	6.8k	10	Vcc	10k

Absolute Maximum Ratings (Ta=25°C)

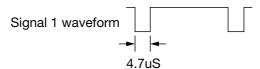
Item	Symbol	Ratings	Units
Storage temperature	Tstg	-40~+125	°C
Operating temperature	Topr	-20~+75	°C
Power supply voltage	Vcc max.	7	V
Allowable loss	Pd	500	mW

Electrical Characteristics

(Except where noted otherwise, Ta=25°C, Vcc=5.0V, X=CSB503F2, R=390 [OHM], C=3300pF, SW1=OFF)

Item	Symbol	Measurement circuit	Measurement conditions	Min.	Тур.	Max.	Units
Operating power supply voltage	Vcc	Vcc		4.7	5.0	5.3	V
Consumption current	Id	Id			7.5	11.0	mA
32fH VCO free-running frequency NTSC	fo1	TP3		497.1	503.5	509.9	kHz
Horizontal sync signal acquisition range NTSC	fcap	Vin	V _{IN} : signal 1 *1 *2	300	500		Hz
32fH VCO free-running frequency PAL	fo2	TP3	X=CSB500F40, R=200OHM, C=4700pF	493.6	500.0	506.4	kHz
Horizontal sync signal acquisition range PAL	fcap2	V _{IN}	X=CSB500F40, R=2000HM, C=4700pF, V _{IN} : signal 1 *1 *3	300	500		Hz
LPF pin DC level	VLPF	TP4	SW1 : ON	0.9	1.4	1.9	V
Sync separation level	VSEPA	V _{IN}	V _{IN} : staircase wave 1V _{P-P} *4	20	50	80	mV
Sync discrimination output voltage L	Vı.4	TP2	V _{IN} : staircase wave 1V _{P-P} *5		0.2	0.4	V
Sync discrimination output voltage H	Vн4	TP2	V _{IN} : no input signal ★5	4.8	5.0		V
Sync discrimination switching voltage L	VTHL4	TP1	TP1 : DC voltage 5V → Low ★5	2.0	2.3	2.6	V
Sync discrimination switching voltage H	Vтнн4	TP1	TP1 : DC voltage 0V → High *5	2.7	3.0	3.3	V

*1 Signal 1 : Pulse signal with 0.3V amplitude and pulse width 4.7µS



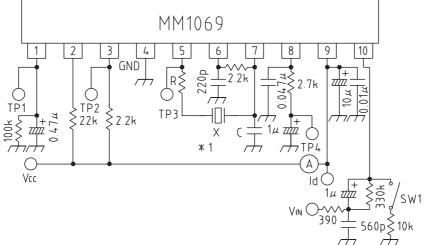
- *2 Measuring horizontal sync signal pull-in range for NTSC
 - Adjust signal 1 frequency toward 15.734kHz. The measurement value is the smaller of signal 1 frequency when TP2 level switches from high to low, and the difference from 15.734.
- *3 Measuring horizontal sync signal pull-in range for PAL

Adjust signal 1 frequency toward 15.625kHz. The measurement value is the smaller of signal 1 frequency when TP2 level switches from high to low, and the difference from 15.625.

- *4 Measuring sync separation level
 - Gradually lower staircase wave signal sync tip level, and measure sync tip level when TP2 level switches from low to high.
- *5 Sync discrimination switching voltage measurement

 Gradually change the voltage impressed on TP1, and measure TP5 voltage when TP2 output switches.

Measuring Circuit

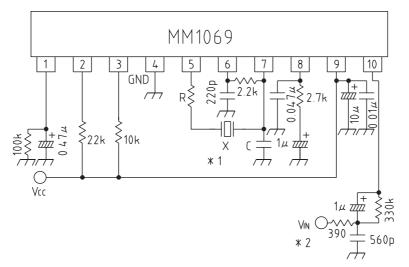


Note: *1

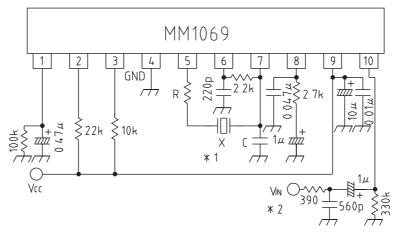
	NTSC	PAL
Х	CSB503F2	CSB500F40
R	390Ω	220Ω
С	3300pF	4700pF

Application Circuits

Application Circuit 1



■ Application Circuit 2



Note 1:1. *1

	NTSC	PAL
X	CSB503F2	CSB500F40
R	390Ω	220Ω
С	3300pF	4700pF

Note 2: *2

- 1. Input signal sync tip must be less than 1V for application circuit 1 Pin 10 external circuit.
- The above 1. does not apply for application circuit
 Pin 10 external circuit. Pin 10 is clamped at approximately 2.5V.