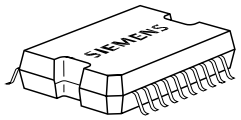
SIEMENS

Smart Quad Channel Low-Side Switch — TLE 5216 G

SPT-IC

Features

- Overload protection
- Short circuit protection
- Cascadeable serial diagnostic interface
- Overvoltage protection
- µC compatible input
- **E**lectro**s**tatic **d**ischarge (ESD) protection



P-DSO-20-10

	Type	Ordering Code	Package
▼	TLE 5216 G	Q67006-A9206	P-DSO-20-10

▼ New Type

Application

- All kinds of resistive and inductive loads (relays, electromagnetic valves)
- µC compatible power switch for 12 V applications
- Solenoid control switch in automotive and industrial control systems

General Description

Quad channel Low-Side Switch in Smart Power Technology (SPT) with four separate LOW active inputs and four open drain DMOS output stages. The TLE 5216G is protected by embedded protection functions and designed for automotive and industrial applications.

Product Summary

Parameter	Symbol	Values	Unit
Supply voltage	V_S	6 … 30	V
Drain source clamping voltage (OUT1 - OUT4)	$V_{DS(AZ)max}$	75	V
ON resistance	$R_{ON(typ)}$	0.35	Ω
Output current	I_D	4 × 2	A

Pin Configuration

(top view)

P-DSO-20-10

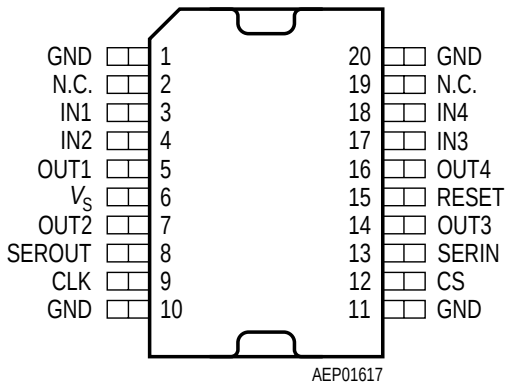


Figure 1

Pin Definitions and Functions

Pin No.	Symbol	Function
3	IN1	Input switch 1; active LOW; internal pull-up
4	IN2	Input switch 2; active LOW; internal pull-up
5	OUT1	Output switch 1; overload and shorted load protected
6	V_S	Supply voltage
7	OUT2	Output switch 2; overload and shorted load protected
8	SEROUT	Data-out of serial diagnostic interface; open drain
9	CLK	Clock for serial diagnostic interface
1, 10, 11, 20	GND	Ground
12	CS	Chip select for serial diagnostic interface; internal pull-up
13	SERIN	Data-in of serial diagnostic interface; internal pull-up
14	OUT3	Output switch 3; overload and shorted load protected
15	RESET	Reset; active LOW; shuts down all outputs and resets the error flags
16	OUT4	Output switch 4; overload and shorted load protected
17	IN3	Input switch 3; active LOW; internal pull-up
18	IN4	Input switch 4; active LOW; internal pull-up
2, 19	N.C.	Not connected

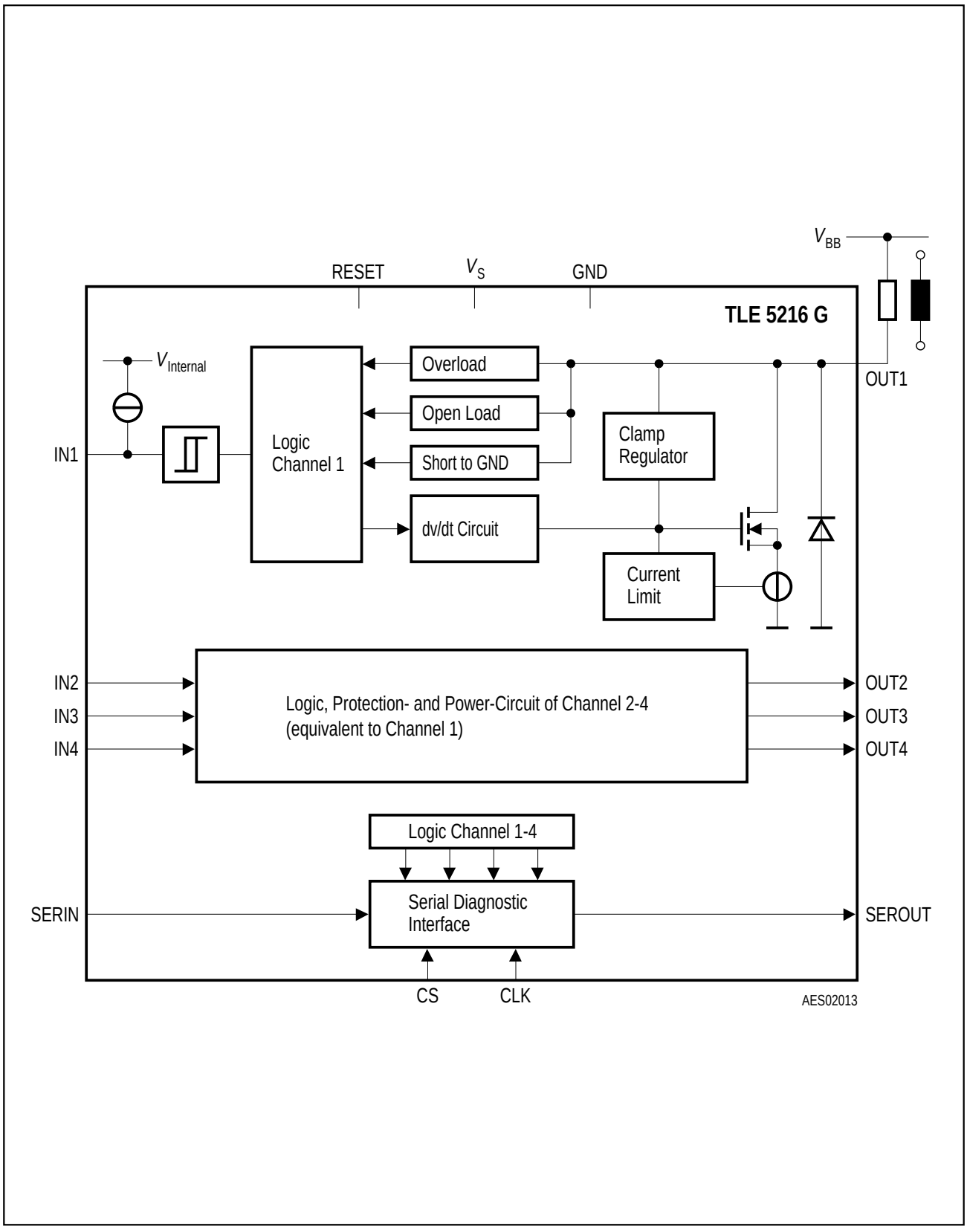


Figure 2
Block Diagram

Application Description

This IC is specially designed to drive inductive loads up to 2 A nominal current (valves, relays, etc.). Integrated clamp-diodes limit the output voltage when inductive loads are turned off.

For the detection of errors at the load there is a serial diagnostic interface, which monitors the following errors for every output separately:

– open load in inactive mode
– shorted output (shorted to ground) in inactive mode
– overload or shorted load in active mode

Circuit Description

The block diagram shows the four independent power drivers with the referring logic block and the serial diagnostic interface which stores and transfers the diagnostic signals to the external circuit. Each power switch connects a high side load to ground when a LOW signal applies at the inputs. To protect the IC against short circuit and over load each output is provided with a current limitation and a delayed overload shutdown. The slew rate of the switching process is limited internally.

The integrated clamp diodes limit the voltage at the output to $V_{DS(AZ)}$, when inductive loads are switched off. The maximum power dissipation, which is given from the static and dynamic thermal resistance, limits the allowable inductive energy. A diode in parallel to every output clamps negative voltage.

All outputs, preferably the outputs 1 and 2 and the outputs 3 and 4 may be used in parallel (no addition of max. freewheeling energy).

A curve of the output voltage is shown in **figure 6**.

The diagnostic block monitors the voltages across the power switch. If in active mode (LOW level input) there is a higher voltage than $V_{DS(OV)}$ for a time longer than $t_{VDS(OV)}$, the diagnostic block will show an overload in the error register and the affected power switch will be shut off. The switch can only be reactivated if the corresponding input is switched off and then on again.

In inactive mode (HIGH level at input) open load or shorted output (shorted load to ground) is detected and signalled to the serial diagnostic interface. If the voltage across the power switch is lower than $V_{DS(OL)}$ for the time $t_{VDS(OL)}$ (min. 50 µs) open load is identified. If the voltage is even lower than $V_{DS(SH)}$ for the time $t_{VDS(SH)}$ (min. 30 µs) "shorted to ground" is detected. An internal voltage divider will pull the output to the voltage V_{DS} if there is an open load.

A new error on the same output stage will over-write the old error report. The protocol of the serial diagnostic interface includes independent error reports for each output driver.

As soon as an error is latched into the error register the serial data output (SEROUT) of the interface will go LOW (while CS is still HIGH). If the chip select gets a LOW signal

(CS = L), all error reports can be shifted out serially. The rising edge of the CS will reset all error registers. The function of the serial diagnostic interface is shown in **figure 7**.

The data input (SERIN) allows several TLE 5216 G or other serial diagnostic interfaces to be cascaded.

A LOW signal on the reset pin (RESET) or a supply voltage lower than the operating range (4.5 V) will erase the error register and disable all four power switches.

Absolute Maximum Ratings

T_j = – 40 °C to 150 °C

Parameter	Symbol	Values	Unit
Supply voltage	V_S	– 2 … 40	V
Input voltages IN1 … IN4, SERIN, CLK, CS, RESET	V_{IN}	– 0.3 … 7	V
Status output voltage Data OUT (SEROUT)	V_{SEROUT}	– 0.3 … 10	V
Operating temperature range	T_j	– 40 … 150	°C
Storage temperature range	T_{Stg}	– 50 … 150	°C
Output current per channel T_j = 25 °C	$I_{D(AZ)}$	– 3.8 … 3.8	A
Output current per channel T_j = 125 °C	$I_{D(AZ)}$	– 2.95 … 2.95	A
Ground pin current T_j = 25 °C	I_{GND}	– 10 … 10	A
Ground pin current T_j = 125 °C	I_{GND}	– 8 … 8	A
Thermal resistance (junction-case static) See diagrams P-DSO-20-10	R_{thJC}	5	K/W
Transient thermal impendance t_p = 100 µs; square pulse	Z_{thJC}	0.5	K/W
Transient thermal impendance t_p = 100 µs; triangle pulse	Z_{thJC}	0.2	K/W

Note: Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Operating Range

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	6	30	V
Supply voltage outputs switchable; no diagnostic	V_S	4.5		V
Input LOW voltage V_S > 6 V	V_{INL}	– 0.3	1	V
Input HIGH voltage V_S > 6 V	V_{INH}	2	6	V
Clock input HIGH voltage V_S > 6 V	V_{CLKH}	2.4	6	V
Inverse current at output V_S > 6 V isolated cooling fin[1)]	I_D	– 0.3		A
Junction temperature	T_j	– 40	150	°C
Clock frequency V_S > 6 V	f_{CLK}	0	500	kHz
Clock pulse width V_S > 6 V	t_{CLKH}, t_{CLKL}	400		ns
CS pulse width V_S > 6 V	t_{CSH}, t_{CSL}	2		µs
Setup time CS to CLK V_S > 6 V	t_{CSC}	2		µs

[1)] If inverse current occurs at output 2 or 3, then provide external pull-up resistor 5.6 kΩ to + 5 V at input DIN.

Note: In the operating range the functions given in the circuit description are fulfilled.

Electrical Characteristics

V_S = 6 V to 18 V; T_j = – 40 °C to 150 °C (unless otherwise specified)

Parameter		Symbol	Limit Values			Unit
			min.	typ.	max.	
Power Supply (V_S)						
Supply current	Outputs ON	I_S		3.5	8	mA
	Outputs OFF	I_S		8	15	mA
Power Outputs						
ON state resistance						
T_j = 25 °C; I_D = 2 A; all V_{DS} > 0 V		$R_{DS(ON)}$		0.35	0.4	Ω
T_j = 125 °C; I_D = 1.5 A; t > 100 µs		$R_{DS(ON)}$		0.55	0.63	Ω
Clamping voltage (OUT1 - OUT4)						
I_D = 1 A; 0 < T_j < 125 °C; all V_{DS} > 0 V		$V_{DS(AZ)}$	65	70	75	V
Negative clamping voltage						
T_j = 25 °C; I_D = – 0.3 A		$V_{DS(AZ)}$	– 1		– 0.5	V
Current limitation	T_j = 0 °C; V_{DS} = $V_{DS\ (OV)}$	$I_{D(lim)}$	3.0	3.6	4.2	A
	T_j = 25 °C; V_{DS} = $V_{DS\ (OV)}$	$I_{D(lim)}$	2.8	3.3	3.8	A
	T_j = 125 °C; V_{DS} = $V_{DS\ (OV)}$	$I_{D(lim)}$	2.25	2.6	2.95	A
Leakage current						
V_S = 0 V; V_{DS} = 12 V; all V_{DS} > 0 V		I_R		0.2	0.5	mA
Digital Inputs						
Inputs IN1 … IN4, CS, SERIN						
Input LOW current	0 V < V_{IN} < 2 V	I_{INL}	– 200	– 100	– 50	µA
Input HIGH current	V_{IN} = 5 V	I_{INH}	– 20	0	5	µA
Input hysteresis		V_{INHys}	0.5	0.6		V
Input Clock (CLK)						
Input current	0 V < V_{INCLK} < 5 V	I_{INCLK}	– 20	2	5	µA
Input hysteresis		$V_{INCLKHys}$	0.5	0.7		V

Electrical Characteristics (cont'd)
V_S = 6 V to 18 V; T_j = – 40 °C to 150 °C (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Input Reset					
Input current 0 V < V_{INR} < 2 V	I_{INR}	– 25	– 10	– 5	µA
Input hysteresis	V_{INRHys}	0.5	0.6		V
Input Currents in Case of Inverse Current at Output ΣI_D **= – 0.3 A;** V_S **= 0 V; 0 V <** V_{IN} **< 5 V**					
Inputs CLK, SEROUT, CS, SERIN	I_{IN}			200	µA
Inputs IN1 … IN4	I_{IN}			100	µA
Input RESET	I_{IN}			25	µA
Timings					
Data valid SEROUT after CLK no 100 % testing	t_{DDA}	0	150	400	ns
Output ON delay R_L = 12 Ω	t_{DON}	0	1.4	10	µs
Output OFF delay R_L = 12 Ω	t_{DOFF}	0	2.4	10	µs
Difference of delays R_L = 12 Ω	$t_{DON} - t_{DOFF}$	– 3	– 1	3	µs
Output slew rate falling C_L = 1 nF; 10 V → 2 V	S_f	– 15	– 8	– 5	V/µs
Output slew rate rising I_D = 1 A; 5 V → 55 V	S_r	10	14	20	V/µs
Diagnostic Output (SEROUT)					
Output leakage current V_{SEROUT} = 5 V	$I_{SEROUTH}$	0		5	µA
Output LOW voltage 0 V < I_{SEROUT} < 1.6 mA	$V_{SEROUTL}$	0	0.2	0.5	V

Electrical Characteristics (cont'd)
V_S = 6 V to 18 V; T_j = – 40 °C to 150 °C (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Diagnostic Functions					
Overload threshold Output ON	$V_{DS(OV)}$	1.5	2	2.5	V
Overload delay V_S = 12 V; V_{BB} = 12 V	$t_{VDS(OV)}$	30	80	200	µs
Open load output voltage					
V_S = 6.5 V; outputs OFF	V_{DS}	3.3	3.8	4.3	V
V_S = 12.5 V	V_{DS}	6.7	7.7	8.7	V
Differential open load output resistance outputs OFF	R_D	5	15	40	kΩ
Open load threshold V_S = 6.5 V; outputs OFF	$V_{DS(OL)}$	4.3	4.7	5.2	V
V_S = 12.5 V	$V_{DS(OL)}$	9.3	10.2	11	V
Open load delay V_S = 12 V	$t_{VDS(OL)}$	50	130	250	µs
Shorted to ground threshold					
V_S = 6.5 V; outputs OFF	$V_{DS(SH)}$	2.4	2.8	3.3	V
V_S = 12.5 V	$V_{DS(SH)}$	4.5	5.4	6.3	V
Shorted to ground delay V_S = 12 V	$t_{VDS(SH)}$	30	80	200	µs

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Test Circuits

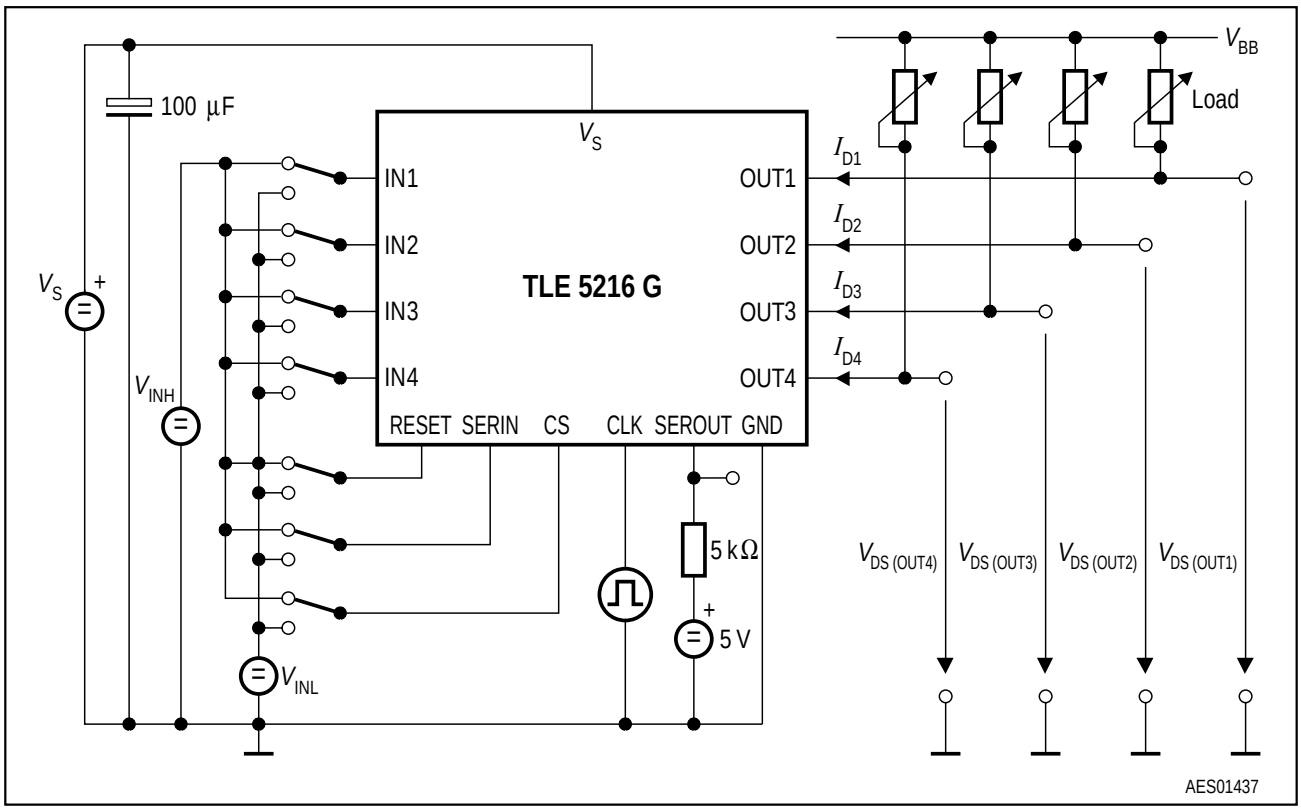


Figure 3
Test Circuit 1

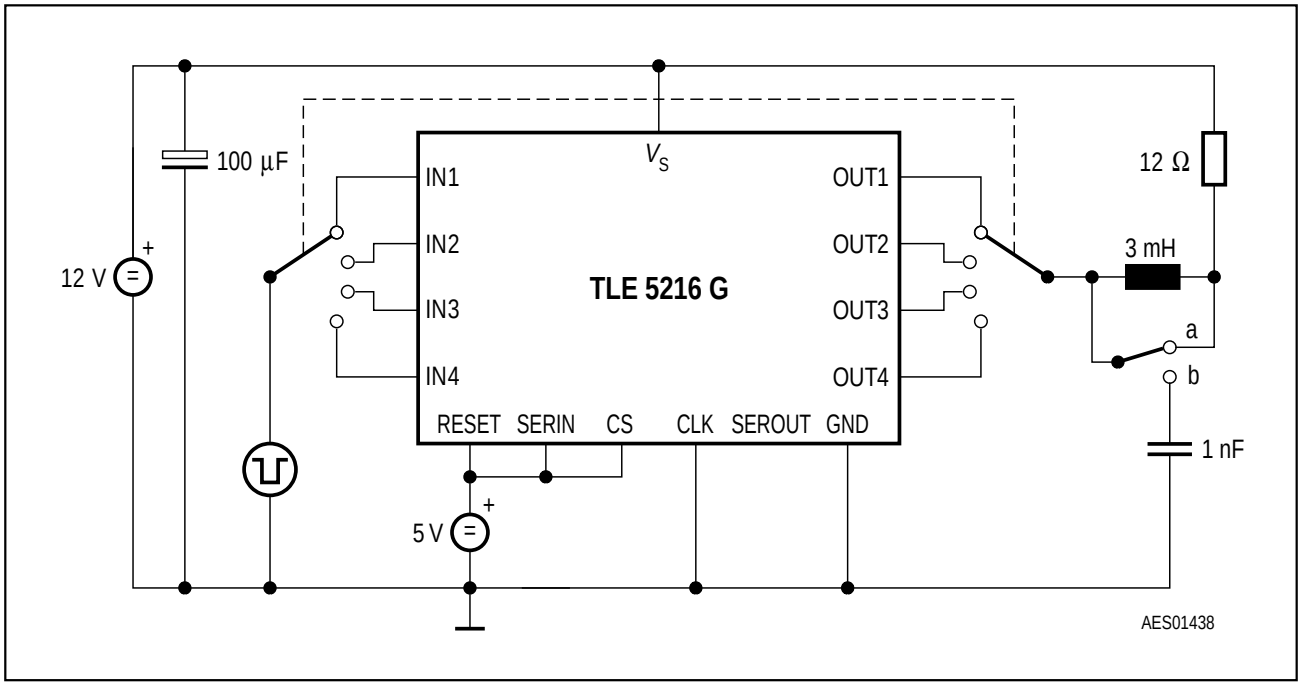


Figure 4
Test Circuit 2

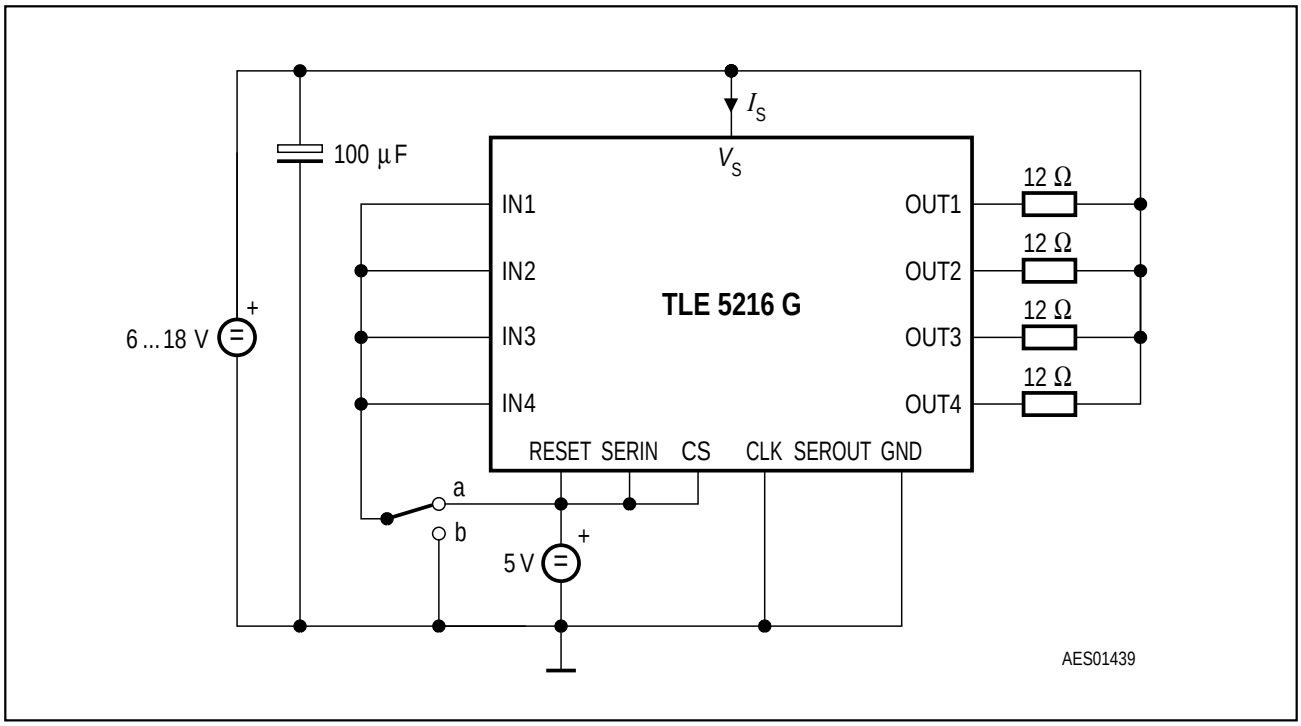


Figure 5
Test Circuit 3

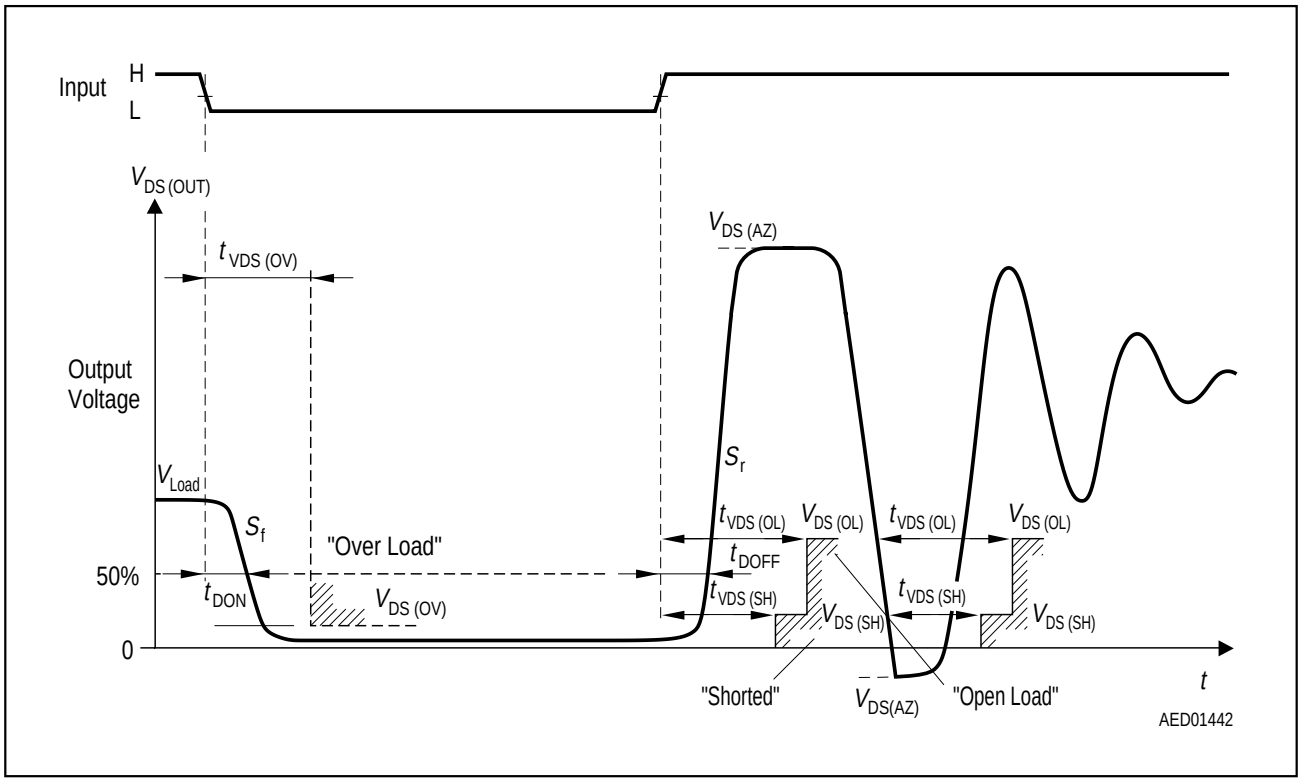


Figure 6
Switching Waveforms with Inductive Loads

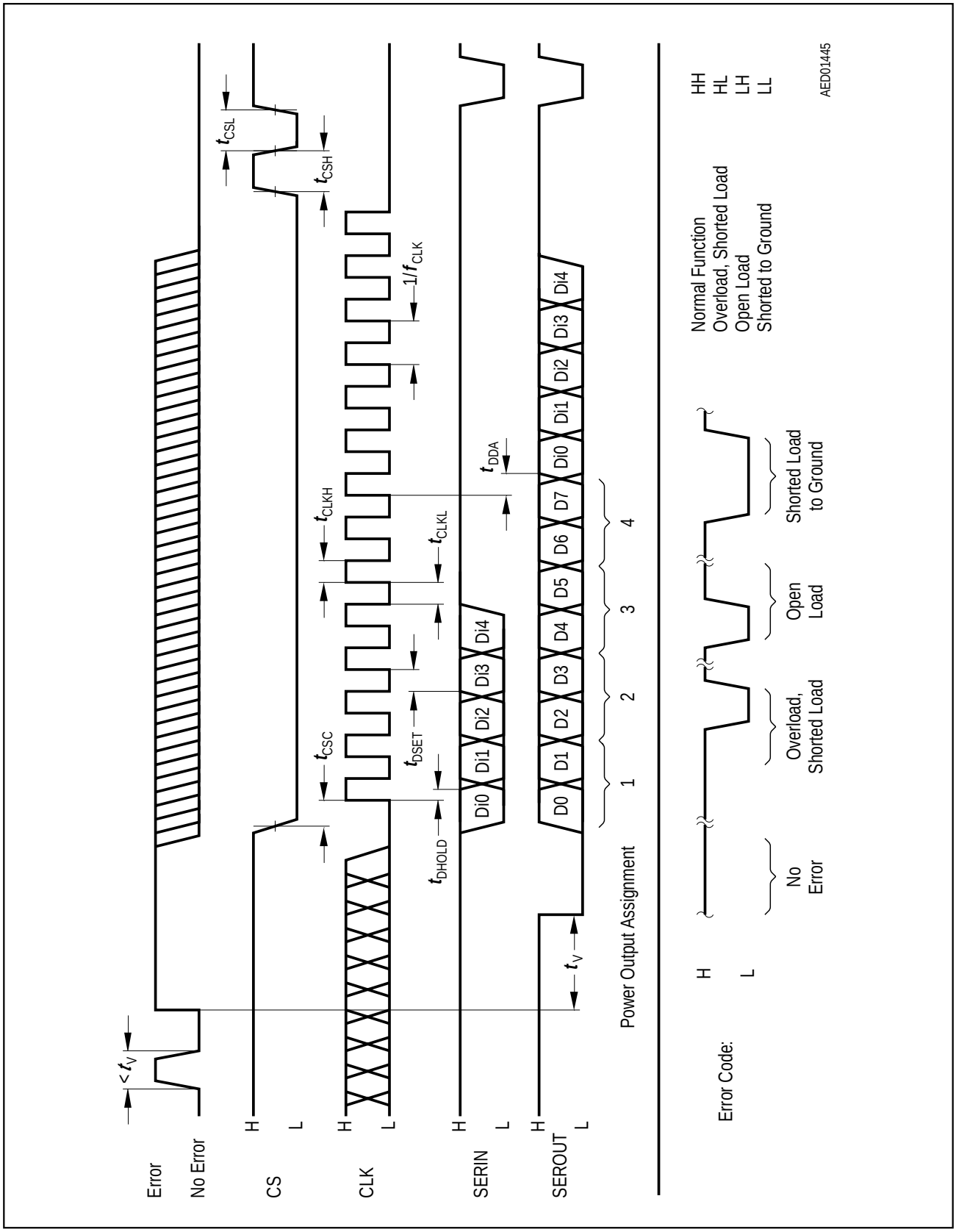
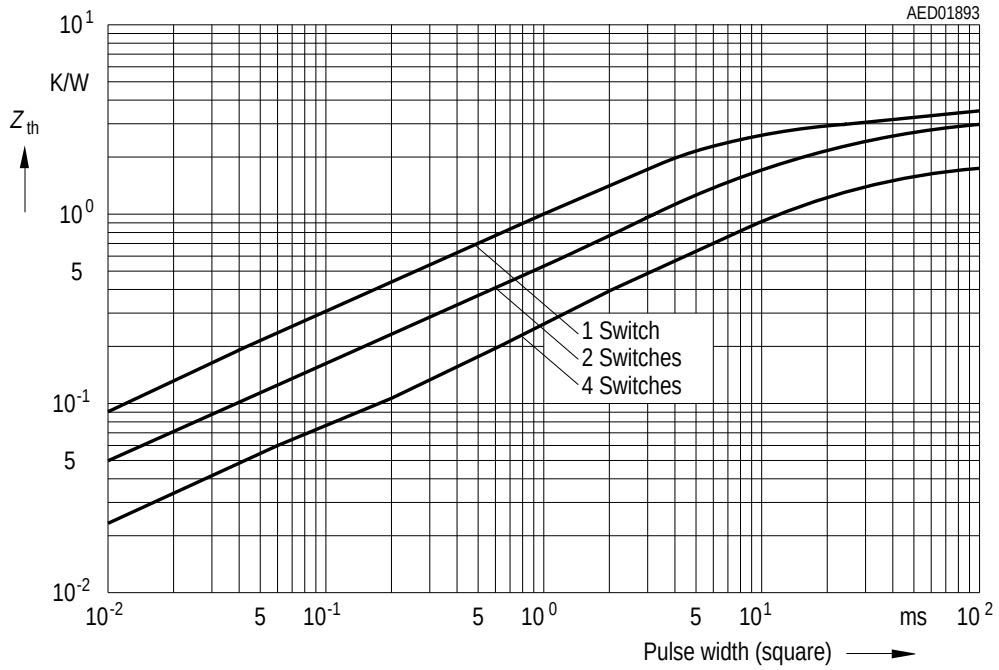


Figure 7
Serial Diagnostic Interface Timing Diagram

Thermal Resistance for P-DSO-20-10



Note: Thermal resistance is measured at T_C = 25 °C and T_{jpeak} = 45 °C. Multiple switches are equally loaded at the same time.

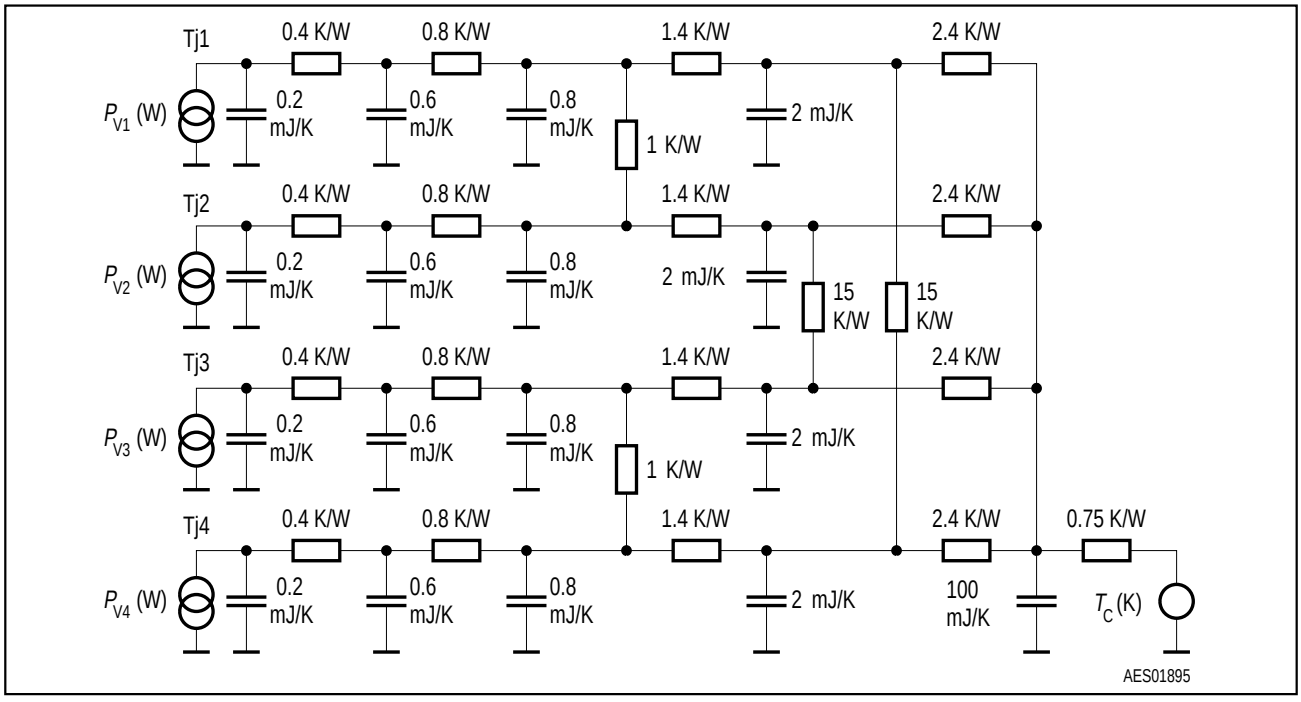
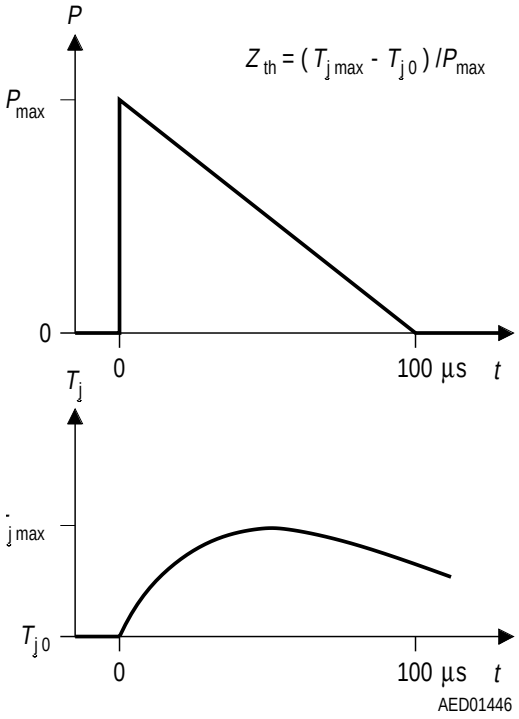


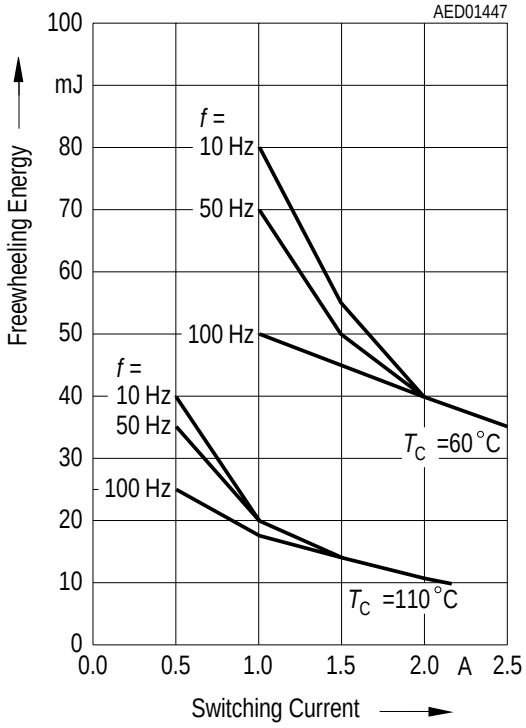
Figure 8
Thermal Equivalent Circuit for P-DSO-20-10

Note: Thermal equivalent circuit is valid at T_C = 25 °C and 25 °C < T_j < 45 °C. At T_C = 110 °C and 110 °C < T_j < 130 °C, Z_{th} is 15 % higher. For high power transients with $T_{j\,max} - T_C \leq$ 100 K add 25 % headroom for thermal non-uniformity.

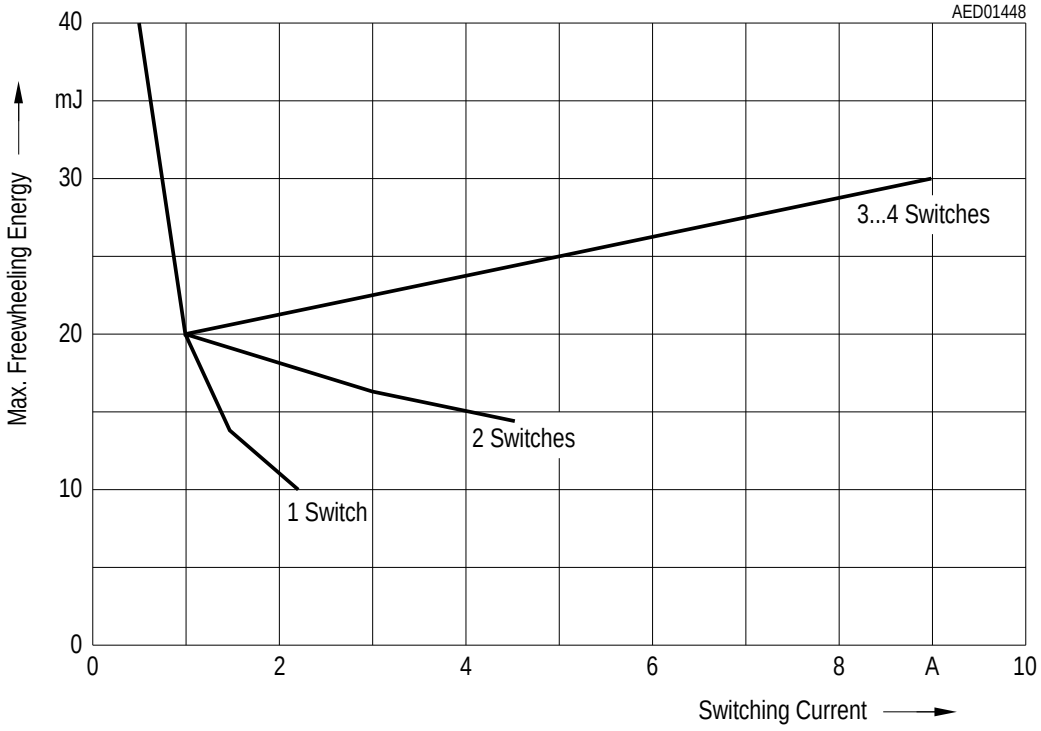
Definition of Dynamic Thermal Resistance (triangle Pulse)



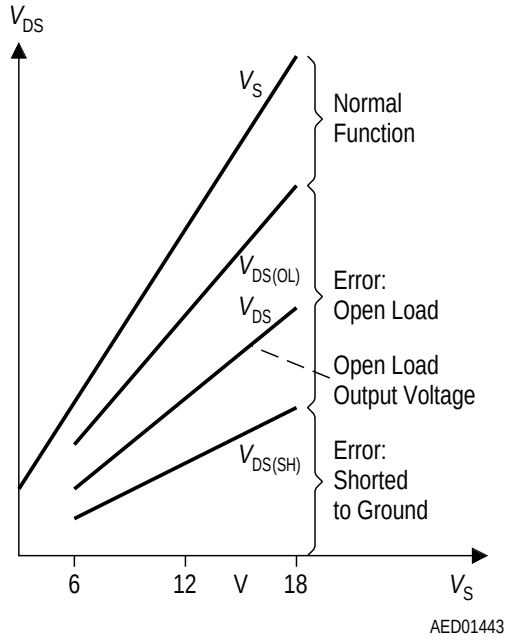
Maximum Freewheeling Energy for Inductive Loads



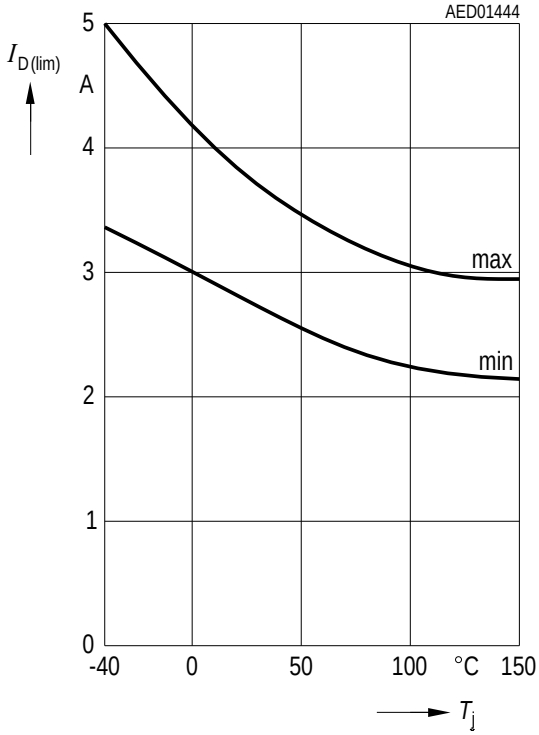
Maximum Freewheeling Energy for Inductive Loads with Various Switches in Parallel T_C = 110 °C, f = 10 Hz



Diagnostic Threshold versus Supply Voltage



Current Limitation versus Temperature



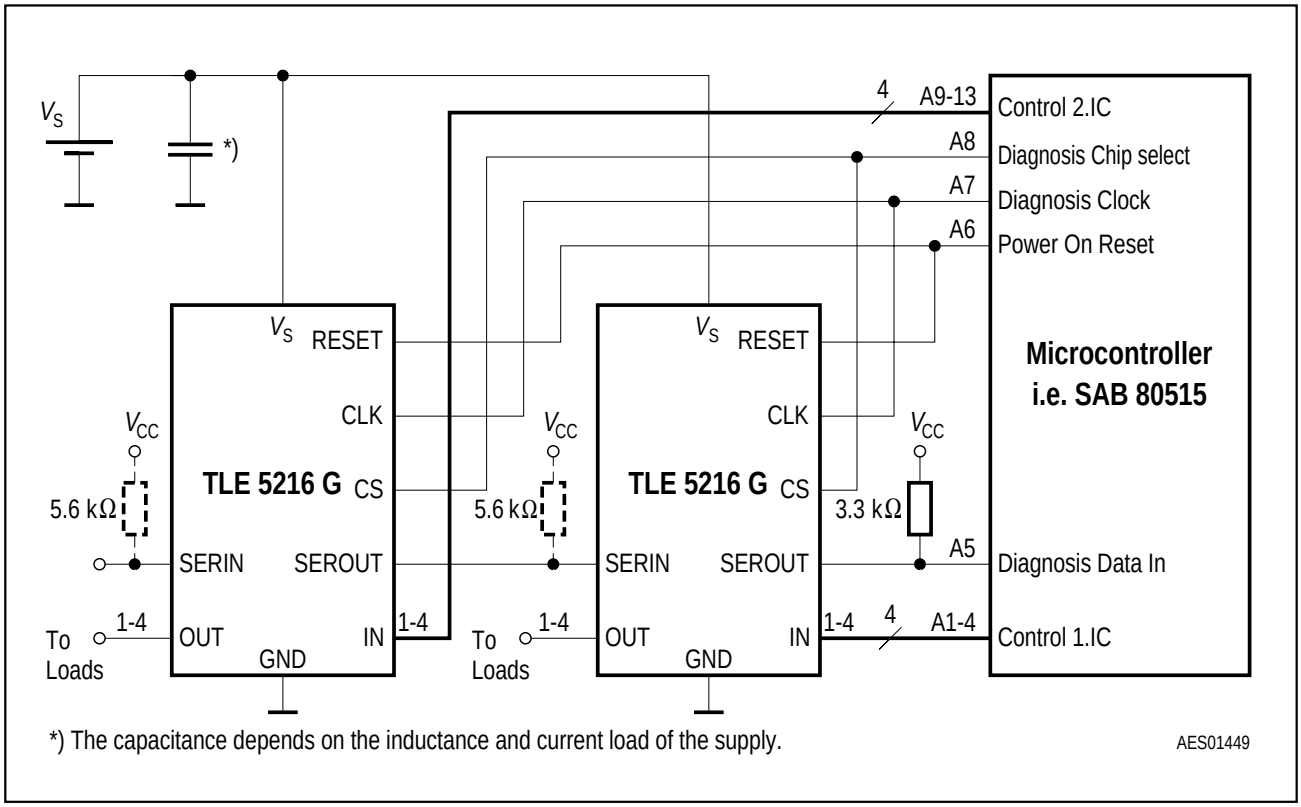
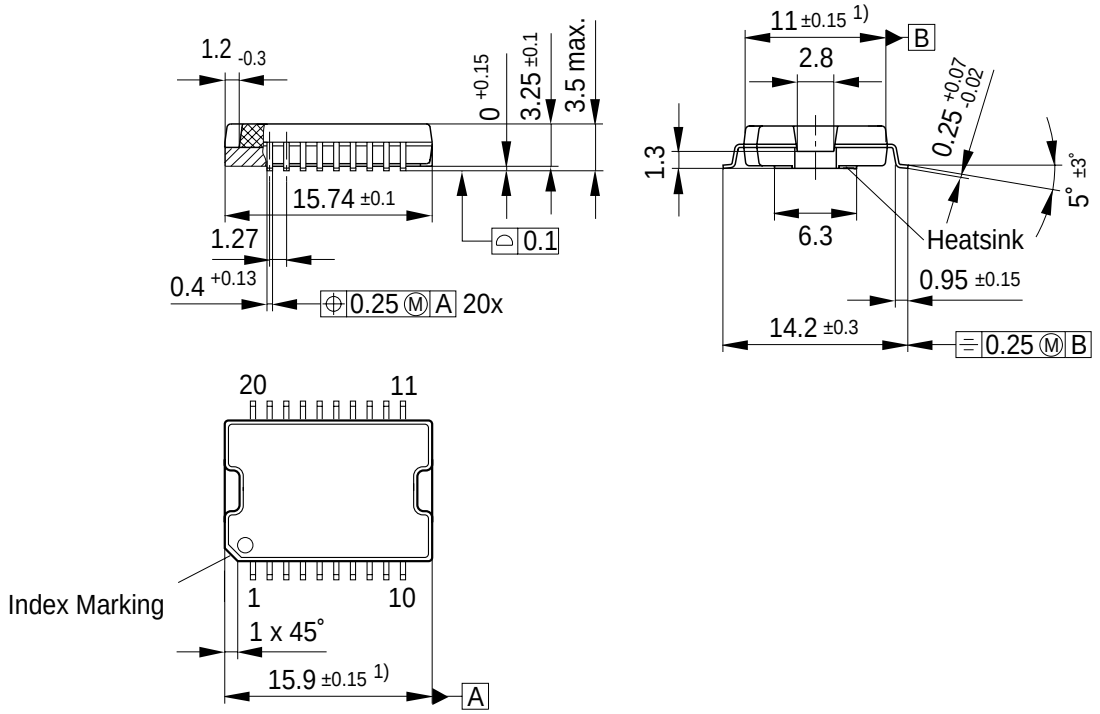


Figure 9
Application Circuit

Package Outlines

P-DSO-20-10
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS05791

GPS05791

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm