Low Cost, Low Power Stereo Audio Analog Front End

Preliminary Technical Data — AD74322

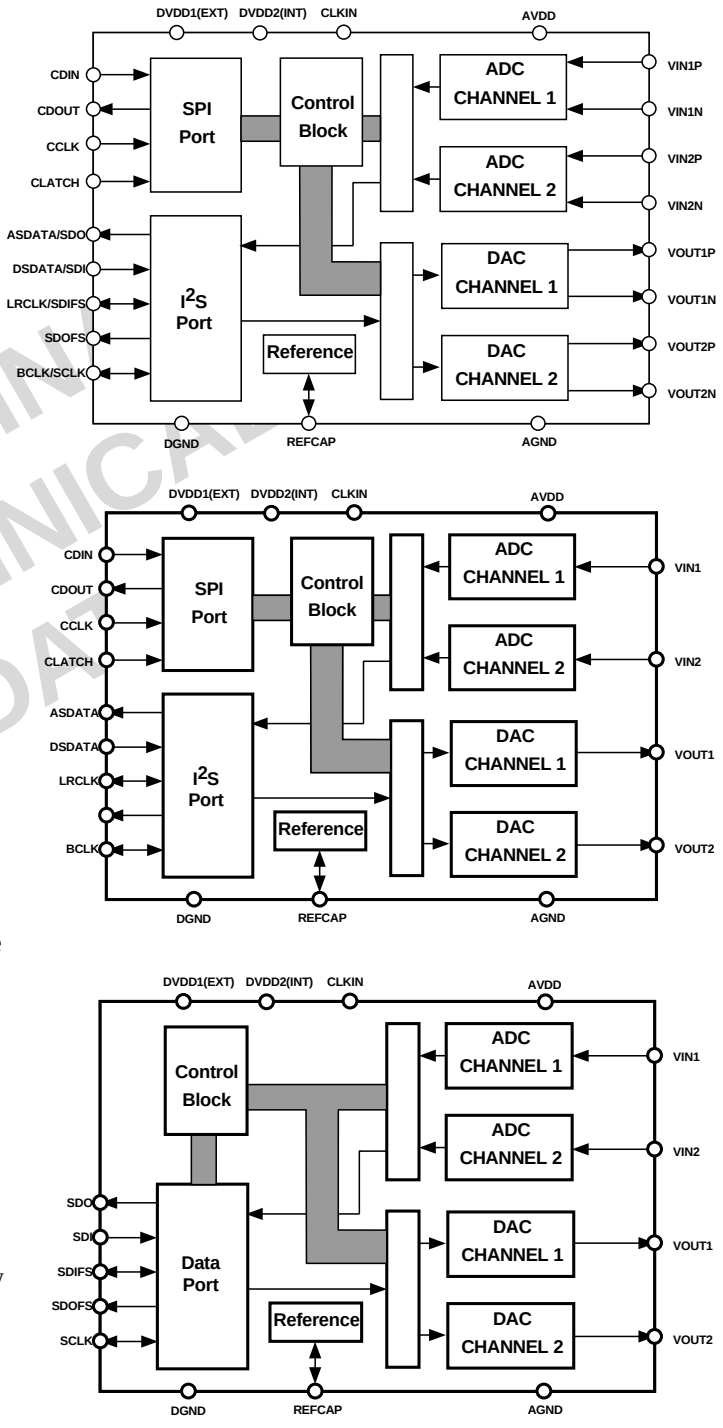
FEATURES

2.5V Stereo Audio Codec with 3.3 V Tolerant Digital Interface
Supports 96 kHz Sample Rates
Supports 16/18 /20/24-Bit Word Lengths
Multibit Sigma Delta Modulators with
"Perfect Differential Linearity Restoration" for Reduced Idle Tones and Noise Floor
Data Directed Scrambling DACs - Least Sensitive to Jitter
Performance (20 Hz to 20 kHz)
90 dB ADC and DAC SNR
Digitally Programmable Input/Output Gain
On-chip Volume Controls Per Output Channel
Hardware and Software Controllable Clickless Mute
Supports 256xFs, 512xF_s and 768xFs Master Mode Clocks
Master Clock Pre-Scaler for use with DSP master clocks
Flexible Serial Data Port with Right-Justified, Left-Justified, I^2S-Compatible and DSP Serial Port Modes
Supports Packed Data Mode ("TDM") for cascading devices.
On-Chip Reference
16, 20 and 24-Lead SOIC, SSOP and TSSOP Package options.

APPLICATIONS

Digital Video Camcorders (DVC)
Portable Audio Devices (Walkman etc)
Audio Processing
Voice Processing
Conference Phones
General Purpose Analog I/O

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD74322 is a front-end processor for general purpose audio and voice applications. It features two multi-bit ΣΔ A/D conversion channels and two multi-bit ΣΔ D/A conversion channels. Each ADC channel provides >85 dB signal-to-noise ratio while each DAC channel provides >90 dB, both over an audio signal bandwidth.

The AD74322 is particularly suitable for a variety of applications where stereo input and output channels are required, including audio sections of Digital Video Camcorder, portable personal audio devices and the analog front ends of conference phones . Its high quality performance also make it suitable for speech and telephony applications such as speech recognition and synthesis and modern feature phones.

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An on-chip reference voltage is included but can be bypassed if required for use with an external reference source.

The AD74322 offers sampling rates which, depending on MCLK selection and MCLK divider ratio, range from 8 kHz in the voiceband range to 96 kHz in the audio range.

The digital interface to the AD74322 is configured as two separate ports which allow separation of device control and data streams. Control and status are monitored using an SPI® compatible serial port while the input and output data streams are controlled using an I²S® port. The two I²S streams are controlled by a common Bit-Clock and Left/Right Clock pins. There is also a DSP mode available on the audio data port which will also allow both control and data to be streamed through the same interface where controller resources are limited.

The AD74322 is available in various lead count package options. These range from a 16-pin variant with single-ended inputs/outputs and no SPI port through a 20-pin variant with single-ended inputs/outputs and an SPI port to a 24-pin variant with differential inputs/outputs and an SPI port. These devices will be available in SOIC, SSOP and TSSOP package options and are specified for the industrial temperature range of -40°C to +85°C.

PARAMETER	AD74322A Min	Typ	Max	Units	Test Conditions
ANALOG-TO-DIGITAL CONVERTERS					
ADC Resolution (all ADCs)		24		Bits	
Dynamic Range (20 Hz to 20 kHz, -60 dB Input)					
No Filter		90		dB	
With A-Weighted Filter		92		dB	
Total Harmonic Distortion + Noise		-85(0.0056)		dB(%)	
Interchannel Isolation		TBD		dB	
Interchannel Gain Mismatch		TBD		dB	
Programmable Input Gain		12		dB	
Gain Step Size		3		dB	
Offset Error			0	LSB	
Full Scale Input Voltage At Each Pin		0.5 (1.414)		Vrms (Vpp)	Single Ended
Automatic Level Control					
Attack Time Resolution		TBD		Bits	
Attack Time		TBD		µs/Bit	
Decay Time Resolution		TBD		Bits	
Decay Time		TBD		µs/Bit	
Gain Drift		TBD		ppm/°C	
Input Resistance	10			kΩ	
Input Capacitance			15	pF	
Common Mode Input Volts		1.1V		V	
DIGITAL-TO-ANALOG CONVERTERS					
Dynamic Range (20 Hz to 20 kHz, -60 dB Input)					
No Filter		90		dB	
With A-Weighted Filter		92		dB	
Total Harmonic Distortion + Noise		-85(0.0056)		dB(%)	
Interchannel Isolation		TBD		dB	
Interchannel Gain Mismatch		TBD		dB(%)	
DC Accuracy					
Gain Error		TBD		%	
Interchannel Gain Mismatch		TBD		ppm/°C	
Gain Drift		TBD		dB	
Interchannel Crosstalk (EIAJ method)		TBD		dB	
Interchannel Phase Deviation		TBD		Degrees	
Volume Control Step Size (1023 Linear Steps)		0.098		%	
Volume Control Range (Max Attenuation)		60		dB	
Mute Attenuation		-100		dB	
De-emphasis Gain Error			+/- 0.1	dB	
Full Scale Output Voltage At Each Pin		0.5 (1.414)		Vrms(Vpp)	Single Ended
Output Resistance At Each Pin		??	??	Ω	
Common Mode Output Volts		2.25		V	
REFERENCE (Internal)					
Absolute Voltage, V_{REF}		1.1		V	
V_{REF} TC		TBD		ppm/°C	
ADC DECIMATION FILTER					
Pass Band			0.xxxFs	Hz	
Pass Band Ripple			±0.00xx	dB	
Transition Band	0.xxFs		0.xxFs	Hz	
Stop Band	0.xxFs			Hz	
Stop Band Attenuation	70			dB	
Group Delay	lll/Fs	nnn/Fs	mmm/Fs	ms	
DAC INTERPOLATION FILTER					
Pass Band			0.xxxFs	Hz	
Pass Band Ripple			±0.00xx	dB	
Transition Band	0.xxFs		0.xxFs	Hz	
Stop Band	0.xxFs			Hz	
Stop Band Attenuation	70			dB	
Group Delay	lll/Fs	nnn/Fs	mmm/Fs	ms	

AD74322–SPECIFICATIONS

(AVDD = DVDD2 = +2.5V ±10%, DVDD1 = 3.0V ±10%, f_{CLKIN} = 12.288 MHz, f_{SAMP} = 48 kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

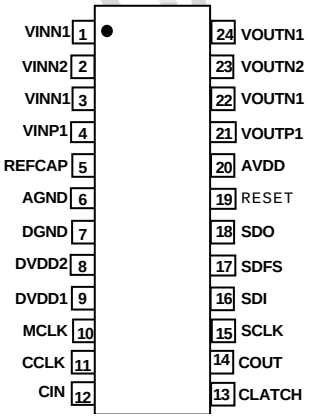
PARAMETER	AD74322A Min	Typ	Max	Units	Test Conditions
LOGIC INPUT					
V_{INH}, Input High Voltage	DVDD1 - 0.8		DVDD1	V	
V_{INL}, Input Low Voltage	0		0.8	V	
Input Current	-10		+10	µA	
Input Capacitance			10	pF	
LOGIC OUTPUT					
V_{OH}, Output High Voltage	DVDD1 - 0.4		DVDD1	V	
V_{OL}, Output Low Voltage	0		0.4	V	
Three-State Leakage Current	-10		+10	µA	
POWER SUPPLIES					
AVDD, DVDD2	2.25	2.5	2.75	V	
DVDD1	2.7	3.0	3.3	V	
POWER CONSUMPTION					
All Sections On			TBD	mA	
ADCs On Only			TBD	mA	
DACs On Only			TBD	mA	
Reference On Only			TBD	mA	
Powerdown Mode			TBD	µA	

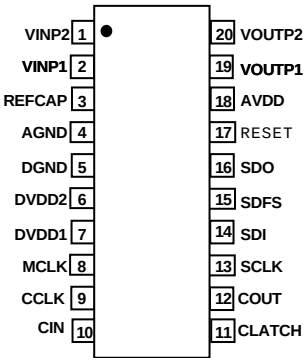
ORDERING GUIDE

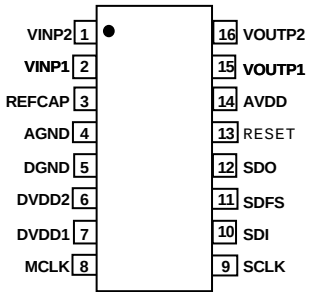
Model	Range	Package
AD74322DAR	-40 C to +85 C	R-16
AD74322DARU	-40 C to +85 C	RU-16
AD74322AAR	-40 C to +85 C	R-20
AD74322AARU	-40 C to +85 C	RU-20
AD74322AAR	-40 C to +85 C	R-24
AD74322AARU	-40 C to +85 C	RU-24

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the XX0000 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.







PIN FUNCTION DESCRIPTION (SINGLE-ENDED I/O ; NO SPI PORT)

Mnemonic	I/O	Function
VIN1	I	Analog Input - Channel 1
VIN2	I	Analog Input - Channel 2
VOUT1	O	Analog Output - Channel 1
VOUT2	O	Analog Output - Channel 2
REFCAP	I/O	Internal Reference - Can also be used for connection of an external reference
AVDD		Analog Power Supply Connection
AGND		Analog Ground/Substrate Connection
DVDD1		Digital Power Supply Connection (Interface)
DVDD2		Digital Power Supply Connection (Core)
DGND		Digital Ground/Substrate Connection
MCLK	I	External Clock Connection
SDO	O	ADC Serial Data Out - DSP Mode
SDI	I	DAC Serial Data In - DSP Mode
$\overline{\text{SDFS}}$	I/O	Serial Data Input Frame Sync - DSP Mode
$\overline{\text{RESET}}$	I	Powerdown/Reset Input
SCLK	I/O	Serial Clock - DSP Mode

PIN FUNCTION DESCRIPTION (SINGLE-ENDED I/O WITH SPI PORT)

Mnemonic	I/O	Function
VIN1	I	Analog Input - Channel 1
VIN2	I	Analog Input - Channel 2
VOUT1	O	Analog Output - Channel 1
VOUT2	O	Analog Output - Channel 2
REFCAP	I/O	Internal Reference - Can also be used for connection of an external reference
AVDD		Analog Power Supply Connection
AGND		Analog Ground/Substrate Connection
DVDD1		Digital Power Supply Connection (Interface)
DVDD2		Digital Power Supply Connection (Core)
DGND		Digital Ground/Substrate Connection
MCLK	I	External Clock Connection
CDIN	I	Serial Data In on SPI Control Port
CDOUT	O	Serial Data Out on SPI Control Port
CCLK	I	Serial Clock on SPI Control Port
CLATCH	I	Serial Data Latch on SPI Control Port
ASDATA	O	ADC Serial Data Out - I^2S
DSDATA	I	DAC Serial Data In - I^2S
LRCLK/	I/O	Left/Right Channel Select - I^2S
BCLK	I/O	Bit Clock - I^2S
RESET	I	Powerdown/Reset Input

PIN FUNCTION DESCRIPTION (DIFFERENTIAL I/O WITH SPI PORT)

Mnemonic	I/O	Function
VINP1	I	Analog Input - Channel 1 Positive
VINN1	I	Analog Input - Channel 1 Negative
VINP2	I	Analog Input - Channel 2 Positive
VINN2	I	Analog Input - Channel 2 Negative
VOUTP1	O	Analog Output - Channel 1 Positive
VOUTN1	O	Analog Output - Channel 1 Negative
VOUTP2	O	Analog Output - Channel 2 Positive
VOUTN2	O	Analog Output - Channel 2 Negative
REFCAP	I/O	Internal Reference - Can also be used for connection of an external reference
AVDD		Analog Power Supply Connection
AGND		Analog Ground/Substrate Connection
DVDD1		Digital Power Supply Connection (Interface)
DVDD2		Digital Power Supply Connection (Core)
DGND		Digital Ground/Substrate Connection
MCLK	I	External Clock Connection
CDIN	I	Serial Data In on SPI Control Port
CDOUT	O	Serial Data Out on SPI Control Port
CCLK	I	Serial Clock on SPI Control Port
CLATCH	I	Serial Data Latch on SPI Control Port
ASDATA	O	ADC Serial Data Out - I^2S
DSDATA	I	DAC Serial Data In - I^2S
LRCLK/	I/O	Left/Right Channel Select - I^2S
BCLK	I/O	Bit Clock - I^2S
RESET	I	Powerdown/Reset Input

FUNCTIONAL DESCRIPTION

ADC Section

There are two ADC channels in the AD74322, configured as a stereo pair. Each ADC channel can be independently muted. The input pins are switched between differential inputs or four single ended inputs accordingly. The gain block can be programmed for independent left and right gains, in steps of +3dB, from 0dB to +12dB. The ADC operates at an oversampling ratio of 128 and the decimation filter reduces the output to the standard sample rates. The output maximum sample rate is 96 kHz at ASDATA.

Automatic Level Control

Analog Sigma Delta Modulator

Decimator Section

The digital decimation filter has a passband ripple of ±0.01dB and a stopband attenuation of 70dB. The filter is an FIR type with a linear phase response. The group delay at 48kHz is ??us. Output sample rates up to 96 kHz are supported.

Input Signal swing

Each ADC input has an input range of $0.5\ V_{RMS}$ / $1.414\ V_{P-P}$ (Single-Ended) about a bias point equal to V_{REFCAP} (See Figure <Input_Swing>)

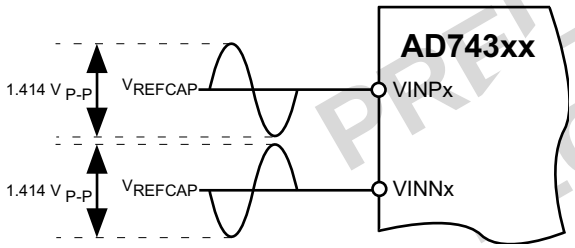


Figure <Input_Swing>

DAC Section

The AD74322 has two DAC channels arranged as a stereo pair, with two, fully differential voltage, analog outputs for improved noise and distortion performance. Each channel has it's own independently programmable attenuator with a maximum attenuation of 63dB, adjustable in 1dB steps. Digital inputs are via a serial data input pin and a common frame (DLRCLK) and bit (DBLCK) clock or using a 'packed data' mode, both channels can be input using a single data pin.

Interpolator Section

Digital Sigma Delta Modulator

DAC

Analog Output Filter

Output Signal swing

Each ADC input has an output range of $0.5\ V_{RMS}$ / $1.414\ V_{P-P}$ (Single-Ended) about a bias point equal to V_{REFCAP} (See Figure <Output_Swing>)

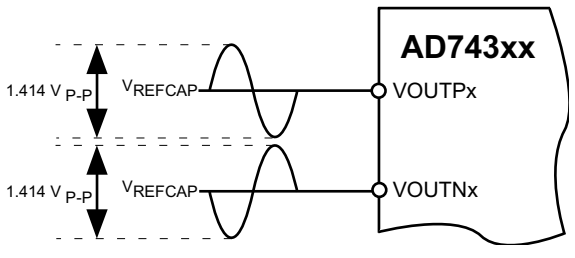


Figure <Output_Swing>

Reference

The AD74322 features an on-chip reference whose nominal value is 1.125 V.A __ nF capacitor applied at the REFCAP pin is necessary to stabilise the referrence. (See Figure <REFCAP_Int>)

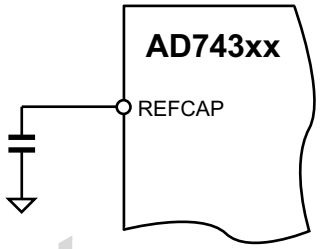


Figure <REFCAP_Int>

If it is required to use an external reference, because of its value or its reference tempco, the internal reference can be disabled via Control Register __ and the external reference applied at the REFCAP pin (See Figure <REFCAP_Ext>).

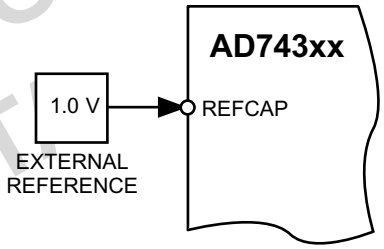
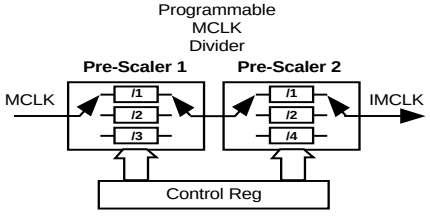


Figure <REFCAP_Ext>

Master Clocking Scheme

The update rate of the AD74322's ADC and DAC channels require an internal master clock (IMCLK) which is 256 times that sample update rate (IMCLK = 256 * F_S). In order to provide some flexibility in selecting sample rates, the device has a series of three master clock pre-scalers which are programmable and allow the user to choose a range of convenient sample rates from a single external master clock. The master clock signal to the AD74322 is applied at the MCLK pin. The MCLK signal is passed through a series of two programmable MCLK pre-scalers (divider) circuits which can be selected to reduce the resulting Internal MCLK (IMCLK) frequency if required. The first MCLK pre-scaler provides divider ratios of /1 (pass through), /2, /3 while the second pre-scaler provides divider ratios of ./1 (pass through), /2, /4 and the third pre-scaler provides ratios of /1 (pass through), /2 and /5..



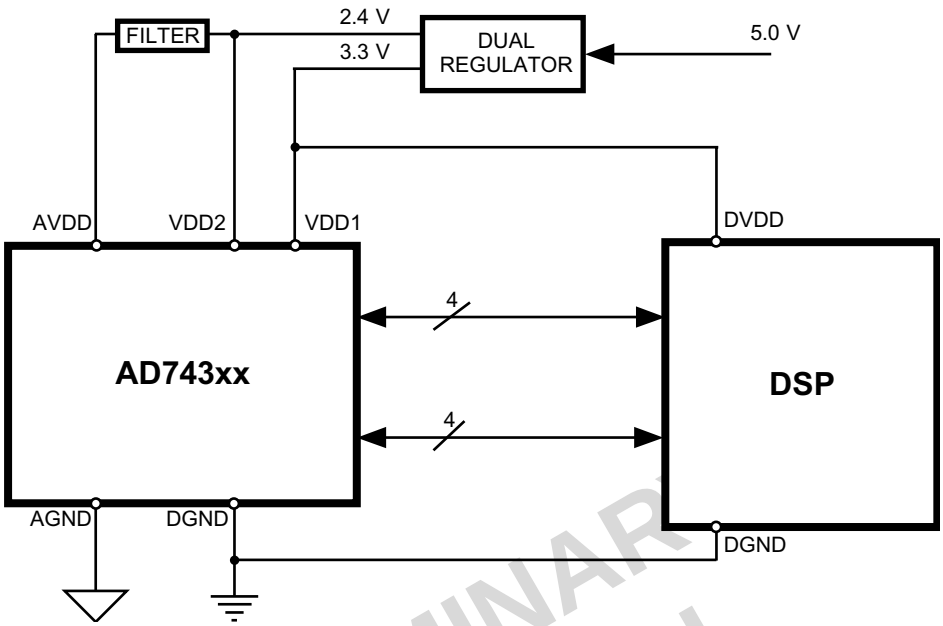


Figure <PSU_Connection>

Figure <MCLK_Divider>

The divider ratios will allow more convenient sample rate selection from a common MCLK which may be required in many voice related applications.

Example 1: f_{SAMP} = 48 kHz and 8 kHz required

MCLK = $48*10^3$ * 256 = 12.288 MHz to cater for 48 kHz f_{SAMP}

For f_{SAMP} = 8 kHz, it is necessary to use the /3 setting in Pre-Scaler 1, the /2 setting in Pre-Scaler 2 and pass through in Pre-Scaler 3. This results in an IMCLK = $8*10^3$ * 256 = 2.048 MHz (= 12.288 MHz/6).

Example 2: f_{SAMP} = 48 kHz and 32 kHz required

MCLK = 24.576 MHz

For f_{SAMP} = 48 kHz, it is necessary to use the /2 setting in Pre-Scaler 1 and the /1 (pass-through) setting in Pre-Scaler 2 and pass through in Pre-Scaler 3. This results in an IMCLK = $48*10^3$ * 256 = 12.288 MHz.

For f_{SAMP} = 32 kHz, it is necessary to use the /3 setting in Pre-Scaler 1 and the /1 (pass-through) setting in Pre-Scaler 2 and pass through in Pre-Scaler 3. This results in an IMCLK = $32*10^3$ * 256 = 8.192 MHz.

Example 3: fSAMP = 44.1 kHz and 11.025 kHz required

MCLK = $44.1*10^3$ * 256 = 11.2896 MHz to cater for 44.1 kHz f_{SAMP}

For f_{SAMP} = 11.025 kHz, it is necessary to use the /1 setting in Pre-Scaler 1 and the /4 setting in Pre-Scaler 2 and pass through in Pre-Scaler 3. This results in an IMCLK = $11.025*10^3$ * 256 = 2.8224 MHz (= 11.2896 MHz/4).

SampleRates

For all applications the sampling rate is defined by the internal master clock frequency (IMCLK) where IMCLK = 256 * f_{SAMP}.

Power-On Reset

The AD74322 features a power-on reset circuit which ensures that all internal circuitry is reset and initialised to a known state following the power-up of the device. There is also a software reset capability available by setting the RESET bit in Control Register _. This control register is accessed through the Control Port.

Power Supplies and Grounds

The AD74322 features three separate supplies: AVDD, DVDD1 and DVDD2.

AVDD is the supply to the analog section of the device and must therefore be of sufficient quality to preserve the AD74322's performance characteristics. It is nominally a 2.4 V supply.

DVDD1 is the supply for the digital interface section of the device. It is fed from the digital supply voltage of the DSP or controller to which the device is interfaced and allows the AD74322 to interface with devices operating at supplies of between 2.4 V -5% to 3.3 V + 10%.

DVDD2 is the supply for the digital core of the AD74322. It is nominally a 2.4 V supply.

MCLK (MHz)	Sampling Rates (kHz) using Scalar (Divider) Ratios (assumes 256fs)										
	1	**2**	**3**	**4**	**5**	**6**	**8**	**9**	**10**	**12**	**15**
2.048	8	4	-	2	-	-	1	-	-	-	-
12.288	48	24	-	12	-	-	6	-	-	-	-
16.384	64	32	-	16	-	-	8	-	-	-	-
24.576	96	48	-	24	-	-	12	-	-	-	-
36.864	-	-	48	-	-	24	-	-	-	12	-

Table <MCLK_Divider>

Sampling Rate f_S (kHz)	Interpolator Mode	MCLK (MHz)		
		256f_S	**512f_S**	**768f_S**
8 16	8x (Normal) 4x (Double)	2.048	4.096	6.144
11.1 22.2	8x (Normal) 4x (Double)	2.8224	5.6448	8.4672
32 64	8x (Normal) 4x (Double)	8.192	16.384	24.576
44.1 88.2	8x (Normal) 4x (Double)	11.2896	22.5792	33.8688
48 96	8x (Normal) 4x (Double)	12.288	24.576	36.864

Table <MCLK_Select>

INTERFACING

The AD74322 features two separate interfaces, Control and Data, which are used to program control settings and send/receive sample data respectively. The Control interface is implemented using an SPI® type protocol but transfers 16-bits per frame. The Data interface uses either a DSP or I²S® protocol to transfer stereo data samples between controller and codec. The DSP compatible interface mode allows data samples to be transferred in a protocol that is supported by the serial interfaces of most fixed- and floating-point DSPs.

In order to reduce peripheral requirements when interfacing the AD74322 with the host DSP, the DSP mode allows the DSP to send both data and control information to the device via the data interface. This is the default mode and requires users to only use a single DSP SPORT to both control the device and service it with data samples.

ControlInterface

Control of the AD74322 operation is via a set of 16 Control Registers which are programmed through the Control Port. The Control Port protocol is similar to the SPIÒ protocol with the exception that 16-bits of data are transferred per frame. The Control Port consists of the following pins: CCLK - Control Port Serial Clock, CLATCH - Control Port Latch or Frame signal, CDIN - Control Port Serial Data In and CDOUT - Control Port Data Out. CLATCH is a framing signal that is active low. When asserted, it gates the other interface lines as being active. CCLK is used to clock input data on CDIN and clock output (readback) data on CDOUT. Figure <Control_Interface> details the connectivity of the Control Port to a controller and Figure <Control_Timing> details the interface timing.

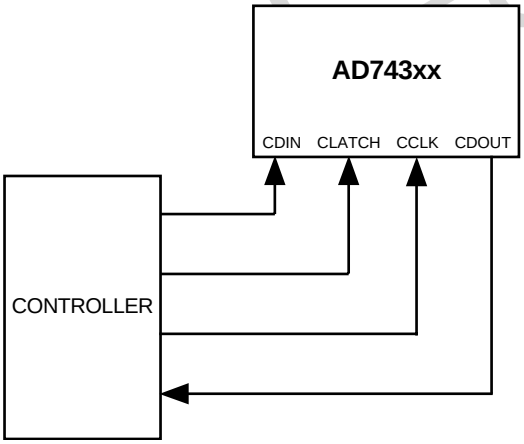


Figure <Control_Interface>

Data in and out of the Control Port go through a 16-bit shift register whose contents are mapped to the internal registers using the mapping scheme of Figure <ContPortMap>. A 16-bit word received by the Control Port is decoded as a read or write to a register address set by bits 15 - 12. This 4-bit register address selects 1 of 16 registers as shown in Table <ContRegMap>. Bit 11 selects whether a register read or write is requested - Write = 0, Read = 1. Bit-10 is reserved. Bits 9 through 0 contain register data. Each Control register's contents are detailed below.

DataInterface

There are two modes of operation of the data interface: DSP mode and I2S mode. The default mode of the data interface is a DSP mode which combines control and data functions in a single protocol. This is to reduce the peripheral overhead required on the DSP when interfacing to the AD74322. This mode operates in a standard DSP serial format. In I2S mode the data interface streams audio data samples being sent to or received from the DACs and ADCs respectively, using the I2S serial protocol.

In either mode it can be configured as either a master or slave device ensuring connectivity to the largest number of host processors.

DSPMode

The DSP mode allows interfacing to most fixed- and floating-point DSPs as well as other processors such as RISCs etc that having serial ports that support synchronous communications. The key feature of synchronous DSP communications is that the serial data is framed by a separate Frame Sync signal. Figures <Data_DSP_Slave> and <Data_DSP_Master> detail connectivity in Master Mode (codec is master) and Slave Mode (codec is slave) respectively.

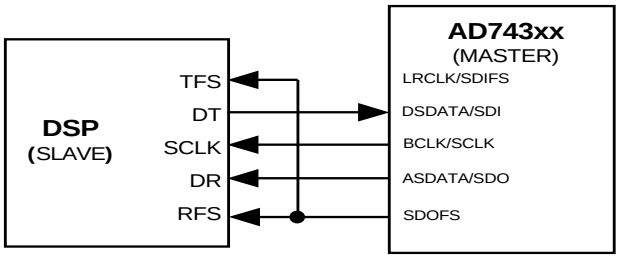


Figure <Data_DSP_Slave>

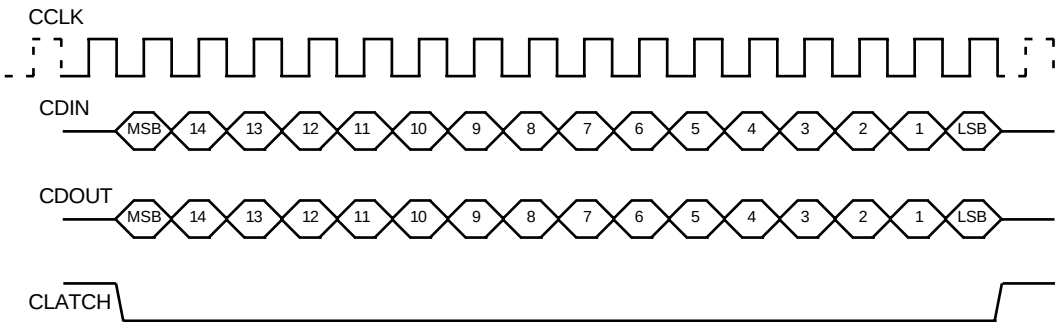


Figure <Control_Timing>

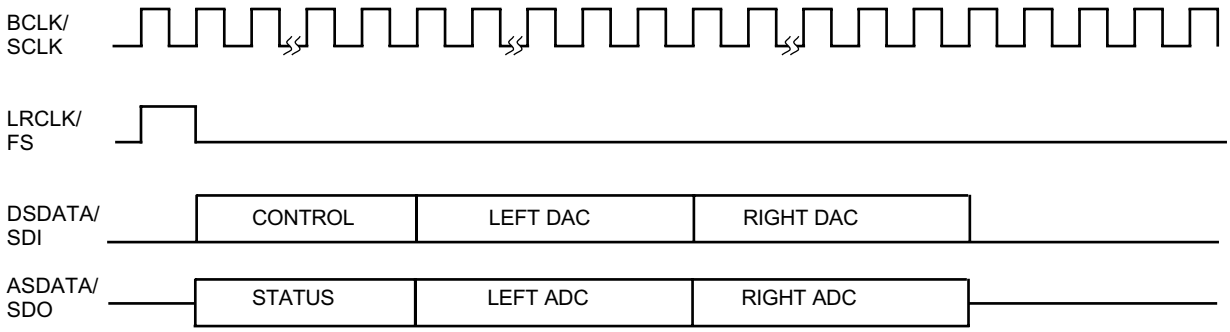


Figure <DSP_Protocol>

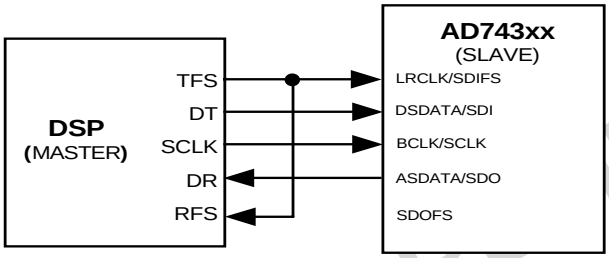


Figure <Data_DSP_Master>

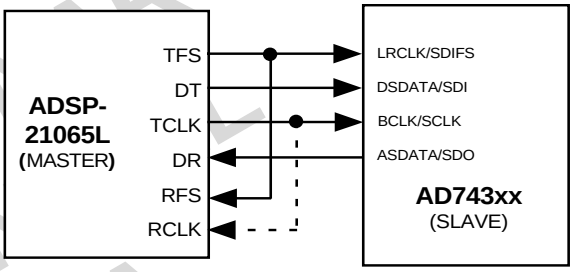


Figure <Data_I2S_DSP_Master>

The serial protocol uses a fixed position for data being sent to or received from the Left and Right DACs and ADCs respectively and the control words being sent to and the status words being received from the device respectively. Figure <DSP_Protocol> details the arrangement of both audio and control/status information in the serial transfer.

I²S® (Inter IC Sound Bus) Mode

The I2S bus is a three line serial bus which features a serial data line carrying both left and right (stereo) channels. The Left and Right channel information are selected by the status of the Left/Right Clock (Word Select) line. Serial data is clocked by the Bit Clock line. Figures <Data_I2S_DSP_Master> and <Data_I2S_DSP_Slave> detail the interface configuration between controller and codec in I^2S mode with controller as master and slave respectively. Figure <> details I^2S timing. The interface allows easy transfer of arbitrary length serial data samples sent MSB first. Toggling of the Left/Right Clock line indicates that the end of the current word will occur after the following Bit Clock cycle and the start of the alternate channel word will occur on the subsequent Bit Clock cycle

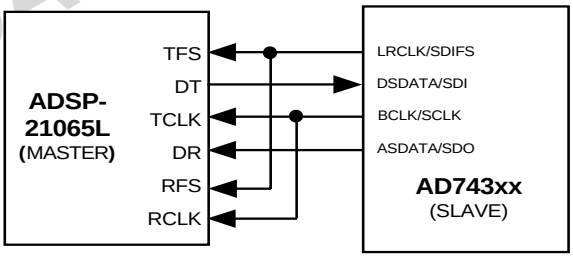
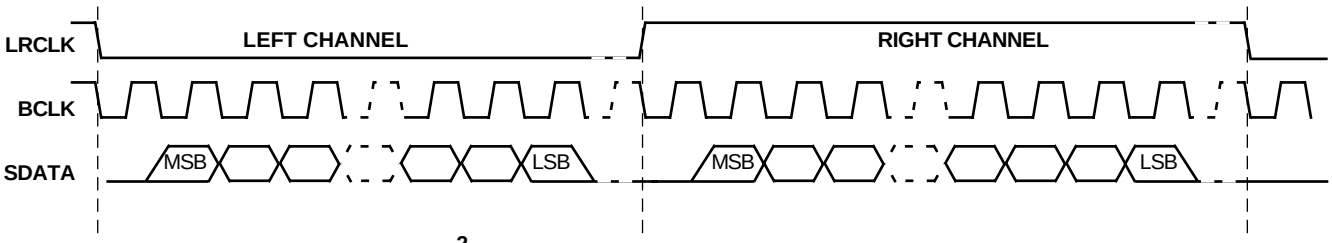


Figure <Data_I2S_DSP_Slave>



I^2S MODE - 16 TO 24-BITS PER CHANNEL

Figure <I2S_Timing>

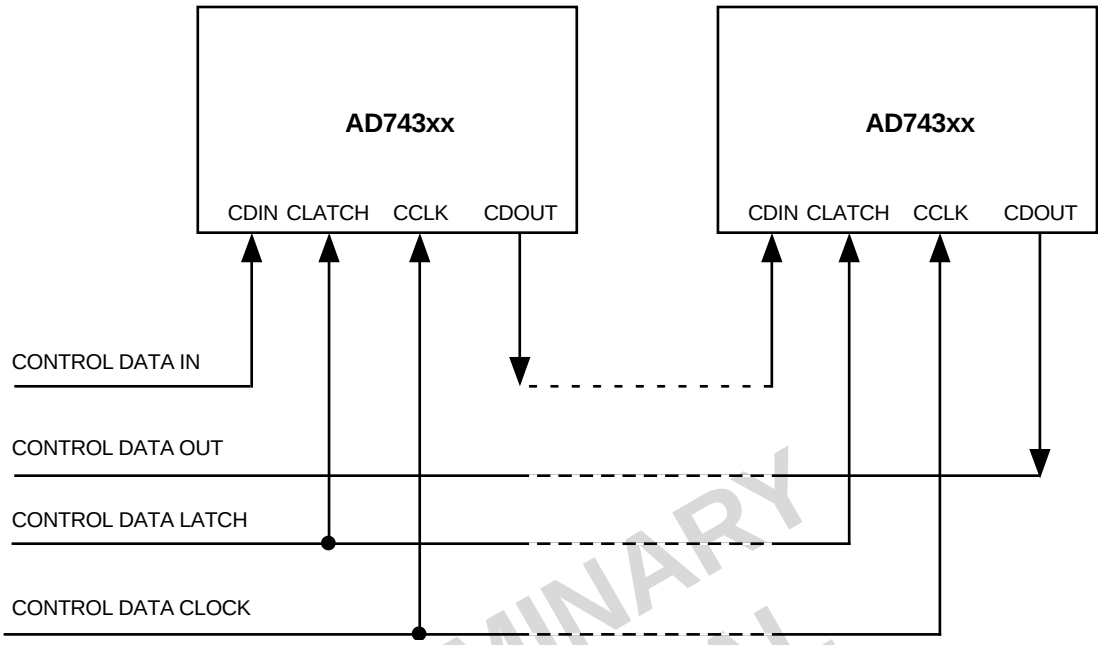


Figure <Control_Cascade_Daisy_Chain>

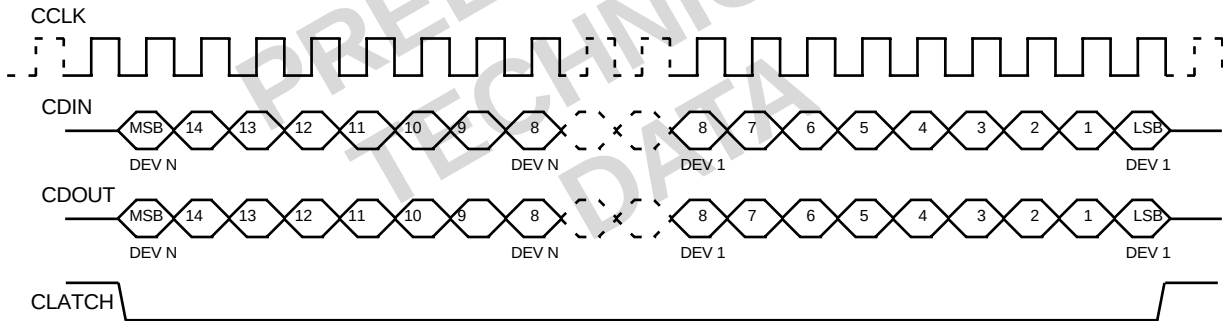


Figure <Control_Cascade_Timing_Daisy_Chain>

INTERFACING MULTIPLE DEVICES

Many applications require multiple channels of input and output. The AD743xx series of devices are designed to cater for extending the number of I/O channels by cascading devices together while interfacing to a single control or data port. This reduces the overhead requirement on the controller in terms of serial ports.

Control Port Cascading

There are two methods of cascading the Control Ports of multiple AD743xx devices together so that all devices can be controlled from a single controller serial port. One method is to configure the multiple devices as a daisy chain of Control Ports each 16-bits wide with common

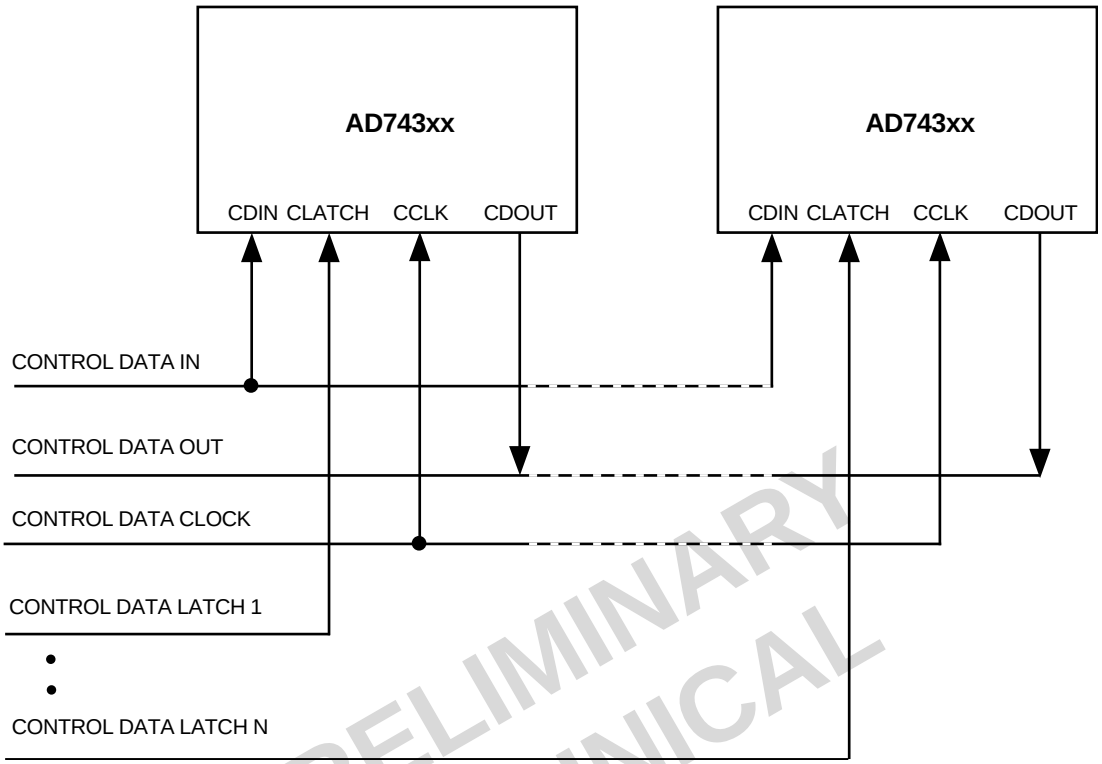


Figure <Control_Cascade_TDM>

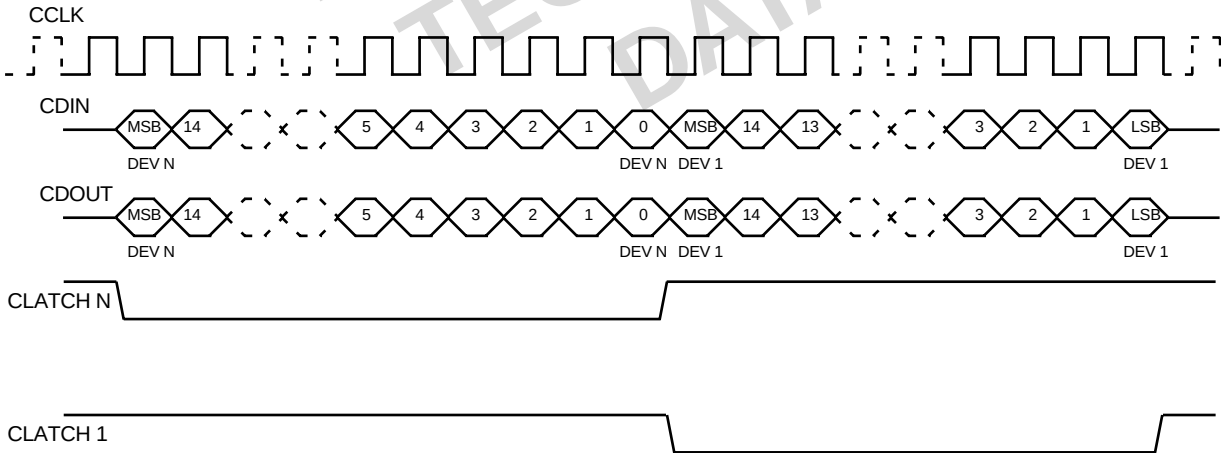
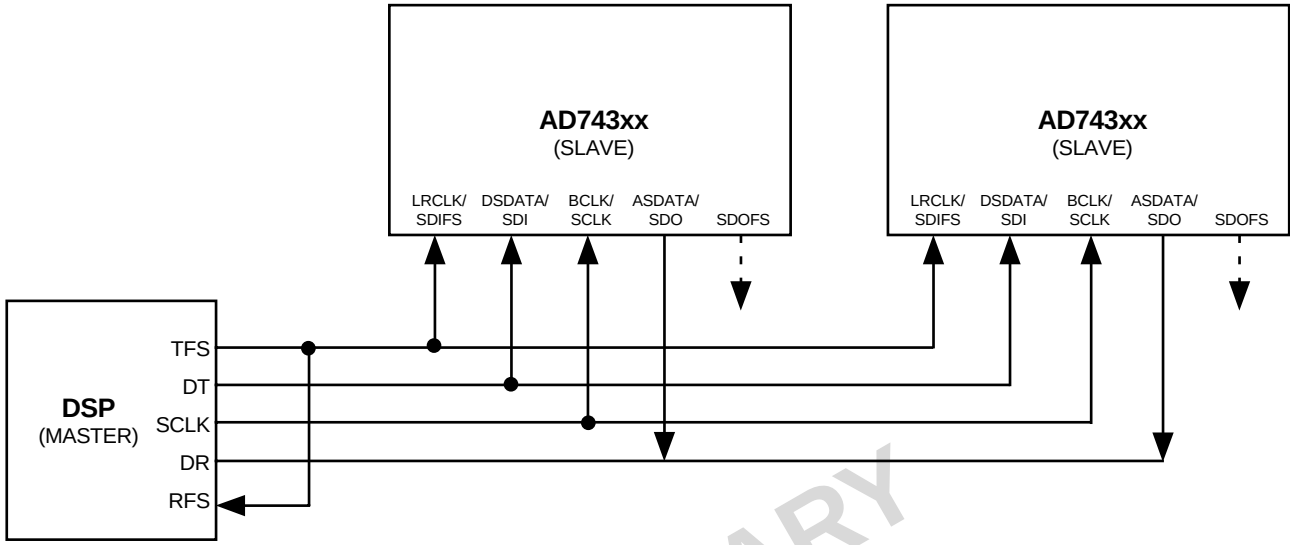


Figure <Control_Cascade_Timing_TDM>



Clock and Latch signals. The other method involves creating a common Data In and Data Out buses where each device has a common Clock but has separate Latch signals which enable the devices on the bus at different times - either as a Time Division Multiplex (TDM) or software control.

Daisy Chain Mode

In Daisy Chain Mode, the serial registers (16-bit) of each device are cascaded together by connecting the controller's Data Out to CDIN of the first device and the CDOUT of the first device to CDIN of the next device (see Figure <Control_Cascade_Daisy_Chain>). The CDOUT of the final device is connected to the controller's Data In. The effective cascade length becomes 16 * N (where N is the number of devices in cascade) and each control word write to each device requires 16 * N CCLK cycles. Please note that the CLATCH pin of each device is driven from a common controller output signal which must be active during the entire 16 * N CCLK cycles as shown in Figure <Control_Cascade_Timing_Daisy_Chain>.

TDM Mode

In TDM Mode, each device's CDIN and CDOUT are commoned to the controller's Data Out and Data In respectively (see Figure <Control_Cascade_TDM>). Each device's CLATCH pin is separately controlled. When CLATCH is disasserted activity on CDIN and CCLK is not recognised and the CDOUT pin is tri-stated. Figure <Control_Cascade_Timing_TDM> shows TDM Mode Control timing.

Data Port Cascading

The Data Port of the AD74322 is designed to allow multiple single or dual channel devices to be cascaded from a single DSP or controller serial port (SPORT). There is also a mode which allows stereo ADCs and DACs (with I2S interfaces) to be interfaced to a cascade of AD743xx devices. This allows extra flexibility in choosing the number of input and out channels in the cascade. The various (potential) modes for interfacing the data ports of multiple devices are listed below:

DSP Mode - Daisy Chaining

In this mode, sample data is passed along a daisychain of I/O registers in a similar manner that used in the present AD733xx devices. At the sample event each ADC result is placed in the I/O register and is subsequently shifted towards the DSP's Rx register. This achieved by a common SDIFS pulse which samples each device (enables each device's sample). {Drawback: as the device is stereo, we would need to send 32 bits (or perhaps more) to the I/O register at each sample event.}

TDM Mode

In multiplexed mode, each device is programmed with its cascade position. This allows devices to be enabled to the data buses only in their appropriate time-slot as defined by the initial frame-sync signal.

REGISTER ADDRESS				R/W	RES	DATA FIELD									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: Bit 15 = MSB

Figure <ContPortMap>

REGISTER ADDRESS				R/W	RES	DATA FIELD									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0			Power Settings									
0	0	0	1			Clock Dividers									
0	0	1	0			Serial Port Control									
0	0	1	1			Mute Control									
0	1	0	0			Input/Output Configuration									
0	1	0	1	0		ADC0 Gain Setting									
0	1	0	1	1		ADC0 Peak Level									
0	1	1	0	0		ADC1 Gain Setting									
0	1	1	0	1		ADC1 Peak Level									
0	1	1	1			Reserved									
1	0	0	0			Reserved									
1	0	0	1			I/O Filter Select									
1	0	1	0			DAC0 Gain Setting									
1	0	1	1			DAC1 Gain Setting									
1	1	0	0			Reserved									
1	1	0	1			Reserved									
1	1	1	0			REF Trim Control									
1	1	1	1			Test Mode Control									

Figure <ContRegMap>

REG ADDRESS	R/W	RES	Power Control									
			RESET	PURA	PUR	PUD1	PUD0	PUA3	PUA2	PUA1	PUA0	PU
15 - 12	11	10	9	8	7	6	5	4	3	2	1	0
0000			Software Reset	Power Up Reference Amplifier	Power Up Reference	Power Up DAC1	Power Up DAC0	Power Up ADC3	Power Up ADC2	Power Up ADC1	Power Up ADC0	Global Power Up

Table <MCLK_Divider>

REG ADDRESS	R/W	RES	Clock Dividers									
			Reserved				BCD2-0			MCD2-0		
15 - 12	11	10	9	8	7	6	5	4	3	2	1	0
0000							Bit Clock Divider			Master Clock Divider		

REG ADDRESS	R/W	RES	Serial Interface Control									
			DSTD-ME	TPOS2	TPOS1	TPOS0	DDF1	DDF0	ADF1	ADF0	DSMM	DSMS
15 - 12	11	10	9	8	7	6	5	4	3	2	1	0
0000			TDM Mode Enable	TDM Mode Position 2	TDM Mode Position 1	TDM Mode Position 0	DAC Data Format 2	DAC Data Format 2	ADC Data Format 2	ADC Data Format 1	Mixed-- Mode Enable	Master/ Slave Mode

REG ADDRESS	R/W	RES	Mute Control									
			DWW1	DWW0	AWW1	AWW0	DMU-TE1	DMU-TE0	-	-	AMU-TE1	AMU-TE0
15 - 12	11	10	9	8	7	6	5	4	3	2	1	0
0000			DAC Word Width 1	DAC Word Width 0	ADC Word Width 1	ADC Word Width 0	Mute DAC 1	Mute DAC 0	Reserved	Reserved	Mute ADC 1	Mute ADC 0

REG ADDRESS	R/W	RES	ADC Configuration									
			PEAKE	RES	DLB	DSLB	ALB1	ALB0	INV1	INV0	SEE1	SEE0
15 - 12	11	10	9	8	7	6	5	4	3	2	1	0
0111			ADC Peak Level Reading	Reserved	Digital Loopback	Data SPORT Loopback	Analog Loopback Ch1	Analog Loopback Ch0	Invert ADC1 Inputs	Invert ADC0 Inputs	ADC1 in Single Ended Mode	ADC0 in Single Ended Mode

REG ADDRESS	R/W	RES	ADC0 Gain Setting/Peak Readback									
			A0G9-0									
15 - 12	11	10	9	8	7	6	5	4	3	2	1	0
0001	0		Reserved								A0G1	A0G0
	1		A0P9				ADC0 Peak Readback					A0P0

REG ADDRESS	R/W	RES	ADC1 Gain Setting/Peak Readback									
			A1G9-0									
15 - 12	11	10	9	8	7	6	5	4	3	2	1	0
0001	0		Reserved								A1G1	A1G0
	1		A1P9				ADC1 Peak Readback					A0P0

REG ADDRESS	R/W	RES	DAC0 Gain Setting									
			D0G9-0									
15 - 12	11	10	9	8	7	6	5	4	3	2	1	0
0101			D0G9				DAC0 Gain Setting					D0G0

REG ADDRESS	R/W	RES	DAC1 Gain Setting									
			D1G9-0									
15 - 12	11	10	9	8	7	6	5	4	3	2	1	0
0110			D1G9	DAC1 Gain Setting								D1G0

REG ADDRESS	R/W	RES	Trim Control									
			BMF	LTE	LT3-0				ST3-0			
15 - 12	11	10	9	8	7	6	5	4	3	2	1	0
0000			Blow Master Fuse	Link Trim Enable	Link Trim				Software Trim			

REG ADDRESS	R/W	RES	Test Mode Control									
			TME1-0		DI3-0				AI3-0			
15 - 12	11	10	9	8	7	6	5	4	3	2	1	0
0000			Test Mode Control		DAC Current Settings				ADC Current Settings			

OUTLINE DIMENSIONS (STYLE: outline hd)

Dimensions shown in inches and (mm). (STYLE: outline sub)