
Features

- Incorporates the ARM7TDMI™ ARM Thumb processor
 - High-performance 32-bit RISC architecture
 - High-density 16-bit instruction set
 - Leader in MIPS/Watt
 - Embedded ICE In Circuit Emulation
- 4K bytes internal RAM
- Fully programmable External Bus Interface (EBI)
 - Maximum external address space of 64M bytes
 - Up to eight chip selects
 - Software programmable 8/16-bit external databus
- Eight-level priority, individually maskable, vectored interrupt controller
 - Four External interrupts, including a high priority low latency interrupt request
- 32 Programmable I/O lines
- Three-channel 16-bit timer/counter
 - Three external clock inputs
 - Two multi-purpose I/O pins per channel
- Two USARTs
 - Two dedicated Peripheral Data Controller (PDC) channels per USART
- Programmable watchdog timer
- Low-power idle and power-down modes
- Fully static operation: 0 Hz to 33 MHz
- 2.7V to 3.6V operating range
- Available in a 100-lead TQFP package

Description

The AT91M40400 is a member of the Atmel AT91 16/32-bit Microcontroller family which is based on the ARM7TDMI embedded processor. This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications. The AT91 ARM-based MCU family also features Atmel's high-density, nonvolatile memory technology. The on-chip Flash program memory is in-system programmable.

The AT91M40400 has a direct connection to off-chip memory, including Flash, through the External Bus Interface.

The device is manufactured using Atmel's high-density CMOS technology. By combining the ARM7TDMI microcontroller core with an on-chip RAM and a wide range of peripheral functions on a monolithic chip, the Atmel AT91M40400 is a powerful microcontroller that provides a flexible, cost-effective solution to many compute-intensive embedded control applications.



16/32-Bit Microcontroller

AT91M40400

Summary

Full datasheet (lit# 0768B)
also available by e-mailing
literature@atmel.com





Pin Configuration

Figure 1. AT91M40400 Pinout (Top View)

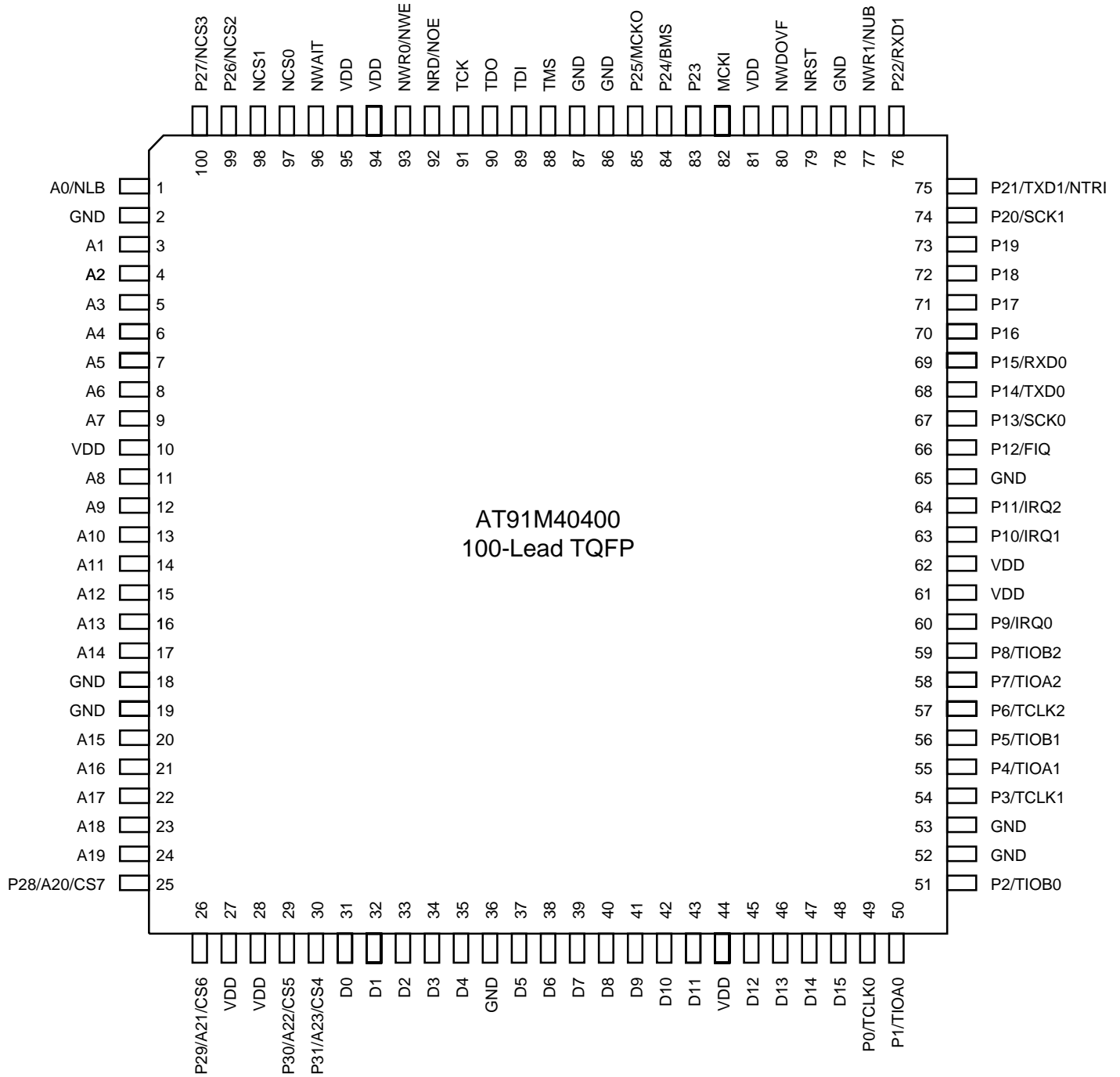
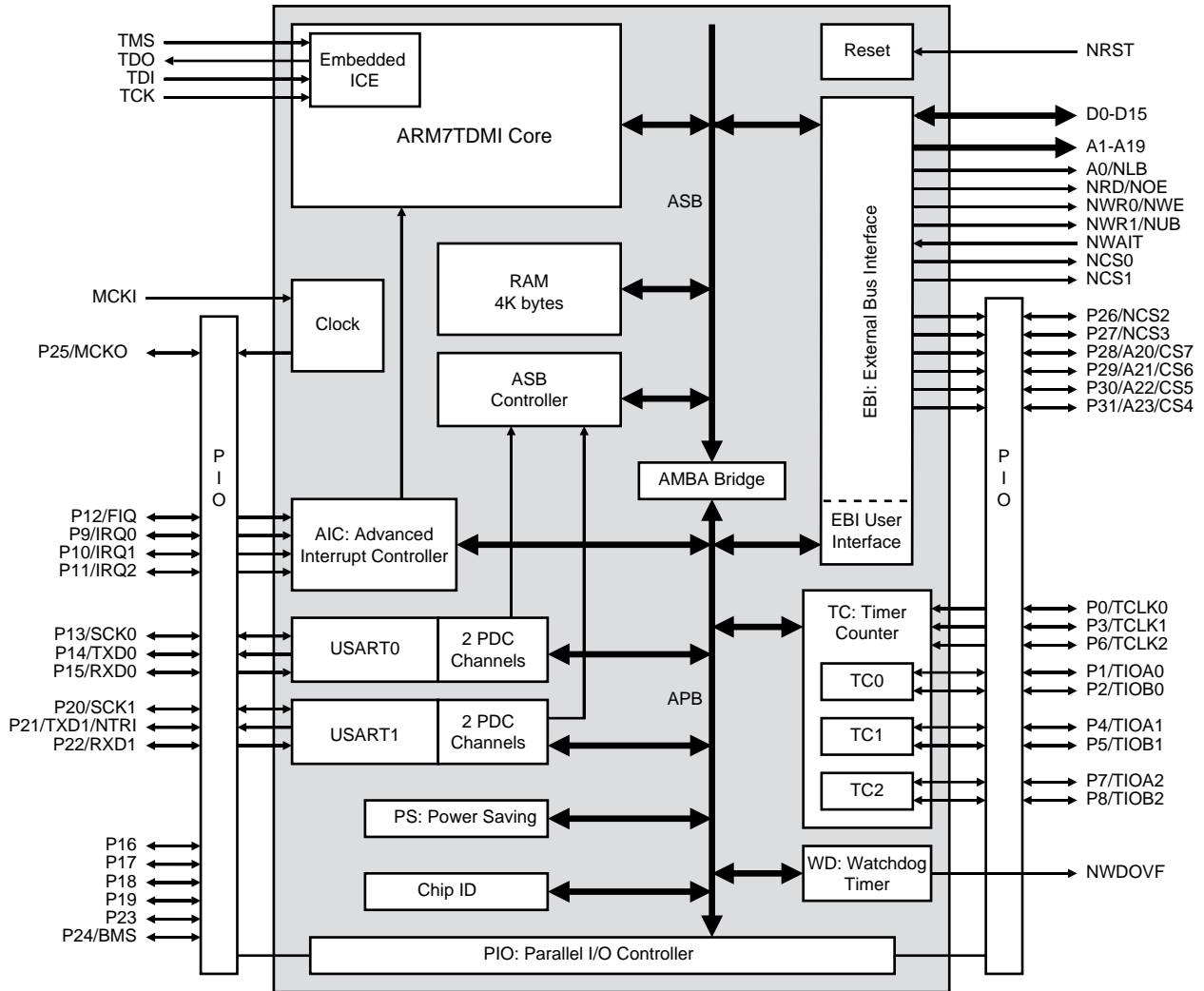


Table 1. AT91M40400 Pin Description

| Module | Name | Function | Type | Active Level | Comments |
|--------|-------------|------------------------------|--------|--------------|-----------------------------------|
| EBI | A0-A23 | Address Bus | Output | -- | All valid after reset |
| | D0-D15 | Data Bus | I/O | -- | |
| | NCS0-NCS3 | Chip Select | Output | low | |
| | CS4-CS7 | Chip Select | Output | high | A23-A20 after reset |
| | NWR0 | Lower Byte 0 Write Signal | Output | low | Used in Byte Write Option |
| | NWR1 | Upper Byte 1 Write Signal | Output | low | Used in Byte Write Option |
| | NRD | Read Signal | Output | low | Used in Byte Write Option |
| | NWE | Write Enable | Output | low | Used in Byte Select Option |
| | NOE | Output Enable | Output | low | Used in Byte Select Option |
| | NUB | Upper Byte Select | Output | low | Used in Byte Select Option |
| | NLB | Lower Byte Select | Output | low | Used in Byte Select Option |
| | NWAIT | Wait Input | Input | low | |
| | BMS | Boot Mode Select | Input | -- | Sampled during reset |
| AIC | FIQ | Fast Interrupt Request | Input | -- | PIO controlled after reset |
| | IRQ0-IRQ2 | External Interrupt Request | Input | -- | PIO controlled after reset |
| Timer | TCLK0-TCLK2 | Timer External Clock | Input | -- | PIO controlled after reset |
| | TIOA0-TIOA2 | Multipurpose Timer I/O pin A | I/O | -- | PIO controlled after reset |
| | TIOB0-TIOB2 | Multipurpose Timer I/O pin B | I/O | -- | PIO controlled after reset |
| USART | SCK0-SCK1 | External Serial Clock | I/O | -- | PIO controlled after reset |
| | TXD0-TXD1 | Transmit Data Output | Output | -- | PIO controlled after reset |
| | RXD0-RXD1 | Receive Data Input | Input | -- | PIO controlled after reset |
| PIO | P0-P31 | Parallel IO line | I/O | -- | |
| WD | NWDOVF | Watchdog overflow | Output | low | Open drain |
| Clock | MCKI | Master Clock Input | Input | -- | Schmidt trigger |
| | MCKO | Master Clock Output | Output | -- | |
| Reset | NRST | Hardware Reset Input | Input | low | Schmidt trigger, internal pull-up |
| | NTRI | Tristate Mode Select | Input | low | Sampled during reset |
| ICE | TMS | Test Mode Select | Input | -- | Schmidt trigger, internal pull-up |
| | TDI | Test Data Input | Input | -- | Schmidt trigger, internal pull-up |
| | TDO | Test Data Output | Output | -- | |
| | TCK | Test Clock | Input | -- | Schmidt trigger, internal pull-up |
| Power | VDD | Power | | | |
| | GND | Ground | | | |

Block Diagram

Figure 2. AT91M40400 Block Diagram



Architectural Overview

The AT91M40400 architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). The ASB is designed for maximum performance. It interfaces the processor with the on-chip 32-bit memories and the external memories and devices by means of the External Bus Interface (EBI). The APB is designed for accesses to on-chip peripherals and is optimized for low power consumption. The AMBA Bridge provides an interface between the ASB and the APB.

An on-chip Peripheral Data Controller (PDC) transfers data between the on-chip USARTs and the on and off-chip memories without processor intervention. Most importantly, the PDC removes the processor interrupt handling overhead and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64k contiguous bytes without reprogramming the starting address. As a result, the performance of the microcontroller is increased and the power consumption reduced.

The AT91M40400 peripherals are designed to be programmed with a minimum number of instructions. Each peripheral has a 16K byte address space allocated in the upper 3M bytes of the 4G byte address space. Except for the interrupt controller, the peripheral base address is the lowest address of its memory space. The peripheral register set is composed of control, mode, data, status and interrupt registers.

To maximize the efficiency of bit manipulation, frequently written registers are mapped into three memory locations. The first address is used to set the individual register bits, the second resets the bits and the third address reads the value stored in the register. A bit can be set or reset by writing a one to the corresponding position at the appropriate address. Writing a zero has no effect. Individual bits can

thus be modified without having to use costly read-modify-write and complex bit manipulation instructions.

All of the external signals of the on-chip peripherals are under the control of the Parallel I/O controller. The PIO controller can be programmed to insert an input filter on each pin or generate an interrupt on a signal change. After reset, the user must carefully program the PIO Controller in order to define which peripheral signals are connected with off-chip logic.

The ARM7TDMI processor operates in little-endian mode in the AT91M40400 microcontroller. The processor's internal architecture and the ARM and Thumb instruction sets are described in the ARM7TDMI Datasheet. The on-chip peripherals are described in the subsequent sections of this datasheet. Electrical characteristics are documented in a separate datasheet entitled "AT91M40400 Electrical and Mechanical Characteristics".

The ARM Standard In-Circuit-Emulation debug interface is supported via the ICE port of the AT91M40400 microcontroller. (This is not a standard IEEE 1149.1 JTAG Boundary Scan interface)

PDC: Peripheral Data Controller

The AT91M40400 has a 4-channel PDC dedicated to the two on-chip USARTs. One PDC channel is connected to the receiving channel and one to the transmitting channel of each USART.

The user interface of a PDC channel is integrated in the memory space of each USART channel. It contains a 32-bit address pointer register (US_RPR or US_TPR) and a 16-bit byte count register (US_RCR or US_TCR). When the programmed number of bytes are transferred, an end of transfer interrupt is generated by the corresponding USART.

EBI: External Bus Interface

The EBI generates the signals which control the access to the external memory or peripheral devices. The EBI is fully programmable and can address up to 64M bytes. It has eight chip selects and a 24-bit address bus, the upper four bits of which are multiplexed with a chip select.

The 16-bit data bus can be configured to interface with 8- or 16-bit external devices. Separate read and write control signals allow for direct memory and peripheral interfacing.

The EBI supports different access protocols allowing single clock cycle memory accesses.

The main features are:

- External Memory Mapping
- Up to 8 chip select lines
- 8- or 16-bit data bus
- Byte write or byte select lines
- Remap of boot memory
- Two different read protocols
- Programmable wait state generation
- External wait request
- Programmable data float time

AIC: Advanced Interrupt Controller

The AT91 has an 8-level priority, individually maskable, vectored interrupt controller. This feature substantially reduces the software and real time overhead in handling internal and external interrupts.

The interrupt controller is connected to the NFIQ (fast interrupt request) and the NIRQ (standard interrupt request) inputs of the ARM7TDMI processor. The processor's NFIQ line can only be asserted by the external fast interrupt request input: FIQ. The NIRQ line can be asserted by the interrupts generated by the on-chip peripherals and the external interrupt request lines: IRQ0 to IRQ2.

An 8-level priority encoder allows the customer to define the priority between the different NIRQ interrupt sources.

Internal sources are programmed to be level sensitive or edge triggered. External sources can be programmed to be positive or negative edge triggered or high or low level sensitive.

PIO: Parallel I/O Controller

The AT91M40400 has 32 programmable I/O lines. Six pins on the AT91M40400 are dedicated as general purpose I/O pins (P16, P17, P18, P19, P23 and P24). Other I/O lines are multiplexed with an external signal of a peripheral to optimize the use of available package pins. The PIO controller enables generation of an interrupt on input change and insertion of a simple input glitch filter on any of the PIO pins.

USART: Universal Synchronous/Asynchronous Receiver/Transmitter

The AT91 provides two identical, full-duplex, universal synchronous/asynchronous receiver/transmitters that interface to the APB and are connected to the Peripheral Data Controller.

The main features are:

- Programmable Baud Rate Generator
- Parity, Framing and Overrun Error Detection
- Line Break Generation and Detection
- Automatic Echo, Local Loopback and Remote Loopback channel modes
- Multi-drop Mode: Address Detection and Generation
- Interrupt Generation
- Two Dedicated Peripheral Data Controller channels
- 5-, 6-, 7- and 8-bit character length

TC: Timer Counter

The AT91M40400 features a Timer Counter block which includes three identical 16-bit timer counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

Each Timer Counter channel has 3 external clock inputs, 5 internal clock inputs, and 2 multi-purpose input/output signals which can be configured by the user. Each channel drives an internal interrupt signal which can be programmed to generate processor interrupts via the AIC (Advanced Interrupt Controller).

The Timer Counter block has two global registers which act upon all three TC channels. The Block Control Register allows the three channels to be started simultaneously with the same instruction. The Block Mode Register defines the external clock inputs for each Timer Counter channel, allowing them to be chained.

WD: Watchdog Timer

The AT91 series microcontrollers have an internal watchdog timer which can be used to prevent system lock-up if the software becomes trapped in a deadlock.

PS: Power Saving

The AT91M40400 Power Saving module provides a low-power Idle Mode. In Idle Mode, the CPU clock is deactivated while all on-chip peripherals and the RAM remain active. The contents of the on-chip RAM and all the special function registers remain unchanged during this mode. The Idle Mode can be terminated by any enabled interrupt or by a hardware Reset.

SF: Special Function

The AT91M40400 provides registers which implement the following special functions.

- Chip identification
- RESET status