HA12220F

CD-ROM Drive Head Amplifier IC

HITACHI

ADE-207-230 (Z)

Target Specification
1st. Edition
April 1997

Functions

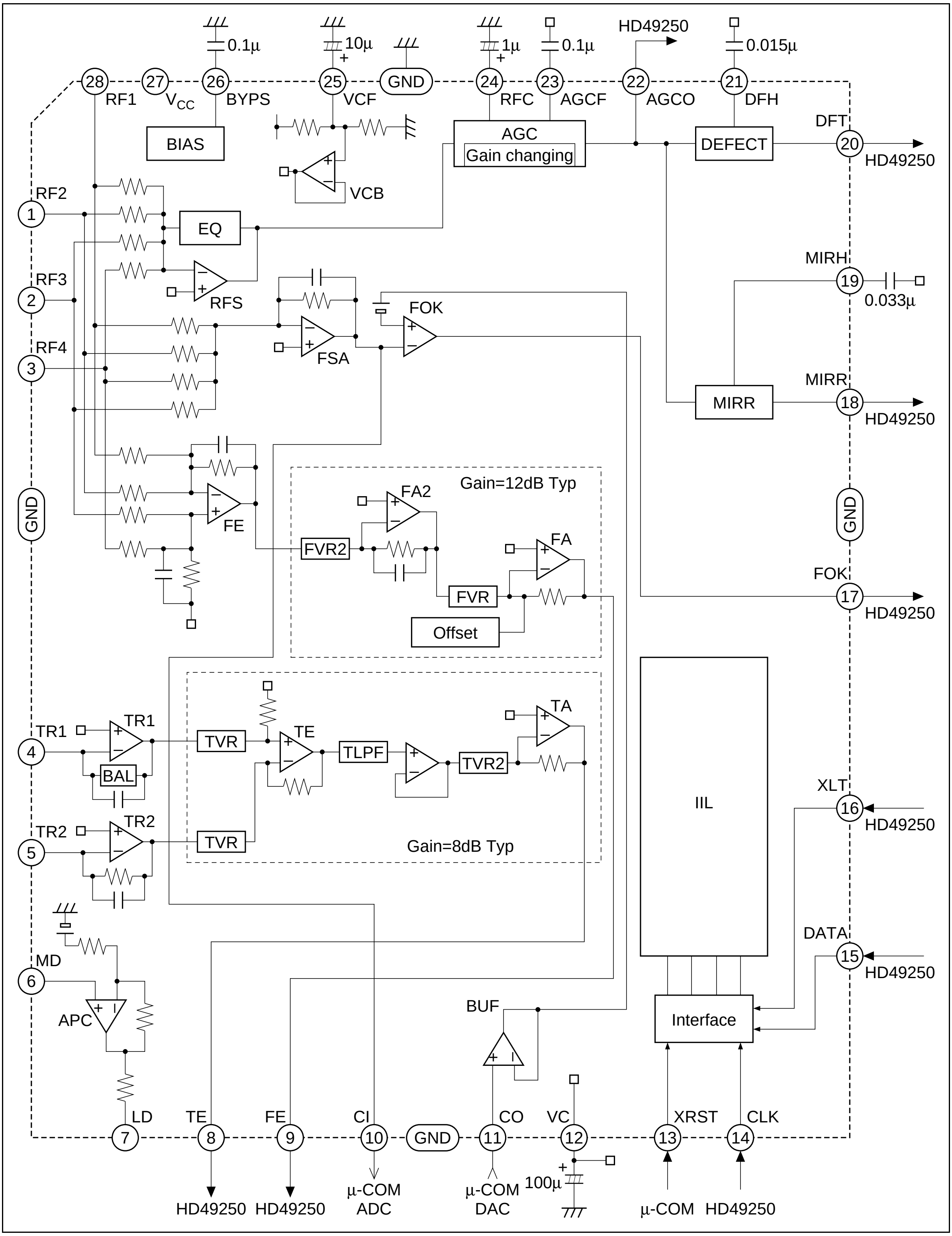
- RF amplifier (Built-in equalizer changing circuit)
- Focus error amplifier (fc = 60kHz Typ)
- Tracking error amplifier (Built-in cut-off frequency changing circuit fc = 30kHz, 60kHz, 100kHz, 200kHz Typ)
- FOK detection circuit (Built-in Vth changing circuit)
- Mirror detection circuit
- Defect detection circuit
- APC amplifier
- RFAGC amplifier

Features

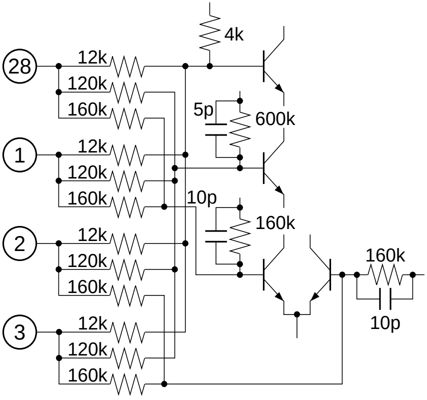
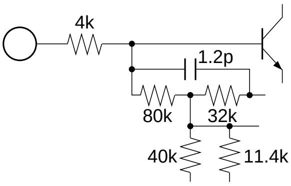
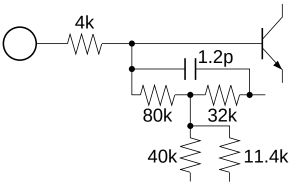
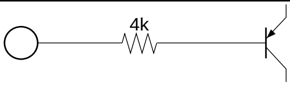
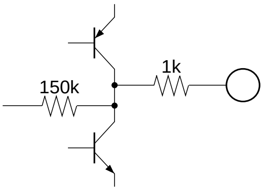
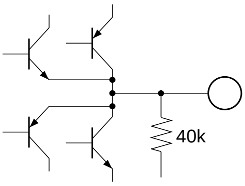
- Built-in variable resistors (+14 to –16% 2% steps) for adjusting tracking error EF balance
- Built-in variable resistors (–8 to +8dB 4dB steps) for rough adjusting tracking gain
- Built-in variable resistors (–8 to +8dB 4dB steps) for rough adjusting focus gain
- Built-in focus offset insertion circuit (–0.7 to +0.7V in 0.1V steps)
- RF amplifier frequency characteristics 30MHz (–3dB) in case of peaking off
- High-speed access support (The mirror circuit internal time constant can be switched between normal, 4× and 8× modes.)
- Support for CD-RW playback
- Few external components
- Available to set the stand-by mode
- FP-28TB package

Hitachi
semiconductor

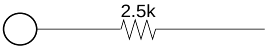
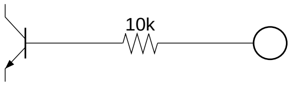
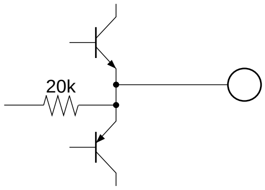
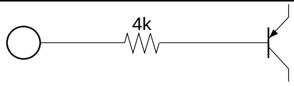
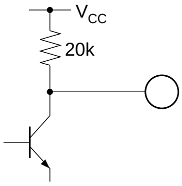
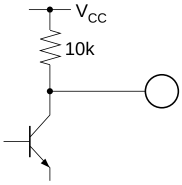
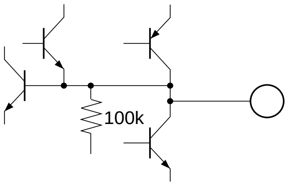
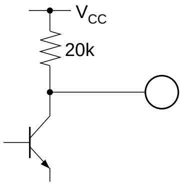
Block Diagram


0.1µ
10µ
1µ
0.1µ
HD49250
0.015µ
28 RF1
27 VCC
26 BYPS
25 VCF
GND
24 RFC
23 AGCF
22 AGCO
21 DFH
BIAS
AGC
Gain changing
DEFECT
DFT 20 HD49250
VCB
RF2 1
EQ
RFS
RF3 2
FSA
FOK
MIRH 19 0.033µ
RF4 3
MIRR
MIRR 18 HD49250
FE
Gain=12dB Typ
FA2
FA
FVR2
FVR
Offset
GND
GND
FOK 17 HD49250
IIL
TR1 4
TR1
BAL
TVR
TE
TLPF
TVR2
TA
TR2 5
TR2
TVR
Gain=8dB Typ
XLT 16 HD49250
DATA 15 HD49250
MD 6
APC
BUF
Interface
LD 7
TE 8 HD49250
FE 9 HD49250
CI 10 µ-COM ADC
GND
CO 11 µ-COM DAC
VC 12 100µ
XRST 13 µ-COM
CLK 14 HD49250

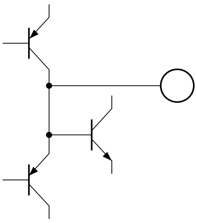
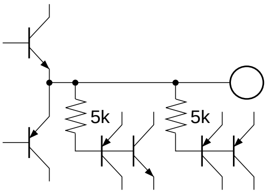
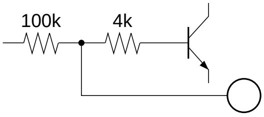
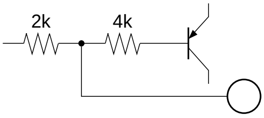
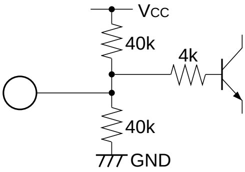
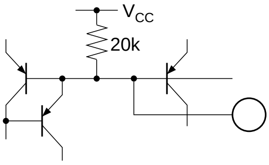
Pin Description and Equivalent Circuit

Pin No.	Pin Name	Equivalent Circuit	Function
1	RF2	 28 1 2 3 12k 120k 160k 4k 5p 600k 10p 160k 160k 10p	RF FE FSA amplifier input2
2	RF3		RF FE FSA amplifier input3
3	RF4		RF FE FSA amplifier input4
28	RF1		RF FE FSA amplifier input1
4	TR1	 4k 1.2p 80k 32k 40k 11.4k	TR1 amplifier input
5	TR2	 4k 1.2p 80k 32k 40k 11.4k	TR2 amplifier input
6	MD		APC amplifier input
7	LD		APC amplifier output
8	TE		Tracking error signal output
9	FE		Focus error signal output

Pin Description and Equivalent Circuit (cont)

Pin No.	Pin Name	Equivalent Circuit	Function
10	CI		FSA amplifier output monitor
11	CO		Setting FOK reference voltage
12	VC		Reference voltage output
13	XRST		Reset input
14	CLK		Serial data synchronous clock input
15	DATA		Serial data input
16	XLT		Serial data latch input
17	FOK		FOK detection signal output
18	MIRR		Mirror detection signal output
19	MIRH		Mirror envelope hold signal output
20	DFT		Defect detection signal output

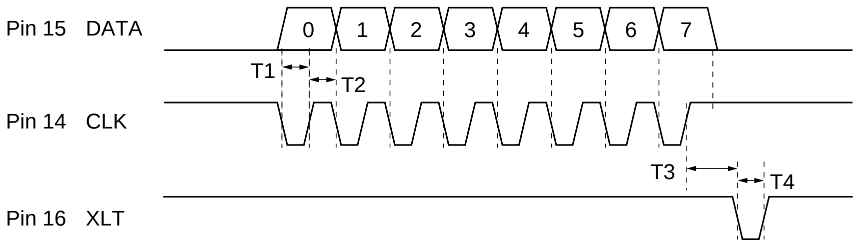
Pin Description and Equivalent Circuit (cont)

Pin No.	Pin Name	Equivalent Circuit	Function
21	DFH		Defect envelope hold signal output
22	AGCO		AGC amplifier output
23	AGCF		Capacitor connection for AGC
24	RFC		Capacitor connection for AGC
25	VCF		Capacitor connection for reference voltage ripple filter
26	BYPS		Capacitor connection for ripple filter
27	V_{CC}	—	V_{CC}

Operation

Control by Serial Data

The IC's internal switches can be operated by sending control data from the HD49250.
The signal timing is shown in figure 1, and the control commands are listed in table 1 and 2.



Item	Symbol	Min	Typ	Max	Unit
Clock frequency	f_{CLK}	—	—	520	kHz
Clock pulse width	T1, T2	0.96	—	—	µs
Delay time	T3	1	—	—	µs
Latch pulse width	T4	2	—	—	µs

Figure 1 Timing Diagram for Serial Data Control

Signals from the HD49250 are input at pins 14 to 16. Pin13 is connected to the microcomputer.
A low input at the XRST pin resets the IC. Normally this pin should be kept high.

The serial data from the HD49250 switches the following settings.

1. Tracking error EF balance
2. Focus offset
3. Tracking gain, Focus gain
4. FOK Vth
5. Mirror circuit, defect circuit normal speed / 4× speed / 8× speed mode
6. Tracking error cut-off frequency
7. APC amplifier ON/OFF
8. RF equalizer
9. Stand-by mode (cleared by setting XRST on)

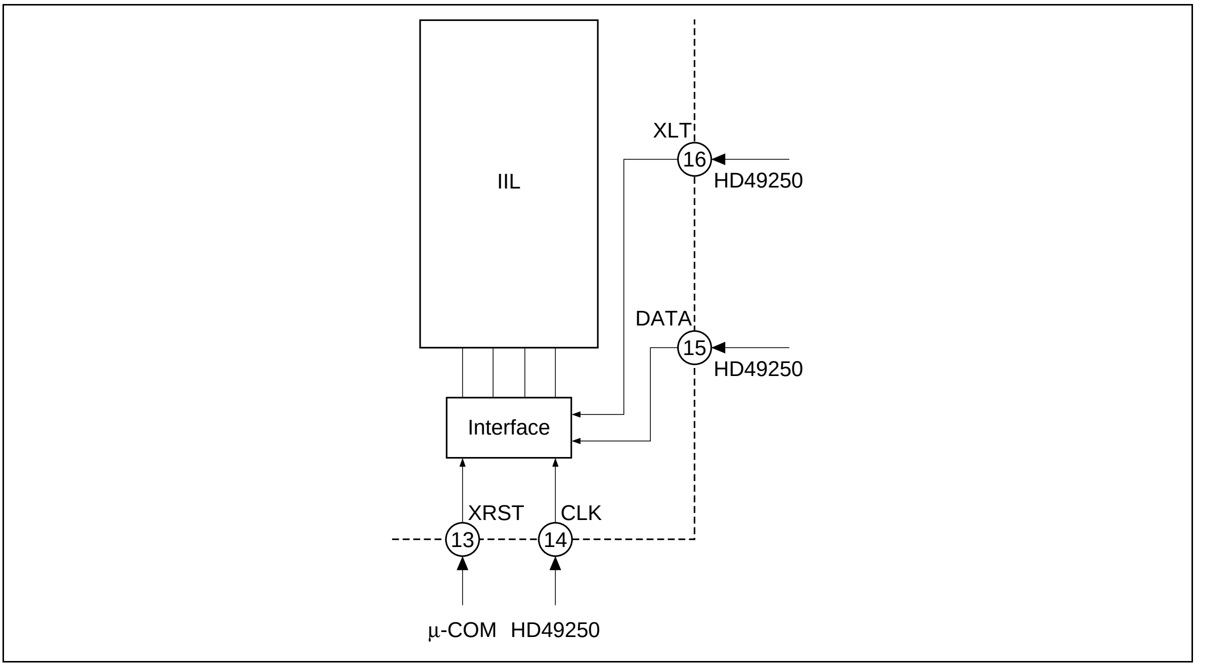

IIL
XLT
16
HD49250
DATA
15
HD49250
Interface
XRST
CLK
13
14
µ-COM
HD49250

Figure 2 Serial Data Control

Table 1 Serial Data Control Command 1

	DATA								Note
	D7	D6	D5	D4	D3	D2	D1	D0	
Focus error gain CD-RW	0	0	0	CD-RW *1	Focus error gain			0	
Focus error offset	0	0	1					0	
Variable resistor BAL for tracking error EF balance	0	1	0					0	

Focus error gain:

D3	D2	D1	Gain (dB)
0	0	0	0
0	1	1	–4
0	1	0	–8
1	0	1	+7.9
1	1	0	+4.3

Focus error offset:

D4	D3	D2	D1	Offset (V)
1	1	1	1	+0.7
	1	1	0	+0.6
	1	0	1	+0.5
	1	0	0	+0.4
	0	1	1	+0.3
	0	1	0	+0.2
	0	0	1	+0.1
0	0	0	0	±0
	0	0	1	–0.1
	0	1	0	–0.2
	0	1	1	–0.3
	1	0	0	–0.4
	1	0	1	–0.5
	1	1	0	–0.6
	1	1	1	–0.7

Variable resistor BAL for tracking error EF balance:

D4	D3	D2	D1	BAL	Ratio
1	0	0	0	336kΩ	–16%
1	0	0	1	344kΩ	–14%
1	0	1	0	352kΩ	–12%
1	0	1	1	360kΩ	–10%
1	1	0	0	368kΩ	–8%
1	1	0	1	376kΩ	–6%
1	1	1	0	384kΩ	–4%
1	1	1	1	392kΩ	–2%
0	0	0	0	400kΩ	±0%
0	0	0	1	408kΩ	+2%
0	0	1	0	416kΩ	+4%
0	0	1	1	424kΩ	+6%
0	1	0	0	432kΩ	+8%
0	1	0	1	440kΩ	+10%
0	1	1	0	448kΩ	+12%
0	1	1	1	456kΩ	+14%

Note: 1. Both tracking error and focus error gains are increased by 12dB. The RFAGC block gain is also increased by 12dB.

Table 2 Serial Data Control Command 2

<table>
<tr><th rowspan="2"></th><th colspan="8">DATA</th><th rowspan="2">Note</th></tr>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>Tracking error gain</td><td>1</td><td>0</td><td>0</td><td>—</td><td colspan="3">Tracking error gain
<table>
<tr><th>D3</th><th>D2</th><th>D1</th><th>Gain (dB)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>–4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>–8</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>+7.9</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>+4.3</td></tr>
</table></td><td>0</td><td></td></tr>
<tr><td>Tracking error filter
Mirror
Defect</td><td>1</td><td>0</td><td>1</td><td colspan="4">
<table>
<tr><th colspan="3">Mirror, Defect *1</th></tr>
<tr><th>D3</th><th>D2</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal</td></tr>
<tr><td>0</td><td>1</td><td>4×</td></tr>
<tr><td>1</td><td>1</td><td>8×</td></tr>
</table>
Tracking error filter
<table>
<tr><th>D4</th><th>D1</th><th></th></tr>
<tr><td>1</td><td>1</td><td>30kHz</td></tr>
<tr><td>0</td><td>1</td><td>60kHz</td></tr>
<tr><td>1</td><td>0</td><td>100kHz</td></tr>
<tr><td>0</td><td>0</td><td>200kHz</td></tr>
</table></td><td>0</td><td></td></tr>
<tr><td>APC ON
FOK Vth
Stand-by</td><td>1</td><td>1</td><td>0</td><td colspan="2">
<table>
<tr><th colspan="3">FOK Vth</th></tr>
<tr><th>D4</th><th>D3</th><th>Vth</th></tr>
<tr><td>1</td><td>1</td><td>–12dB</td></tr>
<tr><td>0</td><td>1</td><td>–6dB</td></tr>
<tr><td>0</td><td>0</td><td>0dB</td></tr>
<tr><td>1</td><td>0</td><td>Prohibit</td></tr>
</table></td><td>Stand-by ON</td><td>APC ON</td><td>0</td><td>Stand-by mode is cleared by setting XRST on.</td></tr>
<tr><td>RFEQ</td><td>1</td><td>1</td><td>1</td><td>SC4</td><td>SC3</td><td>SC2</td><td>SC1</td><td>0</td><td>*2</td></tr>
</table>

Note: 1. Switches the mirror circuit and the defect circuit internal time constants at the same time. Don’t use D3 = “1”, D2 = “0” mode.

2. The switch name surrouded by circle means that the switch turns on when the corresponding bit is “1”. This switch changes the value of the RF peaking capacitor. In case of peaking off all switches must be set off.

RF Amplifiers

The output from PDIC is summed by RFS amplifier.
Figure 4 shows the equivalent circuit for the EQ block in figure 3. The peaking characteristics can be changed with 4-bit data from the HD49250.
On resistance of SC1 to SC4 are 600Ω Typ.

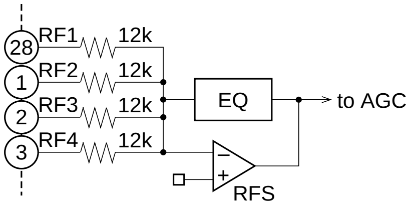

28
RF1
12k
1
RF2
12k
2
RF3
12k
3
RF4
12k
EQ
to AGC
−
+
RFS

Figure 3 RFS Amplifier

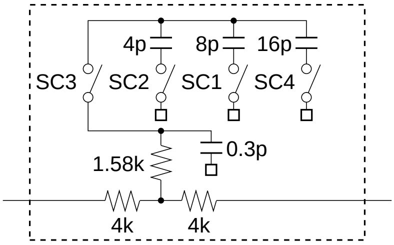

4p
8p
16p
SC3
SC2
SC1
SC4
0.3p
1.58k
4k
4k

Figure 4 RFS Amplifier Equalizer Equivalent Circuit

The RFS amplifier output is input to the AGC amplifier internally in the IC.
Pin 24 is used to connect the capacitor that sets cut-off frequency of high-pass filter between the RFS amplifier and the AGC amplifier. The cut-off frequency will typically be 80Hz with the external constants shown in figure 5.
The RF signal is rectified by an internal resistor and an external capacitor connected to pin 23.
The pins 28, 1, 2, and 3 expect an input level of about 0.1Vpp. The AGC amplifier output (pin 22) will have an amplitude of 1.2Vpp Typ.
When CD-RW mode is set by 1-bit data from the HD49250, the AGC amplifier gain is increased by 12dB. This allows the IC to output a 1.2Vpp Typ amplitude even during CD-RW playback.

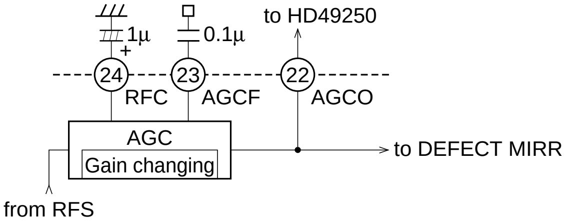

1µ
+
0.1µ
to HD49250
24
23
22
RFC
AGCF
AGCO
AGC
Gain changing
to DEFECT MIRR
from RFS

Figure 5 AGC Amplifier

FOK Detection Circuit

This detector is a comparator that generates the FOK signal. FOK is one of the signals that activate the focus servo.
The FSA amplifier (fc = 53kHz Typ) summes the output from the PDIC. When this output signal becomes lower than the reference voltage by Vth, pin 17 goes high. This Vth can be set by 2-bit data from the HD49250.
Vth is set to 0.8V (0dB) after a reset.
Using µ-com ADC & DAC the voltage of pin 11 had better be set the same voltage as the voltage of pin 10 before focus searching in order to reduce the effect of DC offset voltage at FSA amplifier output.

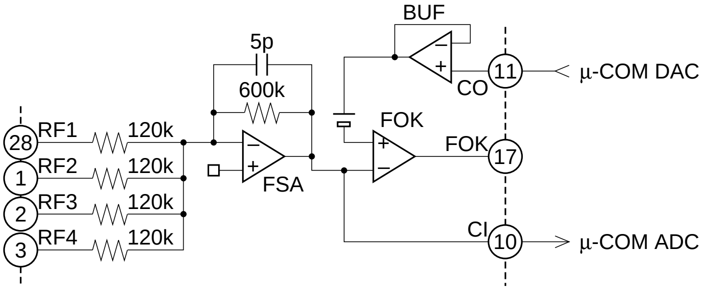

BUF
5p
600k
RF1
120k
RF2
120k
RF3
120k
RF4
120k
28
1
2
3
FSA
FOK
CO
11
µ-COM DAC
FOK
17
CI
10
µ-COM ADC

Figure 6   FOK Detection

APC

This circuit is for the Psub laser diode. This circuit is turned on or off by 1-bit data from the HD49250.

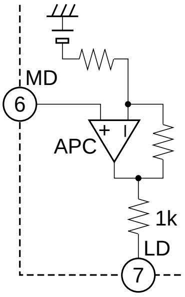

MD
6
APC
1k
LD
7

Figure 7   APC

Focus Error Amplifiers

The FE amplifier adds and subtracts the output from the PDIC.
FVR2 is a variable resistor used to increase the gain by 12dB in CD-RW mode. This variable resistor is set by 1-bit data from the HD49250.
FVR is a variable resistor that changes the focus error gain over the range –8 to +8dB in ±4dB steps. This variable resistor is set by 3-bit data from the HD49250.
An offset of between –0.7 and 0.7V (in 0.1V steps) is inserted into the focus error signal. This is set by 4-bit data from the HD49250. The FE output cut-off frequency (fc) is 60kHz Typ.

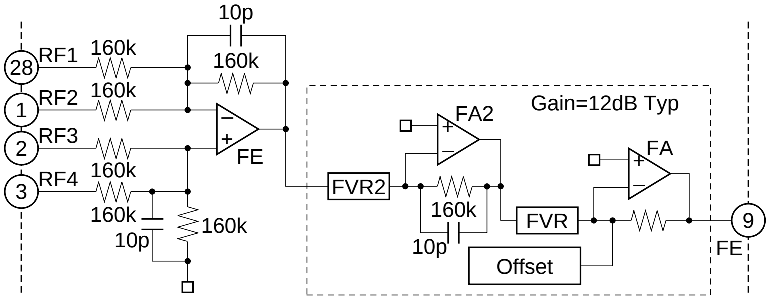

10p
RF1
160k
160k
28
RF2
160k
1
RF3
2
160k
RF4
3
160k
10p
160k
FE
FA2
Gain=12dB Typ
FA
FVR2
160k
10p
FVR
Offset
9
FE

Figure 8 Focus Error Amplifiers

Defect Detection Circuit

When a scratched disc is played, the EFM RF signal has the shape shown in figure 10 (a). The defect detection circuit detects the drop-out area of this signal.

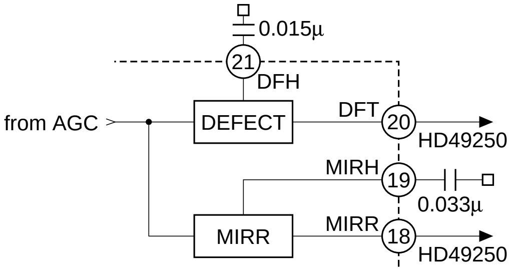

0.015µ
21
DFH
from AGC
DEFECT
DFT
20
HD49250
MIRH
19
0.033µ
MIRR
MIRR
18
HD49250

Figure 9 Mirror Detection, Defect Detection

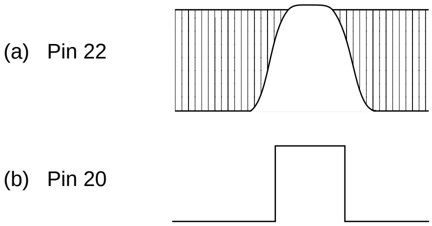


Figure 10 Defect Detection Waveform

Mirror Detection Circuit (MIRR)

As the pick-up travels across tracks, the EFM RF signal varies as in figure 11 (a). The mirror detection circuit detects the mirror region from this signal.
The external capacitor on pin 19 integrates the track-crossing frequency component.
The internal time constant of the mirror detection circuit can be set for normal, 4×, or 8× speed by 2-bit data from the HD49250, to raise the trackable range of track-crossing frequencies. The defect circuit internal time constant is also switched at the same time.

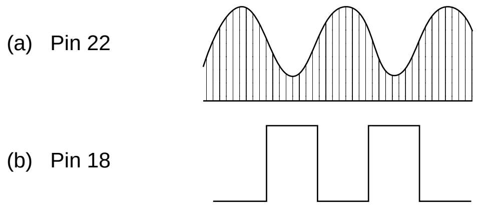


Figure 11 Mirror Detection Waveform

Tracking Error Amplifiers

The sub-beam output of PDIC is passed through a resistor and input at pins 4 and 5. External resistances of pins 4 and 5 should be set according to the pick-up so that the traverse signal at pin 8 is about 2Vpp Typ.
After a reset, the initial value of the feedback resistance BAL of TR1 amplifier is 400kΩ, the same as the feedback resistance of TR2 amplifier.
BAL has a variable resistance value that is changed by 4-bit data from the HD49250. The variability range here is from –16 to +14% in 2% steps. This resistance can be varied to adjust the EF balance of the tracking error.
TE amplifier generates the tracking error signal.
TVR is a resistor that changes the tracking gain from –8 to +8dB in 4dB steps. This is set by 3-bit data from the HD49250. TVR2 is a variable resistor used to increase the gain by 12dB in CD-RW mode. This variable resistor is set by 1-bit data from the HD49250.
TLPF switches the tracking error cut-off frequency. The TE output cut-off frequency is set to either 30, 60, 100, or 200kHz (Typ) by 2-bit data from the HD49250.

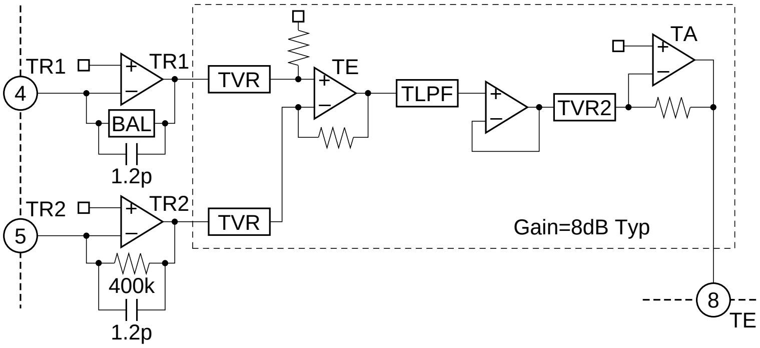


Figure 12 Tracking Error Amplifiers

Bias, Reference Voltage

Pin 26 is for a bypass capacitor to eliminate noise from the IC’s internal bias circuits.
Connect a capacitor to pin 25 to remove the ripple component from the reference voltage.
The IC’s internal reference voltage is connected internally.

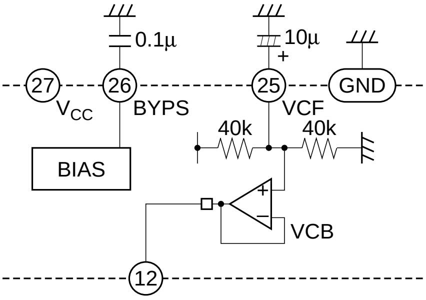

0.1μ
10μ
+
27
26
25
GND
VCC
BYPS
VCF
40k
40k
BIAS
+
−
VCB
12

Figure 13 Bias, Reference Voltage

Absolute Maximum Rating (Ta=25°C)

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	6	V
Power dissipation	P_T	400	mW
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–55 to +125	°C

Note: Recommended operating power supply voltage : 5V ± 0.5V

Electrical Characteristics (Ta = 25°C, V_{CC} = 5V)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Application Terminal
Quiescent current 1		I_{CC1}	—	20	32	mA	No signal	27
Quiescent current 2		I_{CC2}	—	0.6	1.0	mA	Stand-by mode	
Reference voltage		V_C	2.3	2.5	2.7	V	I12 ≤ ±4mA	12
Focus error amp.	Offset voltage *[1]	V_{FE}	–100	0	100	mV		9
	Max output voltage H 1	V_{FEH1}	4.2	4.5	—	V	S2, S3, S51, S9a V51 = 4V	
	Max output voltage L 1	V_{FEL1}	—	0.5	0.8	V	S1, S28, S51, S9a V51 = 4V	
	Max output voltage H 2	V_{FEH2}	3.8	4.1	—	V	S2, S3, S51, S9b V51 = 4V	
	Max output voltage L 2	V_{FEL2}	—	0.9	1.2	V	S1, S28, S51, S9b V51 = 4V	
	Voltage gain 1	G_{VFE1}	16.0	18.0	20.0	dB	S2, S3, S50 V9/VIN50	
	Voltage gain 2	G_{VFE2}	16.0	18.0	20.0	dB	S1, S28, S50 V9/VIN50	
Tracking error amp.	Offset voltage *[1]	V_{TE}	–65	0	65	mV		8
	Max output voltage H 1	V_{TEH1}	4.2	4.5	—	V	S4, S51, S8a V51 = 4V	
	Max output voltage L 1	V_{TEL1}	—	0.5	0.8	V	S5, S51, S8a V51 = 4V	
	Max output voltage H 2	V_{TEH2}	3.8	4.1	—	V	S4, S51, S8b V51 = 4V	
	Max output voltage L 2	V_{TEL2}	—	0.9	1.2	V	S5, S51, S8b V51 = 4V	
	Voltage gain 1	G_{VTE1}	5.0	8.0	11.0	dB	S4, S50 V8/VIN50	
	Voltage gain 2	G_{VTE2}	5.0	8.0	11.0	dB	S5, S50 V8/VIN50	
FOK	FOK Vth	V_{FOK}	110	160	210	mV	S28, S51 when V17 ≥ 4V Min (V51 – V12) *[2]	17
	"H" output voltage	V_{FKH}	4.7	—	—	V		
	"L" output voltage	V_{FKL}	—	—	0.4	V		

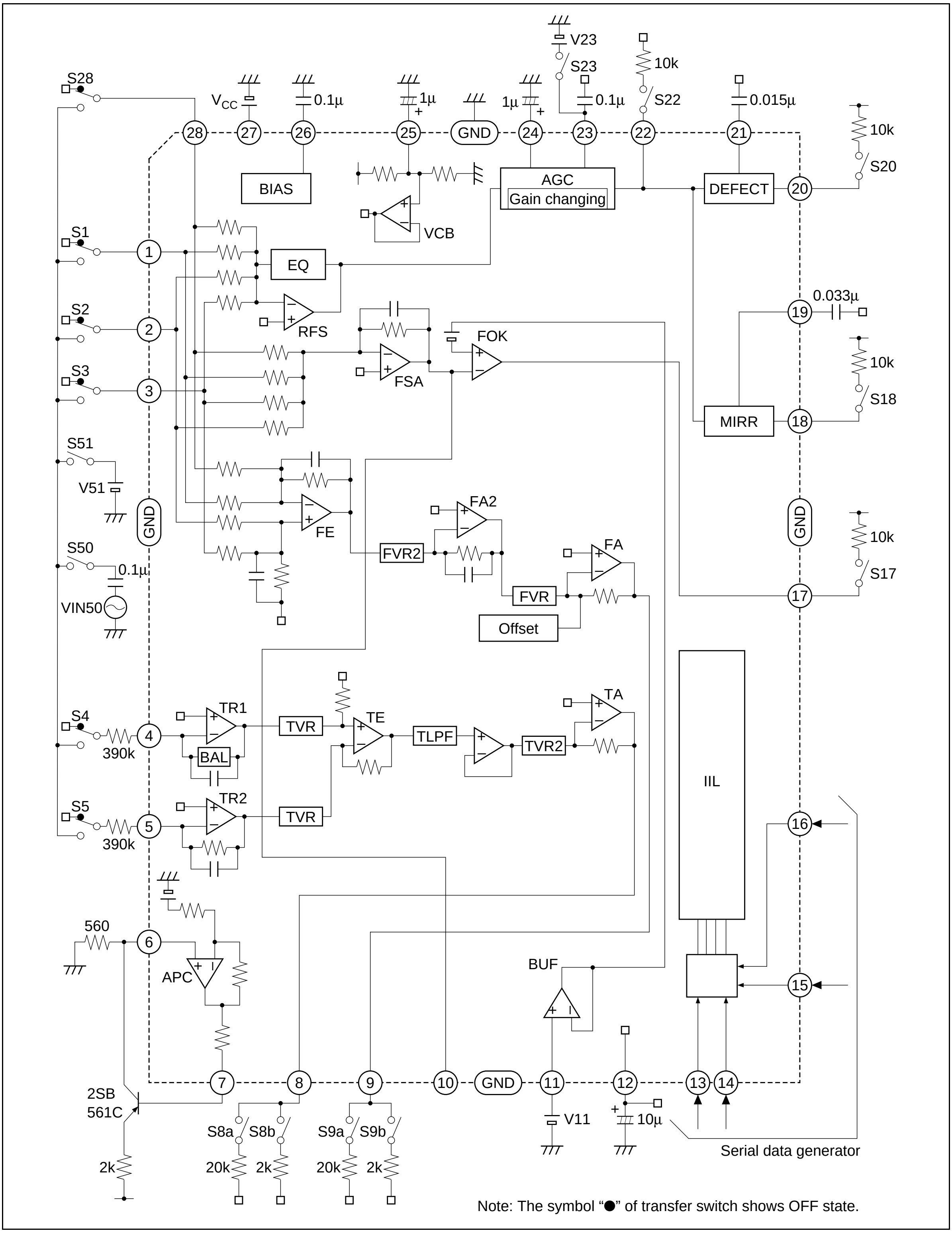
Note:
1. All offset voltages are values referring to VC (pin 12) at reset.
2. V11 = setting the same voltage as the voltage of pin 10 at no signal.

Electrical Characteristics (Ta = 25°C, V_{CC} = 5V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Application Terminal
Defect	Max operation frequency	F_{DH}	2	—	—	kHz	S28, S1, S2, S3, S50, S23	20
	Min operation frequency	F_{DL}	—	—	1	kHz		
	“H” output voltage	V_{DFH}	4.7	—	—	V		
	“L” output voltage	V_{DFL}	—	—	0.4	V		
Mirror	Max operation frequency	F_{MIR}	200	—	—	kHz	S28, S1, S2, S3, S50, S23 8× mode	18
	“H” output voltage	V_{MIH}	4.7	—	—	V		
	“L” output voltage	V_{MIL}	—	—	0.4	V		
CLK DATA XLT XRST	“H” input voltage	V_{PH}	4.0	—	—	V		13, 14, 15, 16
	“L” input voltage	V_{PL}	—	—	1.0	V		
APC	APC voltage	V_{APC}	0.09	0.16	0.23	V		6
RFAGC	Output voltage 1	V_{AGC1}	0.8	1.2	1.6	Vp-p	S28, S50, f = 200kHz 0.4Vpp ± 6dB input	22
	Output voltage 2	V_{AGC2}	0.8	1.2	1.6	Vp-p	S1, S50, f = 200kHz 0.4Vpp ± 6dB input	
	Output voltage 3	V_{AGC3}	0.8	1.2	1.6	Vp-p	S2, S50, f = 200kHz 0.4Vpp ± 6dB input	
	Output voltage 4	V_{AGC4}	0.8	1.2	1.6	Vp-p	S3, S50, f = 200kHz 0.4Vpp ± 6dB input	
	Frequency characteristics 1	F_{AGC1}	—	30	—	MHz	S28, S50, S23 0.4Vpp input *3	
	Frequency characteristics 2	F_{AGC2}	—	30	—	MHz	S1, S50, S23 0.4Vpp input *3	
	Frequency characteristics 3	F_{AGC3}	—	30	—	MHz	S2, S50, S23 0.4Vpp input *3	
	Frequency characteristics 4	F_{AGC4}	—	30	—	MHz	S3, S50, S23 0.4Vpp input *3	

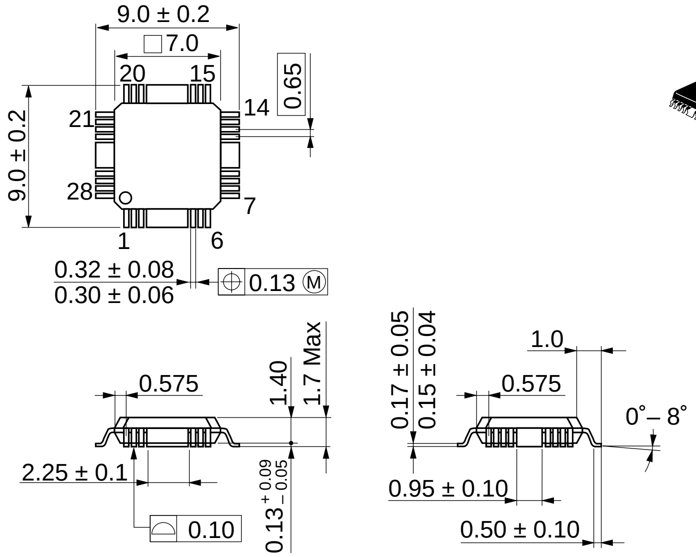
Note: 3. Setting V23 at the value of the pin 23 voltage when S28 is on, VIN50 = 0.4Vpp, and a 200kHz input. The frequency down –3dB from the output level for f = 200kHz.

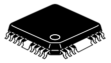
Test Circuit


S28
VCC
0.1µ
1µ
GND
V23
S23
10k
S22
0.015µ
S20
BIAS
AGC
Gain changing
DEFECT
VCB
S1
EQ
S2
RFS
0.033µ
FOK
S3
FSA
S18
MIRR
S51
V51
FE
FA2
FVR2
GND
S50
0.1µ
VIN50
FA
FVR
Offset
S17
IIL
S4
TR1
TVR
TE
TLPF
TVR2
TA
BAL
390k
S5
TR2
560
APC
BUF
2SB
561C
2k
V11
10µ
S8a
S8b
S9a
S9b
20k
Serial data generator
Note: The symbol "●" of transfer switch shows OFF state.

Package Dimensions

Unit: mm


9.0 ± 0.2
□7.0
20
15
14
0.65
21
9.0 ± 0.2
28
7
1
6
0.32 ± 0.08
0.30 ± 0.06
0.13 Ⓜ
0.575
1.40
1.7 Max
2.25 ± 0.1
0.10
$0.13^{+0.09}_{-0.05}$
0.17 ± 0.05
0.15 ± 0.04
1.0
0.575
0° – 8°
0.95 ± 0.10
0.50 ± 0.10



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