HD151011

Dual BCD Programmable Counter with Synchronous Preset Enable

HITACHI

ADE-205-100(Z)
Rev 0
April 1995

The HD151011 has BCD decimal two digits down counter and D-type Flip Flop. The counter can set up to max 99 counts and synchronous preset ($\overline{SPE}$) input can preset the data. When the count value is 0, the next clock pulse presets the data to invert the output. D-type Flip Flop takes the counter output as clock pulse, whose data is transferred to output at the rise edge. It is applied to generate AC signal for STN type liquid crystal and general-use divider.

Features

- High speed operation
  tpd (CLK or $\overline{CLK}$ to Q) = 35 ns (typ)
- High output current
  Fanout of 10 LS TTL Loads
- Wide operating voltage
  Vcc = 2 to 6 V
- Low supply current (Ta = 25°C)
  Icc (Static) = 4 μA (max)

Hitachi semiconductor

Function Table

Control Inputs

CLR	PR	$\overline{SPE}$	C/$\overline{T}$	Mode	Operation Description
H	H	H	X	Generally count	Down count at the rise edge of clock (CLK), Down count at the fall edge of clock ($\overline{CLK}$)
X	X	L	X	Synchronous preset	Jn data is preset at the rise of clock (CLK), the fall of clock ($\overline{CLK}$)
—	—	—	H	—	Clock inputs (CLK, $\overline{CLK}$) is CMOS level
—	—	—	L	—	Clock inputs (CLK, $\overline{CLK}$) is TTL level
L	H	—	—	Initialize of Q output	Initialize of Q = "L"
H	L	—	—	Initialize of Q output	Initialize of Q = "H"

H: High level

L: Low level

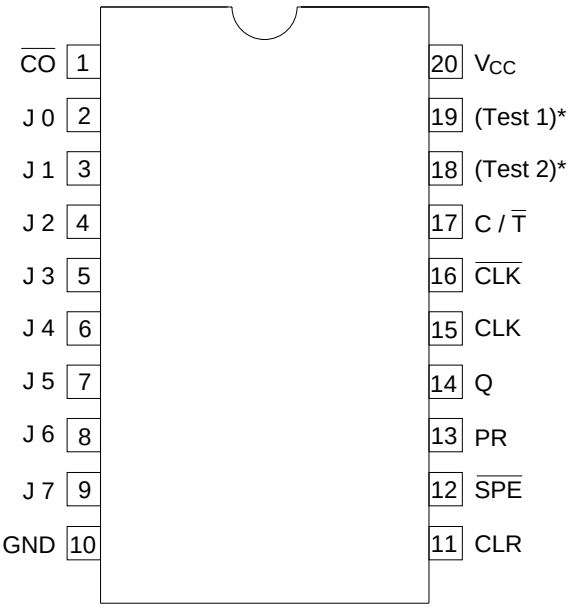
Z: Immaterial

—: Irrespective of condition

1. Synchronous preset ($\overline{SPE}$) input can set max 99 down counts.
2. When the count value is 0, the next clock pulse presets the data to invert the output.
3. CLR and PR inputs initialize output state.
4. Clock inputs (CLK, $\overline{CLK}$) is selectable CMOS level (V_{CC} = 2.0 to 6.0 V) and TTL level (V_{CC} = 4.5 to 5.5V) (Jn, C/$\overline{T}$, PR, CLR and $\overline{SPE}$ inputs are CMOS level)

Note: Don't set data exceeding 99 to Jn. (J0: LSB, J7: MSB)

Pin Arrangement



(Top view)

* Pins 18 and 19 are for function test only and should be open.

Pin Description

Pin Name		Pin Description	
Input pins	J0 to J7	Count data input for option	
	C/T	Level change input for CLK, CLK (CMOS level or TTL level)	
	CLK, CLK	Clock inputs	CLK : Rise edge trigger
			CLK : Fall edge trigger
	SPE	Preset input for Jn data	
	PR	Preset input for D-type Flip Flop (Initialize "L" at Q output)	
	CLR	Clear input for D-type Flip Flop (Initialize "H" at Q output)	
Output pins	CO	Output for BCD decimal counter	
	Q	Output for D-type Flip Flop	

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	–0.5 to 7.0	V
Input / output voltage	V_{IN} / V_{OUT}	–0.5 to V_{CC} +0.5	V
VCC, GND current	I_{CC}, I_{GND}	±50	mA
Output current / pin	I_{OUT}	±25	mA
Power dissipation	P_T	757	mW
Storage temperature	Tstg	–65 to 150	°C
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA

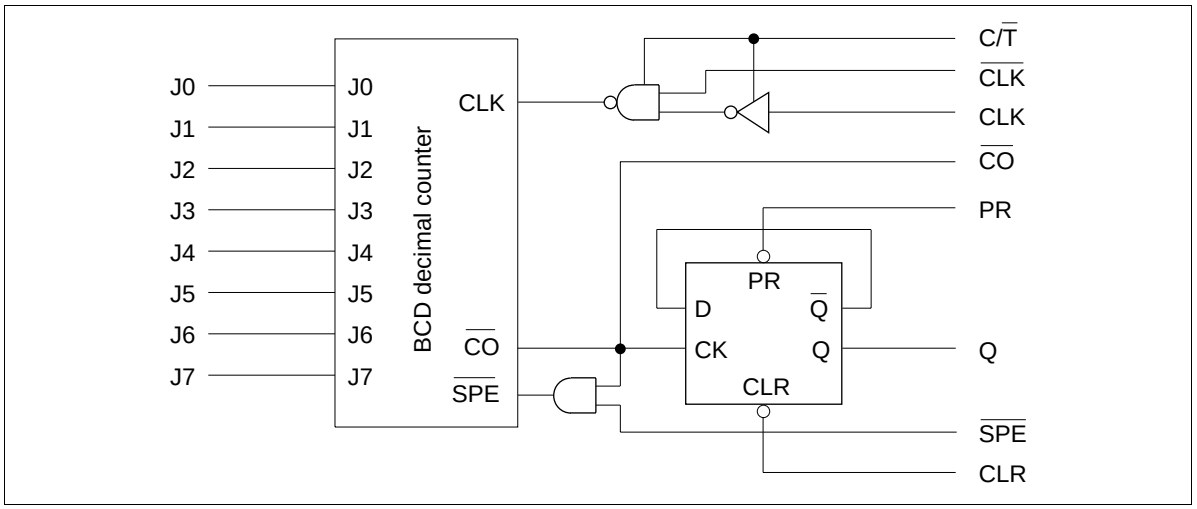
Notes: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.
2. All voltage values except for differential input voltage are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	2	—	6	V
Input / output voltage		V_{IN} / $_{OUT}$	0	—	V_{CC}	V
Operating temperature		Topr	–40	—	+85	°C
Input rise / fall time [*1]	V_{CC} = 2.5 V	tr, tf	0	—	1000	ns
	V_{CC} = 4.5 V		0	—	500	
	V_{CC} = 5.5 V		0	—	400	

Note: 1. This item guarantees maximum limit when one input switches.

Logic Diagram



Electrical Characteristics

			Ta = 25°C			Ta = –40 to 85°C			
Item	**Symbol**	**V_{CC}**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
High level input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V	J0 to J7
		4.5	3.15	—	—	3.15	—		C/$\overline{T}$, $\overline{SPE}$
		6.0	4.2	—	—	4.2	—		PR, CLR
		2.0	1.5	—	—	1.5	—		$\overline{CLK}$, CLK C/$\overline{T}$ = V_{IH}
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
		4.5 to 5.5	2.0	—	—	2.0	—		C/$\overline{T}$ = V_{IL}
Low level input voltage	V_{IL}	2.0	—	—	0.5	—	0.5	V	J0 to J7
		4.5	—	—	1.35	—	1.35		C/$\overline{T}$, SPE
		6.0	—	—	1.8	—	1.8		PR, CLR
		2.0	—	—	0.5	—	0.5		$\overline{CLK}$, CLK C/$\overline{T}$ = V_{IH}
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
		4.5 to 5.5	—	—	0.8	—	0.8		C/$\overline{T}$ = V_{IL}
High level output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	V_{IN} = V_{IH} or V_{IL} I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	4.31	—	4.13	—		I_{OH} = –4 mA
		6.0	5.68	5.80	—	5.63	—		I_{OH} = –5.2 mA
Low level output voltage	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	V_{IN} = V_{IH} or V_{IL} I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	0.17	0.26	—	0.33		I_{OL} = 4 mA
		6.0	—	0.18	0.26	—	0.33		I_{OL} = 5.2 mA
Input capacitance	IIN	6.0	—	—	±0.1	—	±1.0	mA	V_{IN} = V_{CC} or GND
Supply current	I_{CC}	6.0	—	—	4.0	—	40.0	mA	V_{IN} = V_{CC} or GND

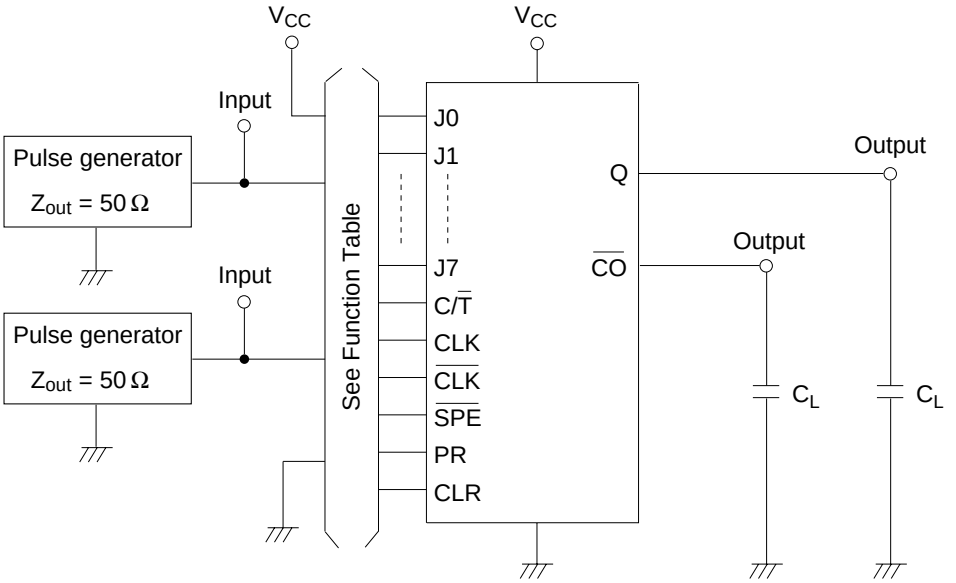
Switching Characteristics (C_L = 50 pF, tr = tf = 6 ns)

			Ta = 25°C			Ta = –40 to 85°C			
Item	**Symbol**	**V_{CC}**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Maximum clock frequency	fmax	2.0	—	—	4	—	3	MHz	
		4.5	—	36	20	—	16		
		6.0	—	—	24	—	19		
Output rise / fall time	t_{TLH}	2.0	—	30	75	—	95	ns	
	t_{THL}	4.5	—	8	15	—	19		
		6.0	—	7	13	—	16		
Propagation delay time	t_{PLH}	2.0	—	—	250	—	318	ns	CLK or $\overline{CLK}$ to $\overline{CO}$
	t_{PHL}	4.5	—	30	50	—	63		
		6.0	—	—	45	—	53		
	t_{PLH}	2.0	—	—	300	—	380		CLK or $\overline{CLK}$ to Q
	t_{PHL}	4.5	—	35	60	—	75		
		6.0	—	—	53	—	65		
	t_{PLH}	2.0	—	—	150	—	185		PR or CLR to Q
	t_{PHL}	4.5	—	18	30	—	38		
		6.0	—	—	25	—	32		
Pulse width	tw	2.0	80	—	—	100	—	ns	
(CLK, CLK, PR, CLR)		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		
Setup time	ts	2.0	100	—	—	125	—	ns	
(Jn - CLK, CLK)		4.5	20	—	—	25	—		
(SPE, CLK, CLK)		6.0	17	—	—	21	—		
Hold time	th	2.0	15	—	—	15	—	ns	
(Jn - CLK, CLK)		4.5	10	—	—	10	—		
(SPE, CLK, CLK)		6.0	5	—	—	5	—		
Input capacitance	C_{IN}	—	—	5	10	—	10	pF	
Power dissipation capacitance	C_{PD}	—	—	48	—	—	—	pF	

Note: 1. CPD is equivalent capacitance inside of the IC calculated from the operating current without load (see test circuit). The average operating current without load is calculated according to the expression below.

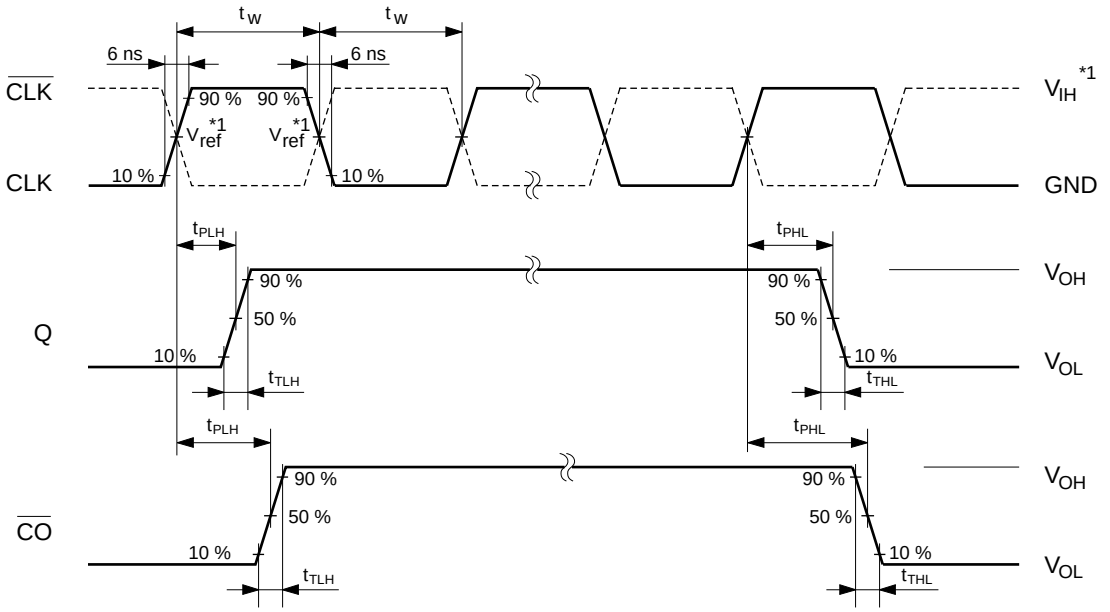
$$I_{CC}\ (opr) = C_{PD}\, V_{CC} \bullet f_{IN} + I_{CC}$$

- **Test Circuit**



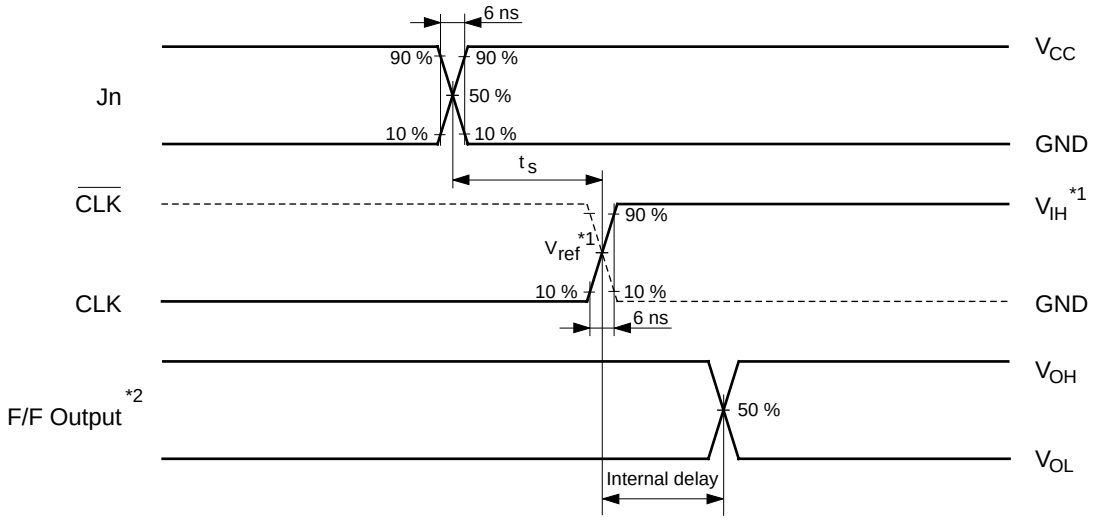
Note: 1. C_L includes probe and jig capacitance.

- **Waveforms – 1**



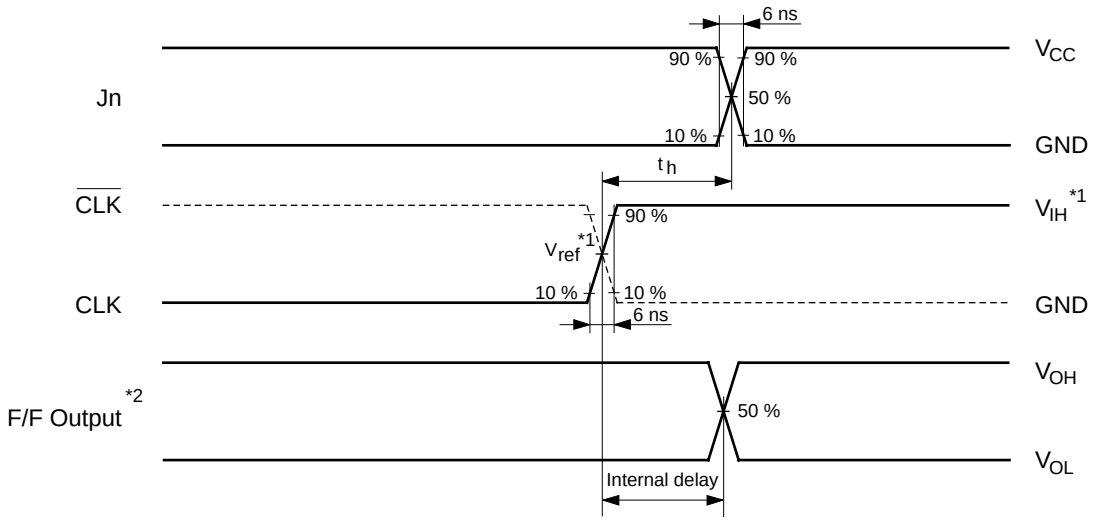
Note: 1. In case of C/$\overline{T}$ = "L", CLK, $\overline{CLK}$ is V_{IH} = 3 V, Vref is 1.3 V
In case of C/T = "H", CLK, $\overline{CLK}$ is V_{IH} = V_{CC}, Vref is V_{CC} × 50%

- **Waveforms – 2**



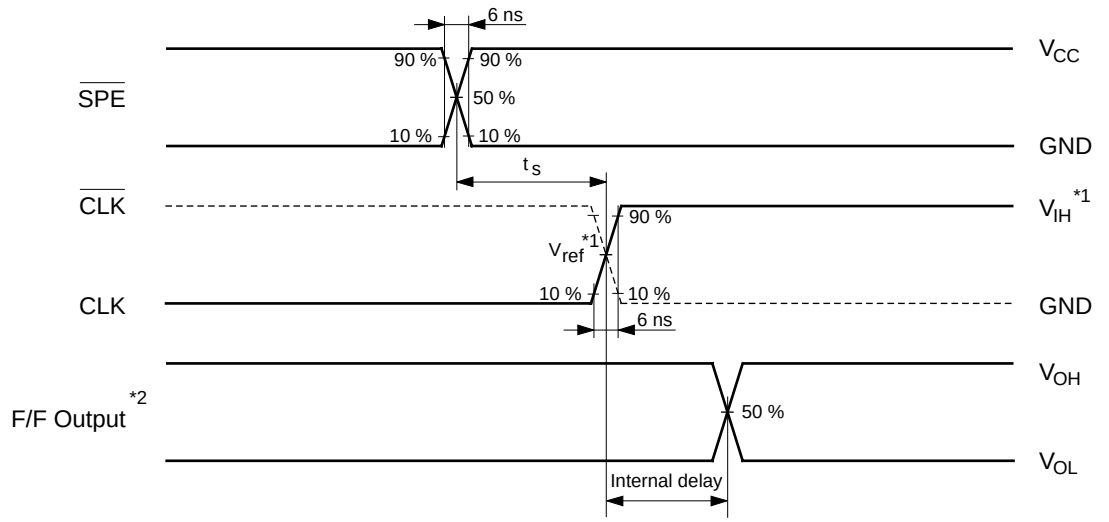
Notes: 1. In case of C/$\overline{T}$ = "L", CLK, $\overline{CLK}$ is V_{IH} = 3 V, Vref is 1.3 V
In case of C/T = "H", CLK, $\overline{CLK}$ is V_{IH} = V_{CC}, Vref is V_{CC} × 50%
2. F/F output is internal signal of IC.

- **Waveforms – 3**



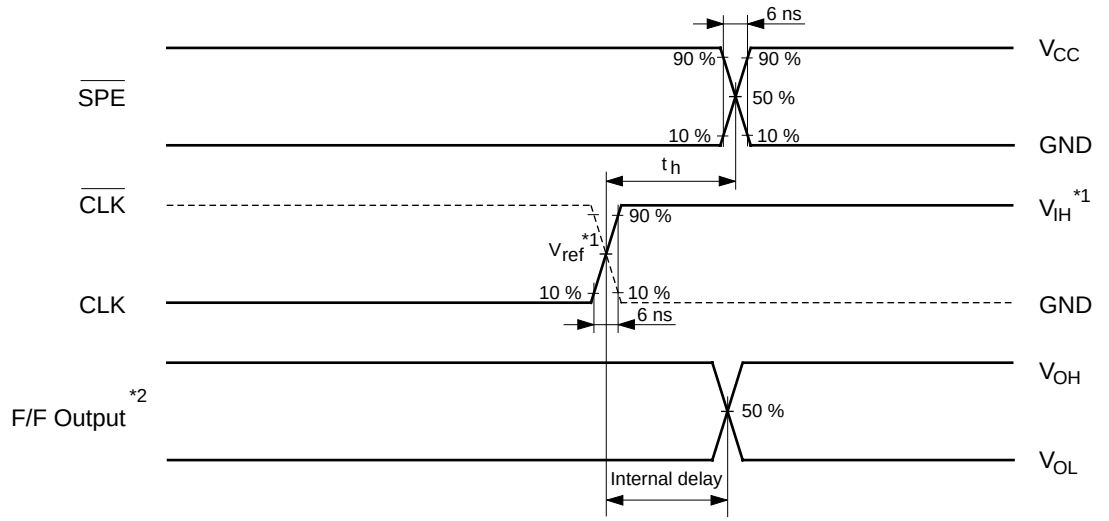
Notes: 1. In case of C/$\overline{T}$ = "L", CLK, $\overline{CLK}$ is V_{IH} = 3 V, Vref is 1.3 V
In case of C/T = "H", CLK, $\overline{CLK}$ is V_{IH} = V_{CC}, Vref is V_{CC} × 50%
2. F/F output is internal signal of IC.

- **Waveforms – 4**



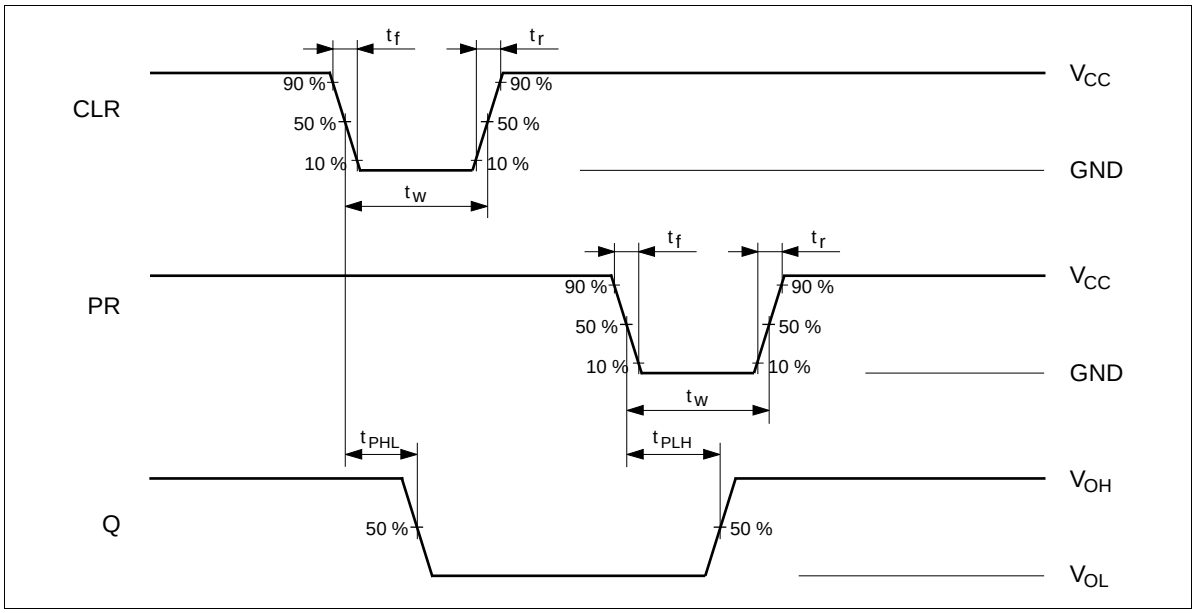
Notes: 1. In case of C/$\overline{T}$ = "L", CLK, $\overline{CLK}$ is V_{IH} = 3 V, Vref is 1.3 V
In case of C/T = "H", CLK, $\overline{CLK}$ is V_{IH} = V_{CC}, Vref is $V_{CC} \times 50\%$
2. F/F output is internal signal of IC.

- **Waveforms – 5**

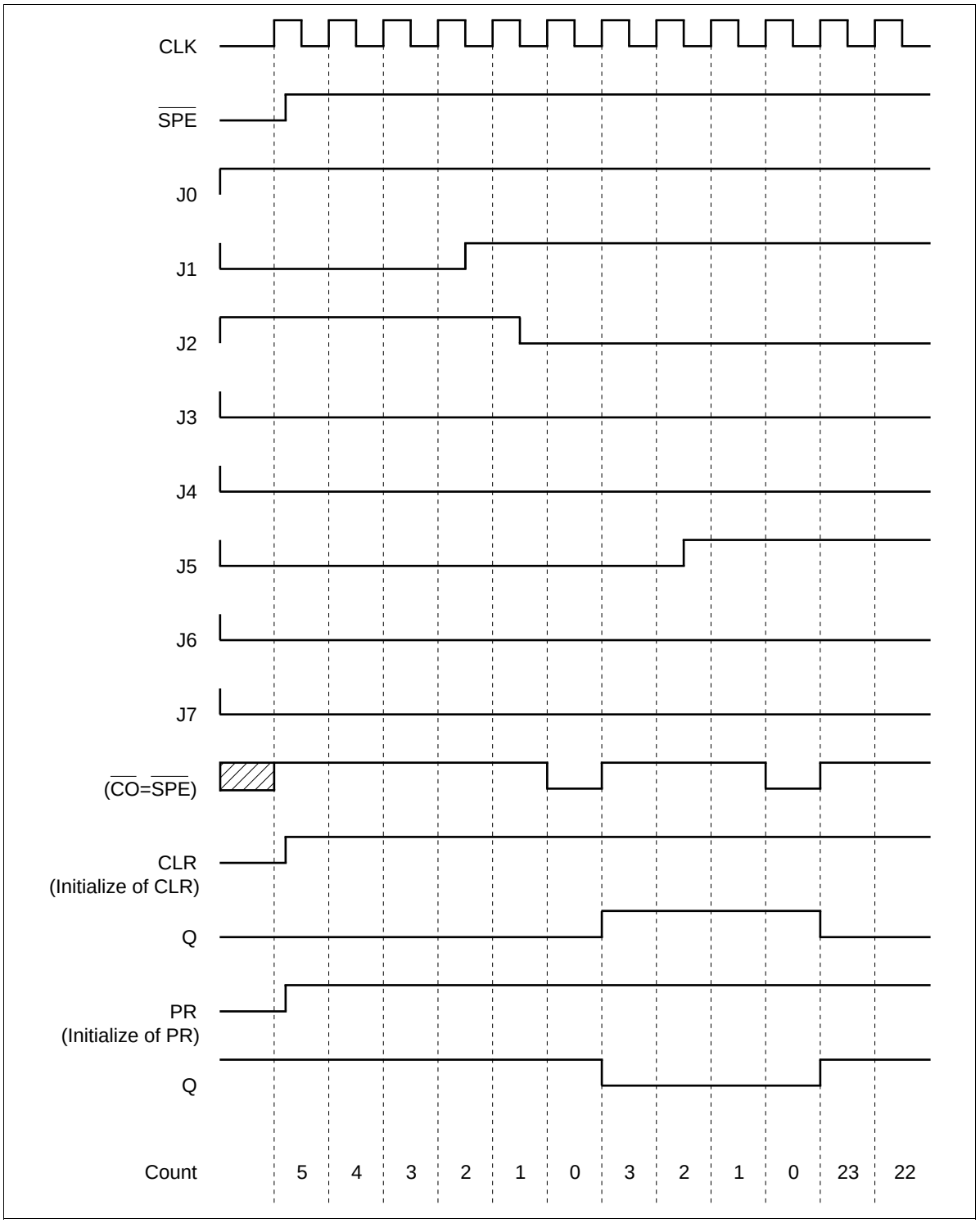


Notes: 1. In case of C/$\overline{T}$ = "L", CLK, $\overline{CLK}$ is V_{IH} = 3 V, Vref is 1.3 V
In case of C/T = "H", CLK, $\overline{CLK}$ is V_{IH} = V_{CC}, Vref is $V_{CC} \times 50\%$
2. F/F output is internal signal of IC.

- **Waveforms – 6**



Timing Chart

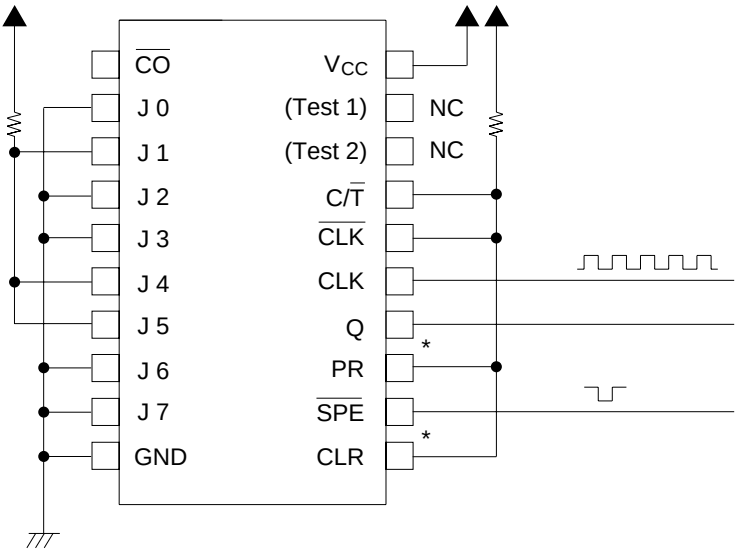


Example of Application Circuit

• AC Signal Generator for STN Type Liquid Crystal Panel

CLK ($\overline{CLK}$) : CMOS level input

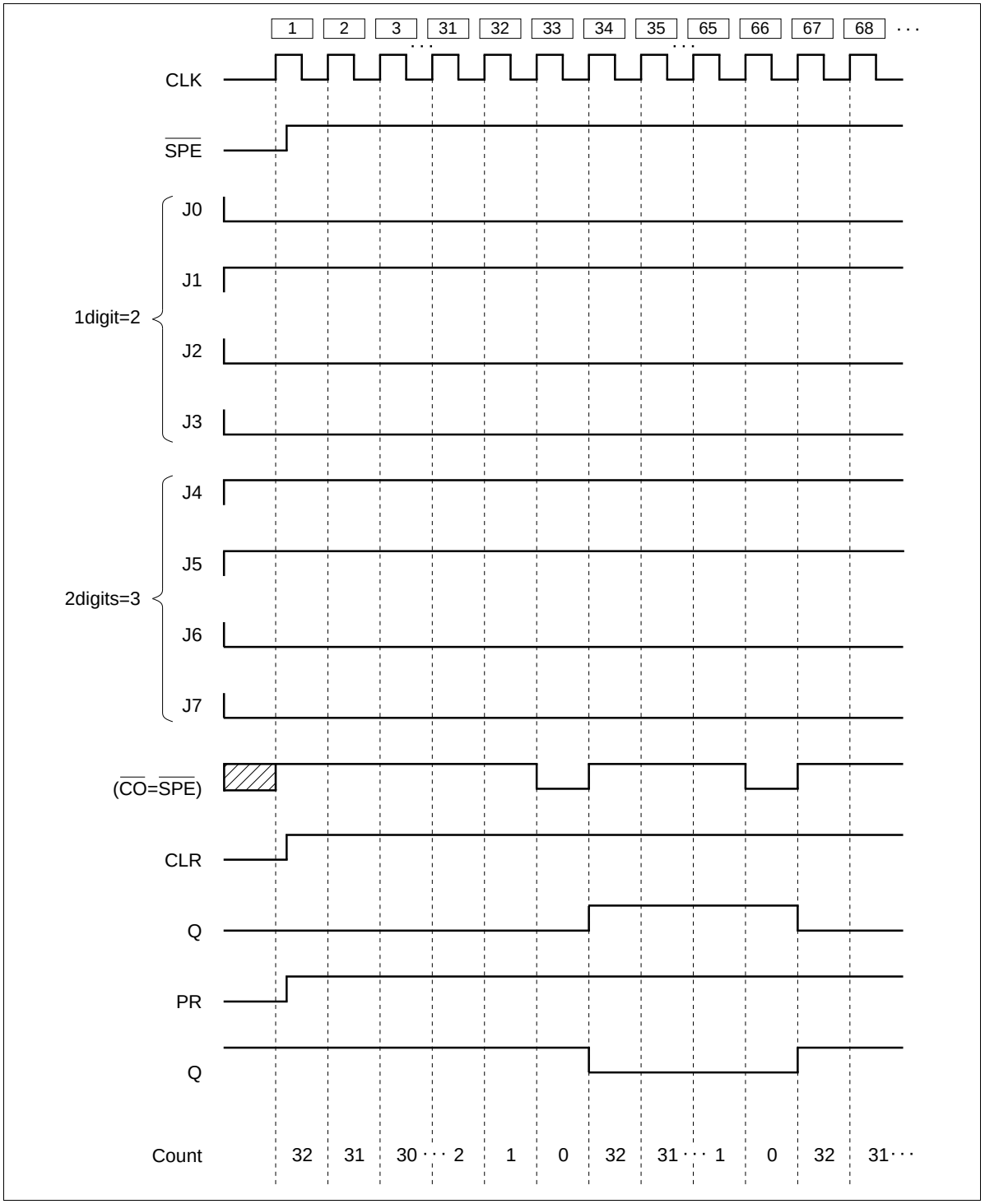
Initialize counter : 32



*When initializing output D-F/F apply "L"

Timing Chart

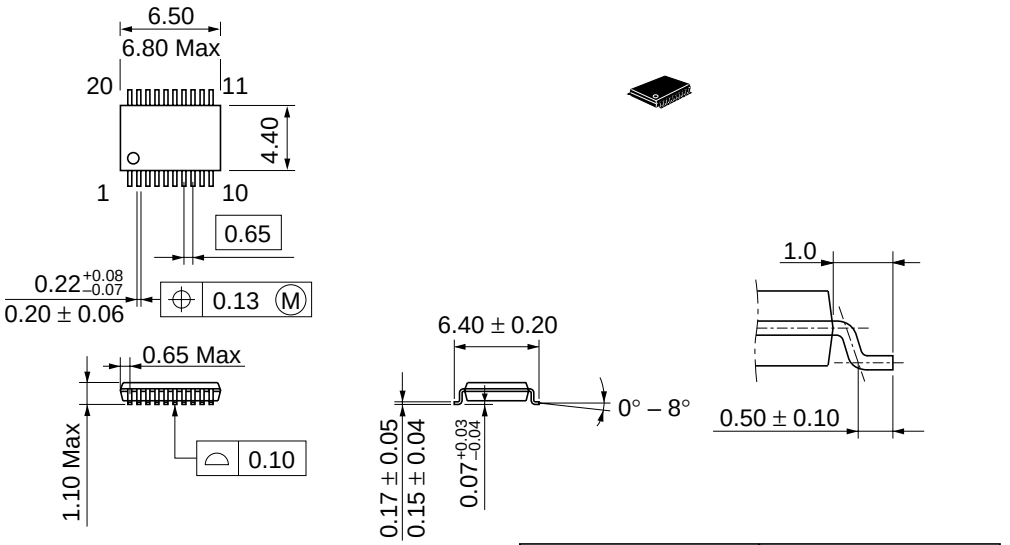
• Example of AC Signal Generator



Package Dimensions

Unit : mm

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g

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