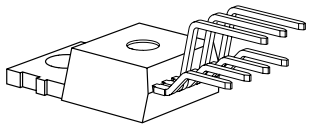
5-A H-Bridge for DC-Motor Applications TLE 5205-2

1 Overview

1.1 Features

- Delivers up to 5 A continuous 6 A peak current
- Optimized for DC motor management applications
- Operates at supply voltages up to 40 V
- Very low $R_{DS\ ON}$; typ. 200 mΩ @ 25 °C per switch
- Output full short circuit protected
- Overtemperature protection with hysteresis and diagnosis
- Short circuit and open load diagnosis with open drain error flag
- Undervoltage lockout
- CMOS/TTL compatible inputs with hysteresis
- No crossover current
- Internal freewheeling diodes
- Wide temperature range; – 40 °C < T_j < 150 °C



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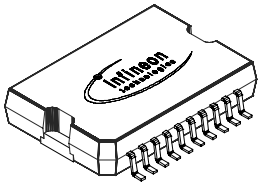

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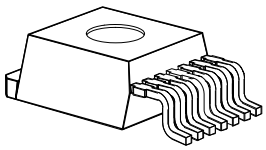

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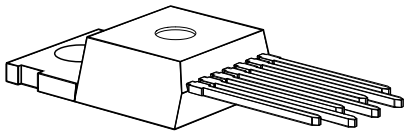


P-TO220-7-12

Type	Ordering Code	Package
TLE 5205-2	Q67000-A9283	P-TO220-7-11
TLE 5205-2GP	Q67006-A9237	P-DSO-20-12
TLE 5205-2G	Q67006-A9325	P-TO263-7-1
TLE 5205-2S	Q67000-A9324	P-TO220-7-12

Description

The TLE 5205-2 is an integrated power H-bridge with DMOS output stages for driving DC-Motors. The part is built using the Infineon multi-technology process SPT® which allows bipolar and CMOS control circuitry plus DMOS power devices to exist on the same monolithic structure.

Operation modes forward (cw), reverse (ccw), brake and high impedance are invoked from just two control pins with TTL/CMOS compatible levels. The combination of an extremely low $R_{DS\ ON}$ and the use of a power IC package with low thermal resistance and high thermal capacity helps to minimize system power dissipation. A blocking capacitor at the supply voltage is the only external circuitry due to the integrated freewheeling diodes.

1.2 Pin Configuration (top view)

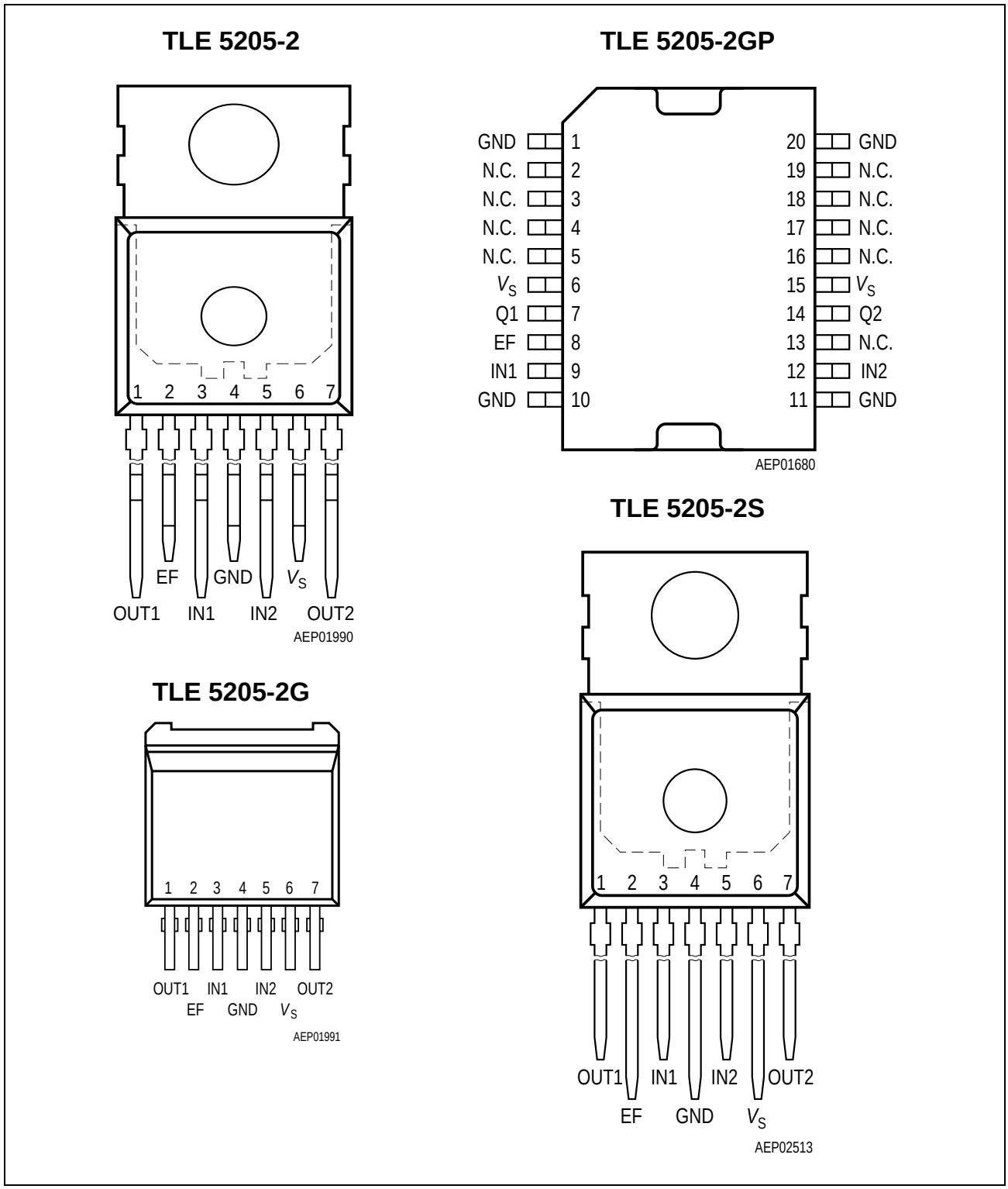


Figure 1

1.3 Pin Definitions and Functions

Pin No. P-TO220	Pin No. P-DSO	Symbol	Function
1	7	OUT1	**Output of Channel 1;** Short-circuit protected; integrated freewheeling diodes for inductive loads.
2	8	EF	**Error Flag;** TTL/CMOS compatible output for error detection; (open drain)
3	9	IN1	**Control Input 1;** TTL/CMOS compatible
4	1, 10, 11, 20	GND	**Ground;** internally connected to tab
5	12	IN2	**Control Input 2;** TTL/CMOS compatible
6	6, 15	V_S	**Supply Voltage;** block to GND
7	14	OUT2	**Output of Channel 2;** Short-circuit protected; integrated freewheeling diodes for inductive loads.
–	2, 3, 4, 5, 16, 17, 18, 19	N.C.	**Not Connected**

1.4 Functional Block Diagram

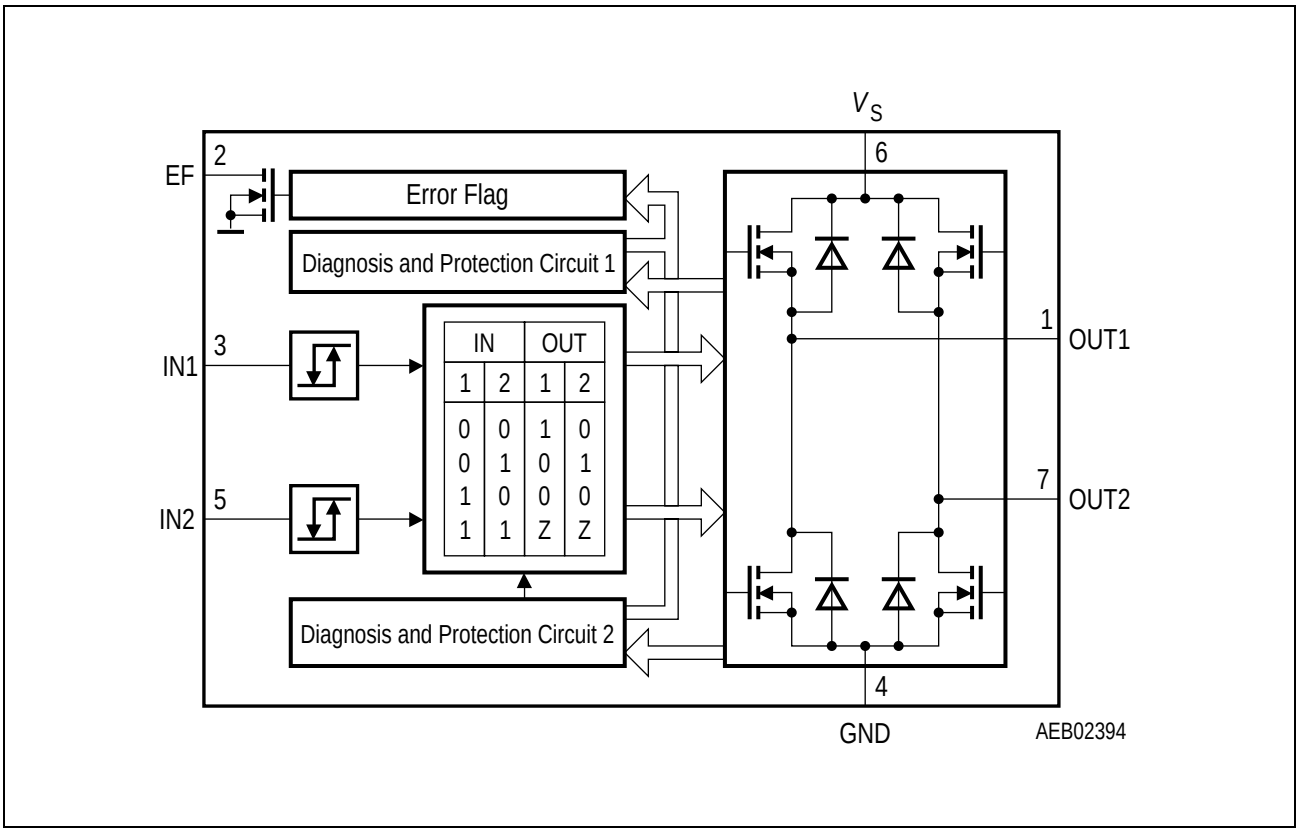


Figure 2 Block Diagram

1.5 Circuit Description

Input Circuit

The control inputs consist of TTL/CMOS-compatible schmitt-triggers with hysteresis. Buffer amplifiers are driven by this stages.

Output Stages

The output stages consist of a DMOS H-bridge. Integrated circuits protect the outputs against short-circuit to ground and to the supply voltage. Positive and negative voltage spikes, which occur when switching inductive loads, are limited by integrated freewheeling diodes.
A monitoring circuit for each output transistor detects whether the particular transitor is active and in this case prevents the corresponding source transistor (sink transistor) from conducting in sink operation (source operation). Therefore no crossover currents can occur.

1.6 Input Logic Truth Table

Functional Truth Table

IN1	IN2	OUT1	OUT2	Comments
L	L	H	L	Motor turns clockwise
L	H	L	H	Motor turns counterclockwise
H	L	L	L	Brake; both low side transistors turned-ON
H	H	Z	Z	Open circuit detection

Notes for Output Stage

Symbol	Value
L	Low side transistor is turned-ON High side transistor is turned-OFF
H	High side transistor is turned-ON Low side transistor is turned-OFF
Z	High side transistor is turned-OFF Low side transistor is turned-OFF

1.7 Monitoring Functions

Undervoltage lockout (UVLO):
When V_S reaches the switch on voltage $V_{S\,ON}$ the IC becomes active with a hysteresis. All output transistors are switched off if the supply voltage V_S drops below the switch off value $V_{S\,OFF.}$

1.8 Protective Function

Various errors like short-circuit to + V_S, ground or across the load are detected. All faults result in turn-OFF of the output stages after a delay of 50 µs and setting of the error flag EF to ground. Changing the inputs resets the error flag.

a. Output Shorted to Ground Detection
If a high side transistor is switched on and its output is shorted to ground, the output current is internally limited. After a delay of 50 µs all outputs will be switched-OFF and the error flag is set.

b. Output Shorted to + V_S Detection
If a low side transistor is switched on and its output is shorted to the supply voltage, the output current is internally limited. After a delay of 50 µs all outputs will be switched-OFF and the error flag is set.

c. Overload Detection
An internal circuit detects if the current through the low side transistor exceeds the trippoint I_{SDL}. In this case all outputs are turned off after 50 µs and the error flag is set.

d. Overtemperature Protection
At a junction temperature higher than 150 °C the thermal shutdown turns-OFF, all four output stages commonly and the error flag is set with a delay.

e. Open Load Detection
The output Q1 has a 10 kΩ pull-up resistor and the output Q2 has a 10 kΩ pull-down resistor. If E1 and E2 are high, all output power stages are turned-OFF. In case of no load between Q1 and Q2 the output voltage Q1 is V_S and Q2 is ground. This state will be detected by two comparators and an error flag will be set after a delay time of 50 µs. Changing the inputs resets the error flip flop.

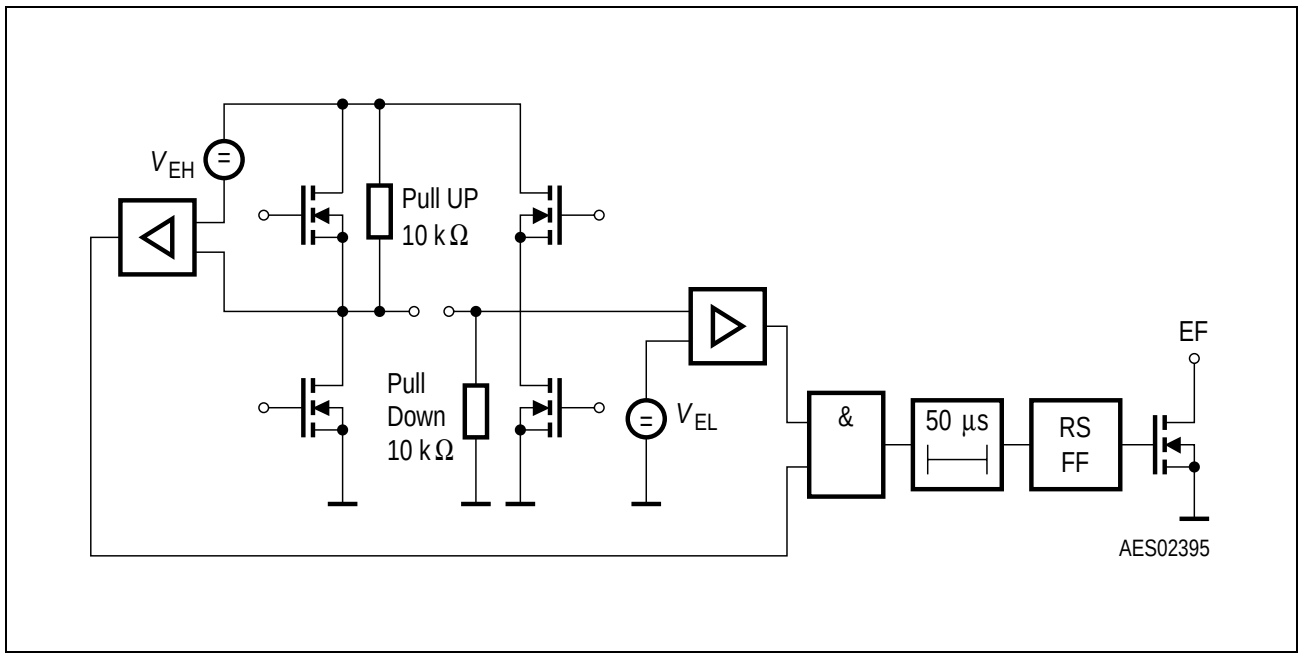


Figure 3 Simplified Schematic for Open Load Detection

2 Diagnosis

Various errors as listed in the table “Diagnosis” are detected. Short circuits and overload result in turning off the output stages after a delay t_{dSD} and setting the error flag simultaneously [EF = L]. Changing the inputs to a state where the fault is not detectable resets the error flag (input toggling) with the exception of short circuit from OUT1 to OUT2 (load short circuit).

Flag	IN1	IN2	OUT1	OUT2	EF	Remarks	Nr.
Open circuit between OUT1 and OUT2	0	0	H	L	1	Not detectable	1
	0	1	L	H	1	Not detectable	2
	1	0	L	L	1	Not detectable	3
	1	1	Z	Z	0		4
Short circuit from OUT1 to OUT2	0	0	V_S/2	V_S/2	0		5
	0	1	V_S/2	V_S/2	0		6
	1	0	L	L	1	Not detectable	7
	1	1	Z	Z	1	Not detectable	8
Short circuit from OUT1 to GND	0	0	GND	L	0		9
	0	1	GND	H	1	Not detectable	10
	1	0	GND	L	1	Not detectable	11
	1	1	GND	L	1	Not detectable	12
Short circuit from OUT2 to GND	0	0	H	GND	1	Not detectable	13
	0	1	L	GND	0		14
	1	0	L	GND	1	Not detectable	15
	1	1	L	GND	1	Not detectable	16
Short circuit from OUT1 to V_S	0	0	V_S	L	1	Not detectable	17
	0	1	V_S	H	0		18
	1	0	V_S	H	0		19
	1	1	V_S	H	1	Not detectable	20
Short circuit from OUT2 to V_S	0	0	H	V_S	0		21
	0	1	L	V_S	1	Not detectable	22
	1	0	H	V_S	0		23
	1	1	H	V_S	1	Not detectable	24
Overtemperature or undervoltage	0	0	Z	Z	0		25
	0	1	Z	Z	0		26
	1	0	Z	Z	0		27
	1	1	Z	Z	0		28

IN: 0 = Logic LOW
1 = Logic HIGH

OUT: Z = Output in tristate condition
= V_S /2 due to internal Pull-up/down resistors
L = Output in sink condition
H = Output in source condition

EF: 1 = No error
0 = Error

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

– 40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	– 0.3	40	V	–
		– 1	40	V	t < 0.5 s; I_S > – 5 A
Logic input voltage	$V_{IN1, 2}$	– 0.3	7	V	0 V < V_S < 40 V
Diagnostics output voltage	V_{EF}	– 0.3	7	V	–
Currents of DMOS-Transistors and Freewheeling Diodes					
Output current (cont.)	$I_{OUT1, 2}$	– 5	5	A	–
Output current (peak)	$I_{OUT1, 2}$	– 6	6	A	t_p < 100 ms; T = 1 s
Output current (peak)	$I_{OUT1, 2}$	–	–	A	t_p < 50 µs; T = 1 s; internally limitted; see overcurrent
Temperatures					
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–
Thermal Resistances					
Junction case	R_{thjC}	–	3	K/W	P-TO220-7-11/12, P-TO263-7-1
Junction ambient	R_{thjA}	–	65	K/W	P-TO220-7-11/12
		–	75	K/W	P-TO263-7-1
Junction case	R_{thjC}	–	5	K/W	P-DSO-20-12
Junction ambient	R_{thjA}	–	50	K/W	P-DSO-20-12

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

3.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	$V_{UV\ ON}$	40	V	After V_S rising above $V_{UV\ ON}$
Supply voltage increasing		– 0.3	$V_{UV\ ON}$	V	Outputs in tristate condition
Supply voltage decreasing		– 0.3	$V_{UV\ OFF}$	V	
Logic input voltage	$V_{IN1,\ 2}$	– 0.3	7	V	–
Junction temperature	T_j	– 40	150	°C	–

3.3 Electrical Characteristics

6 V < V_S < 18 V; IN1 = IN2 = HIGH
$I_{OUT1,\ 2}$ = 0 A (No load); – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption						
Quiescent current	I_S	–	–	10	mA	IN1 = IN2 = LOW; V_S = 13.2 V
Under Voltage Lockout						
UV-Switch-ON voltage	$V_{UV\ ON}$	–	5.3	6	V	V_S increasing
UV-Switch-OFF voltage	$V_{UV\ OFF}$	3.5	4.7	5.6	V	V_S decreasing
UV-ON/OFF-Hysteresis	$V_{UV\ HY}$	0.2	0.6	–	V	$V_{UV\ ON} - V_{UV\ OFF}$

3.3 Electrical Characteristics (cont'd)

6 V < V_S < 18 V; IN1 = IN2 = HIGH
$I_{OUT1, 2}$ = 0 A (No load); – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Outputs OUT1, 2						
Static Drain-Source-On Resistance						
Source I_{OUT} = – 3 A	$R_{DS\ ON\ H}$	–	220	350	mΩ	6 V < V_S < 18 V T_j = 25 °C
			–	500	mΩ	6 V < V_S < 18 V
			350	500	mΩ	$V_{S\ ON}$ < V_S ≤ 6 V T_j = 25 °C
			–	800	mΩ	$V_{S\ ON}$ < V_S ≤ 6 V
Sink I_{OUT} = 3 A	$R_{DS\ ON\ L}$	–	230	350	mΩ	6 V < V_S < 18 V T_j = 25 °C
			–	500	mΩ	6 V < V_S < 18 V
			400	600	mΩ	$V_{S\ ON}$ < V_S ≤ 6 V T_j = 25 °C
			–	1000	mΩ	$V_{S\ ON}$ < V_S ≤ 6 V

Note: Values of $R_{DS\ ON}$ for $V_{S\ ON}$ < V_S ≤ 6 V are guaranteed by design.

Overcurrent

Source shutdown trippoint	– I_{SDH}	–	–	10	A	T_j = – 40 °C
		–	8	–	A	T_j = 25 °C
		6	–	–	A	T_j = 150 °C
Sink shutdown trippoint	I_{SDL}	–	–	10	A	T_j = – 40 °C
		–	8	–	A	T_j = 25 °C
		6	–	–	A	T_j = 150 °C
Shutdown delay time	t_{dSD}	25	50	80	µs	–

3.3 Electrical Characteristics (cont'd)

6 V < V_S < 18 V; IN1 = IN2 = HIGH
$I_{OUT1, 2}$ = 0 A (No load); – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Short Circuit Current Limitation						
Source current	$-I_{SCH}$	–	–	20	A	$t < t_{dSD}$
Sink current	I_{SCL}	–	–	15	A	$t < t_{dSD}$
Open Circuit						
Pull up resistor	R_{UP}	5	10	20	kΩ	–
Pull down resistor	R_{DOWN}	5	10	20	kΩ	–
Switching threshold H	V_{EH}	2	2.5	3	V	–
Switching threshold L	V_{EH}	2	2.4	3	V	–
Detection delay time	t_{dSD}	25	50	80	µs	–
Output Delay Times (Device Active for *t* > 1 ms)						
Source ON	$t_{d\ ON\ H}$	–	10	20	µs	I_{OUT} = – 3 A resistive load
Sink ON	$t_{d\ ON\ L}$	–	10	20	µs	I_{OUT} = 3 A resistive load
Source OFF	$t_{d\ OFF\ H}$	–	2	5	µs	I_{OUT} = – 3 A resistive load
Sink OFF	$t_{d\ OFF\ L}$	–	2	5	µs	I_{OUT} = 3 A resistive load

3.3 Electrical Characteristics (cont'd)

6 V < V_S < 18 V; IN1 = IN2 = HIGH
$I_{OUT1, 2}$ = 0 A (No load); – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Switching Times (Device Active for *t* > 1 ms)						
Source ON	$t_{ON\ H}$	–	15	30	µs	I_{OUT} = – 3 A resistive load
Sink ON	$t_{ON\ L}$	–	5	10	µs	I_{OUT} = 3 A resistive load
Source OFF	$t_{OFF\ H}$	–	2	5	µs	I_{OUT} = – 3 A resistive load
Sink OFF	$t_{OFF\ L}$	–	2	5	µs	I_{OUT} = 3 A resistive load
Clamp Diodes						
Forward Voltage						
High-side	V_{FH}	–	1	1.5	V	I_F = 3 A
Low-side	V_{FL}	–	1.1	1.5	V	I_F = 3 A
Leakage Current						
Source	I_{LKH}	– 100	– 50	–	µA	OUT1 = V_S
Sink	I_{LKL}	–	50	100	µA	OUT2 = GND
Logic						
Control Inputs IN 1, 2						
H-input voltage threshold	V_{INH}	2.8	2.5	–	V	–
L-input voltage	V_{INL}	–	1.7	1.2	V	–
Hysteresis of input voltage	V_{INHY}	0.4	0.8	1.2	V	–
H-input current	I_{INH}	– 2	0	2	µA	V_{IN} = 5 V
L-input current	I_{INL}	– 10	– 4	0	µA	V_{IN} = 0 V

3.3 Electrical Characteristics (cont'd)

6 V < V_S < 18 V; IN1 = IN2 = HIGH
$I_{OUT1, 2}$ = 0 A (No load); – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Error Flag Output EF						
Low output voltage	V_{EFL}	–	0.25	0.5	V	I_{EF} = 3 mA
Leakage current	I_{EFL}	–	–	10	µA	V_{EF} = 7 V
Thermal Shutdown						
Thermal shutdown junction temperature	T_{jSD}	150	175	200	°C	–
Thermal switch-on junction temperature	T_{jSO}	120	–	170	°C	–
Temperature hysteresis	ΔT	–	30	–	K	–
Shutdown delay time	t_{dSD}	25	50	80	µs	–

Note: Values of thermal shutdown are guaranteed by design.

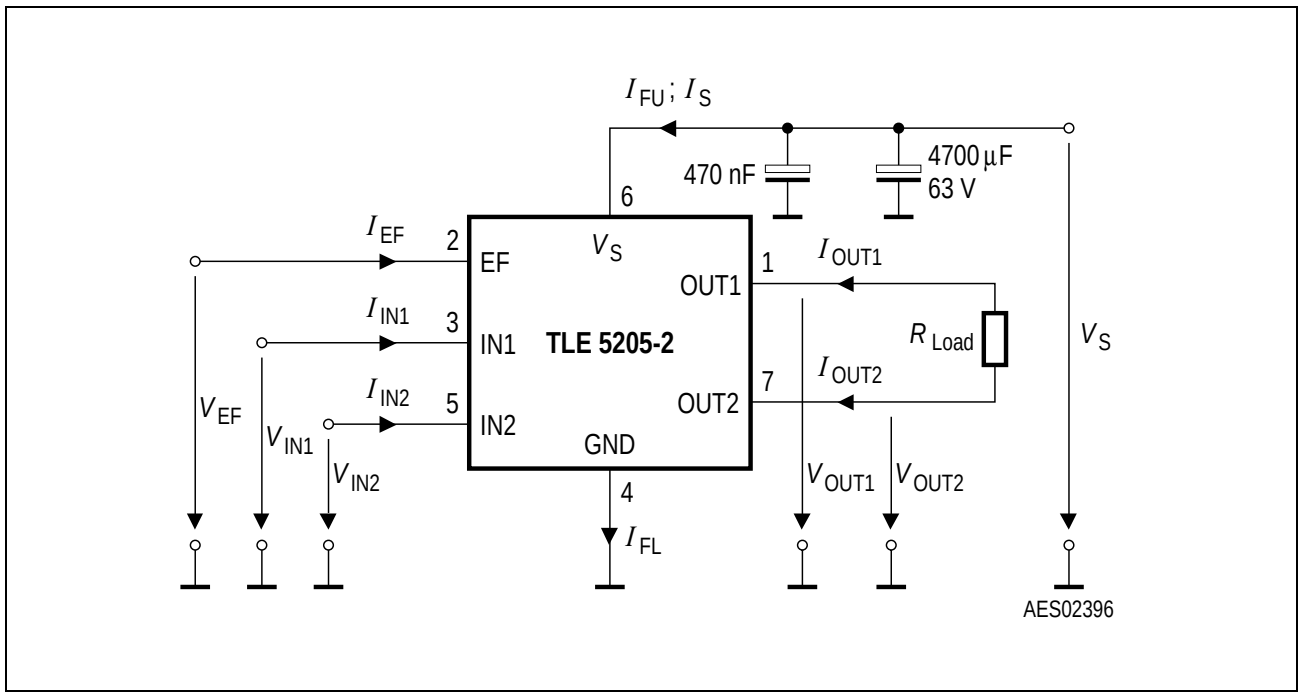


Figure 4 Test Circuit

	Overcurrent	Short Circuit	Open Circuit
I_{OUT}	I_{SD}	I_{SC}	I_{OC}

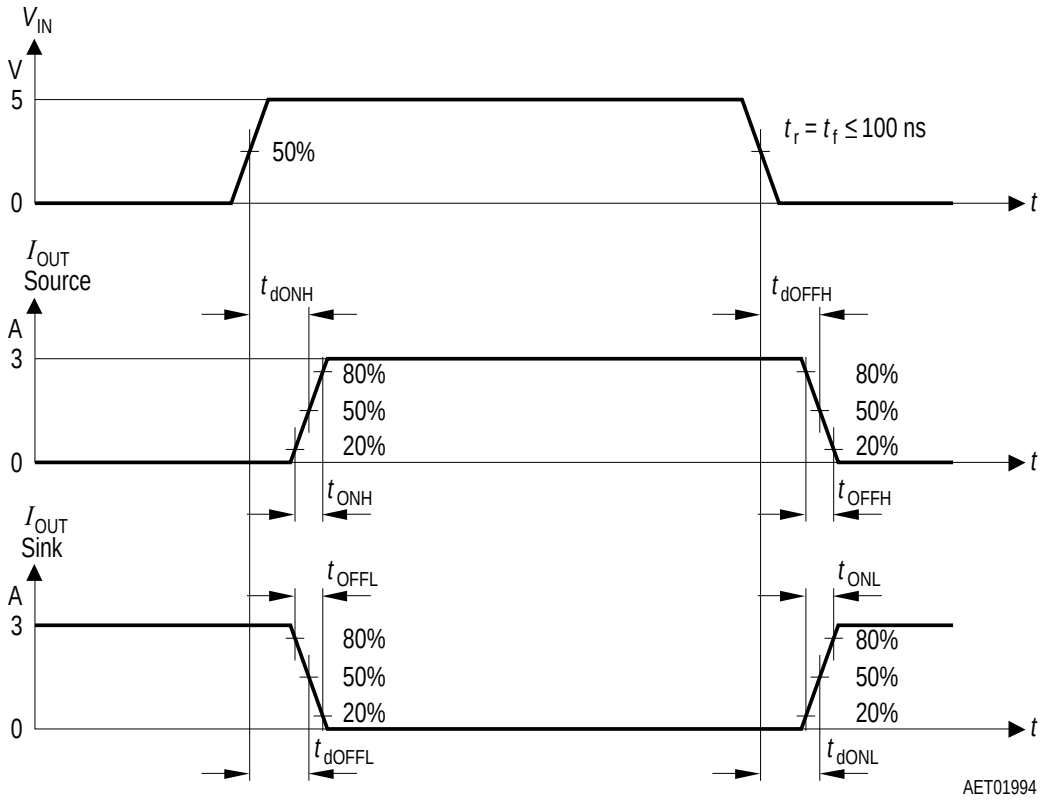


Figure 5 Switching Time Definitions

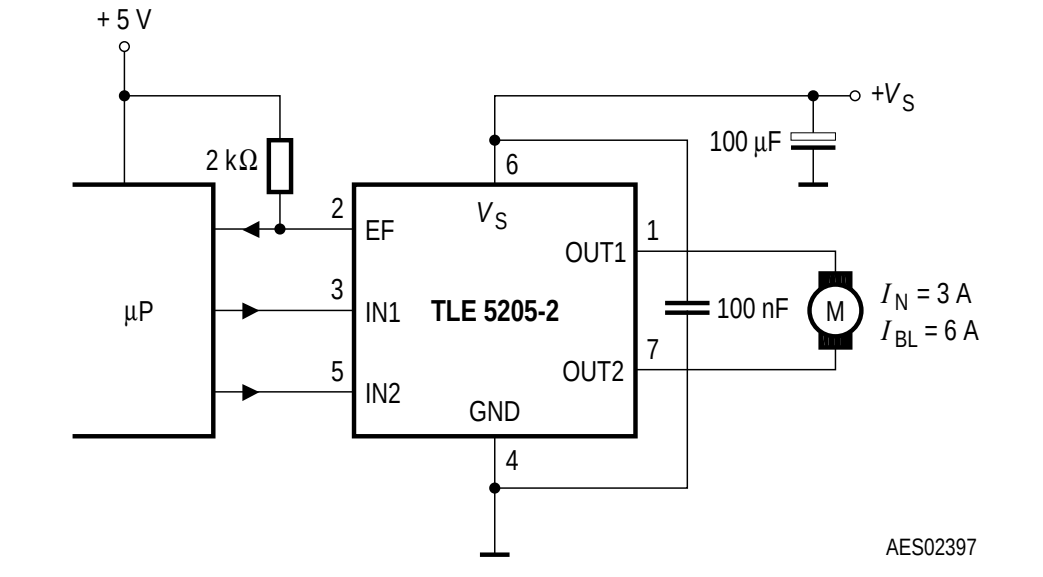


Figure 6 Application Circuit

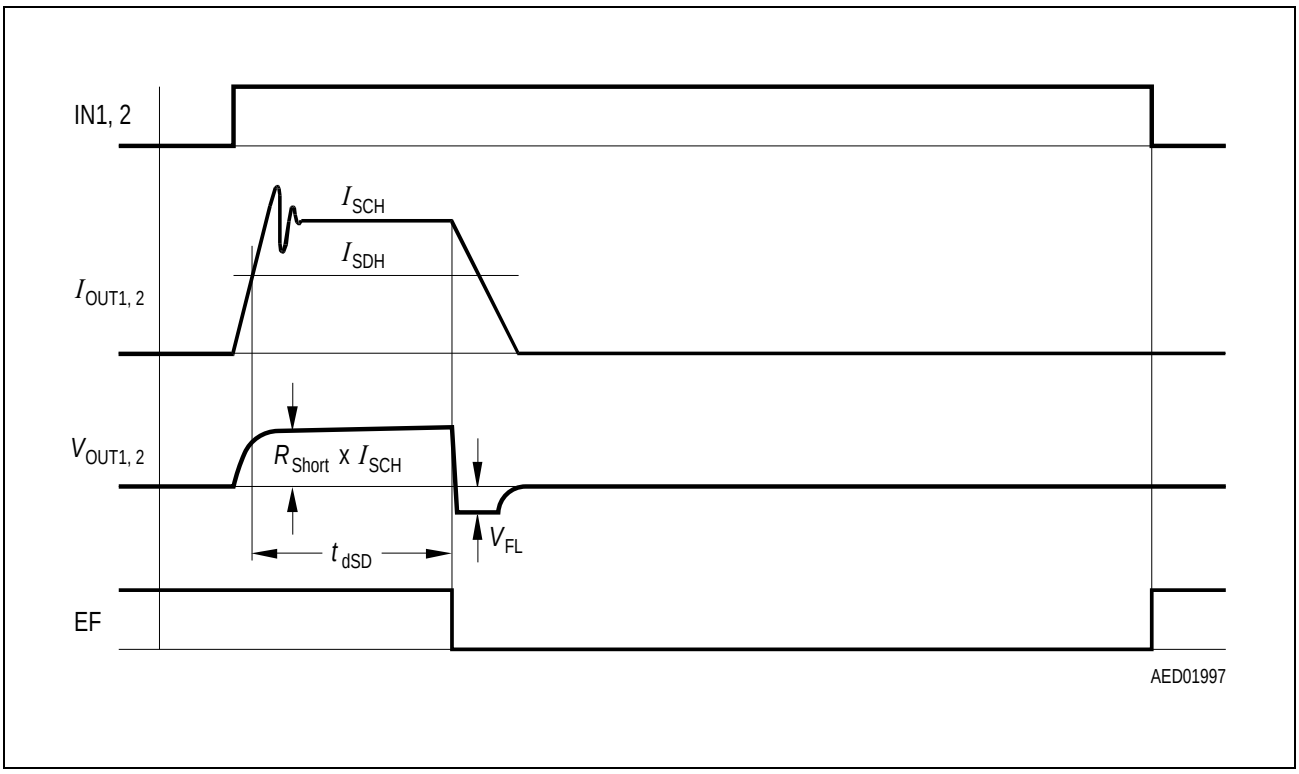


Figure 7 Timing Diagram for Output Shorted to Ground

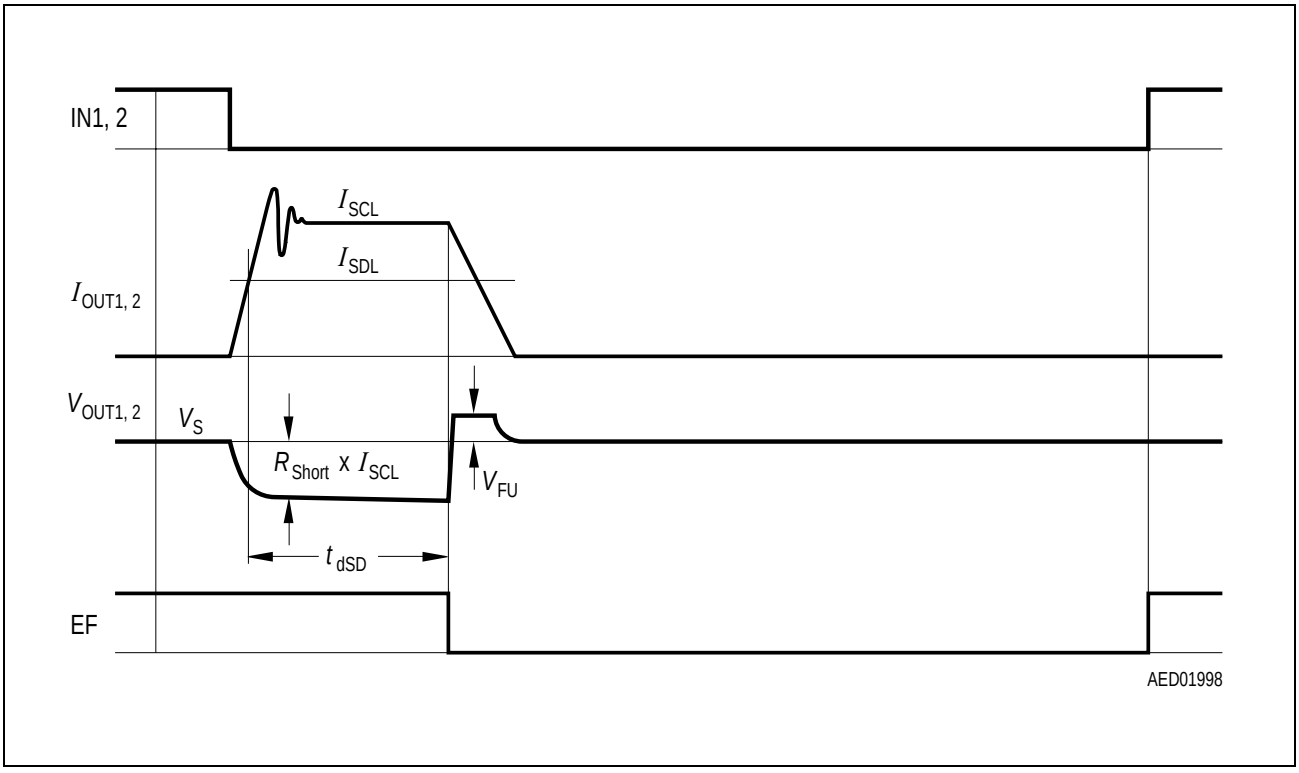
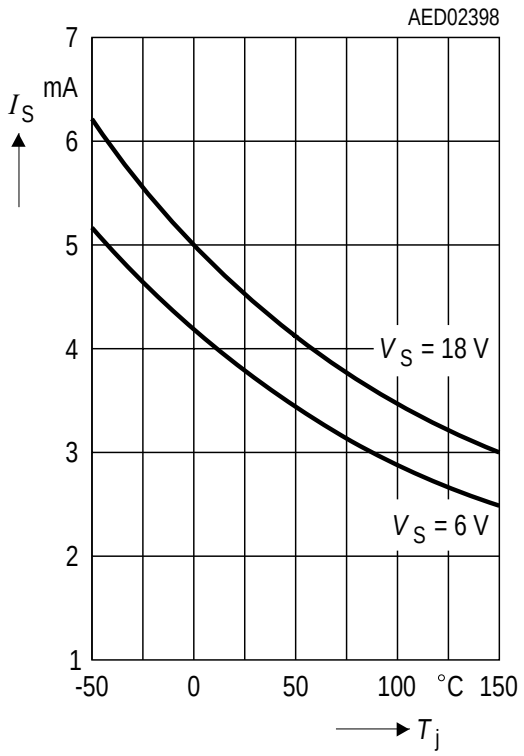


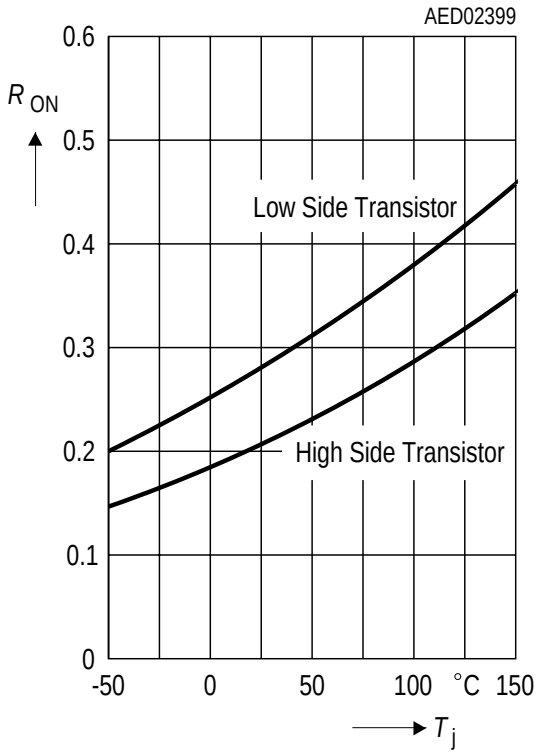
Figure 8 Timing Diagram for Output Shorted to V_S

Diagrams

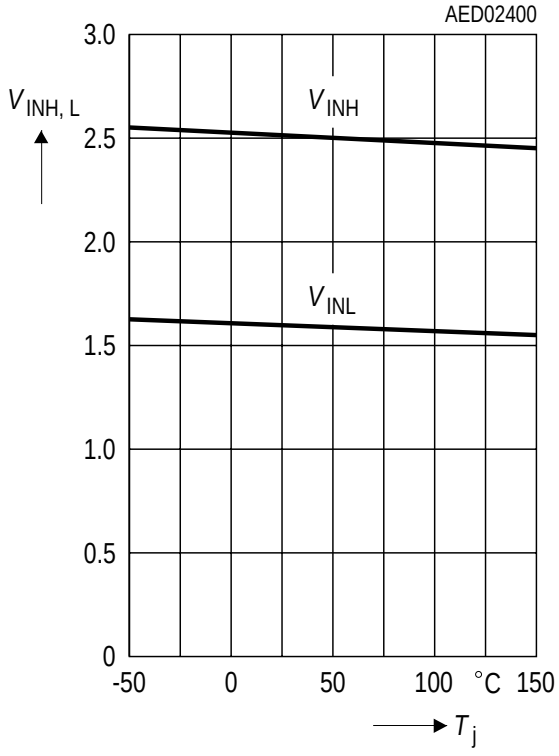
Quiescent Current I_S (Active) versus Junction Temperature T_j



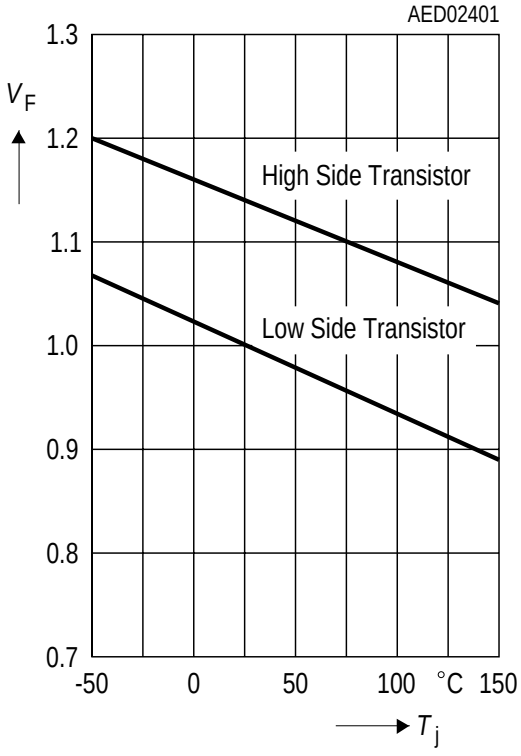
Static Drain-Source ON-Resistance versus Junction Temperature T_j



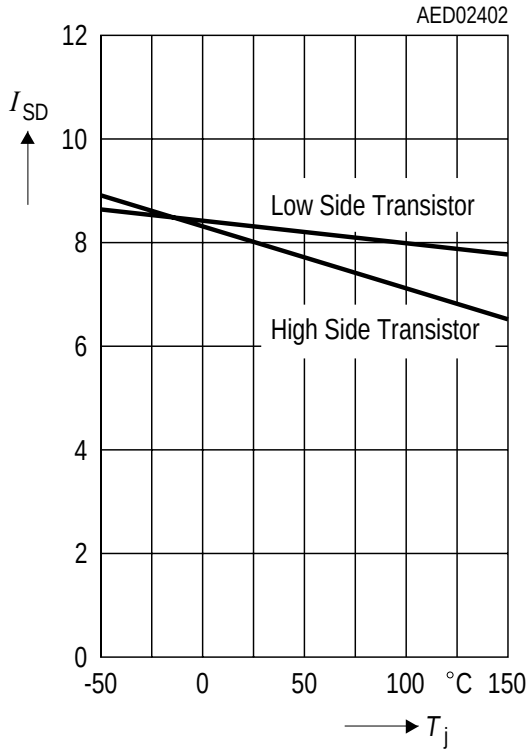
Input Switching Thresholds $V_{INH, L}$ versus Junction Temperature T_j



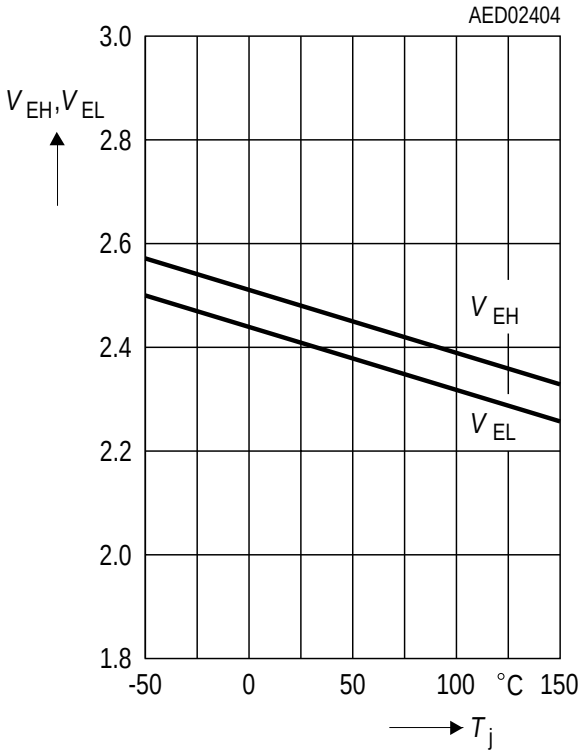
Clamp Diode Forward Voltage V_F versus Junction Temperature T_j



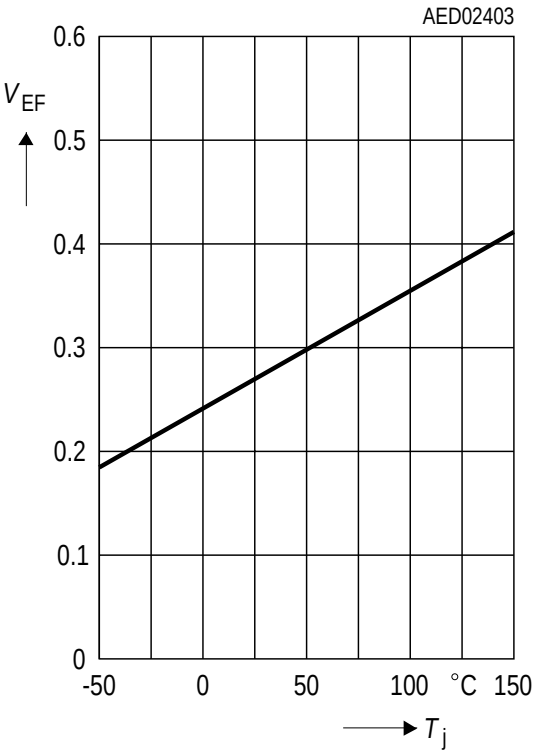
Overcurrent Shutdown Threshold I_{SD} versus Junction Temperature T_j



Switching Threshold V_{EH}, V_{EH} versus Junction Temperature T_j



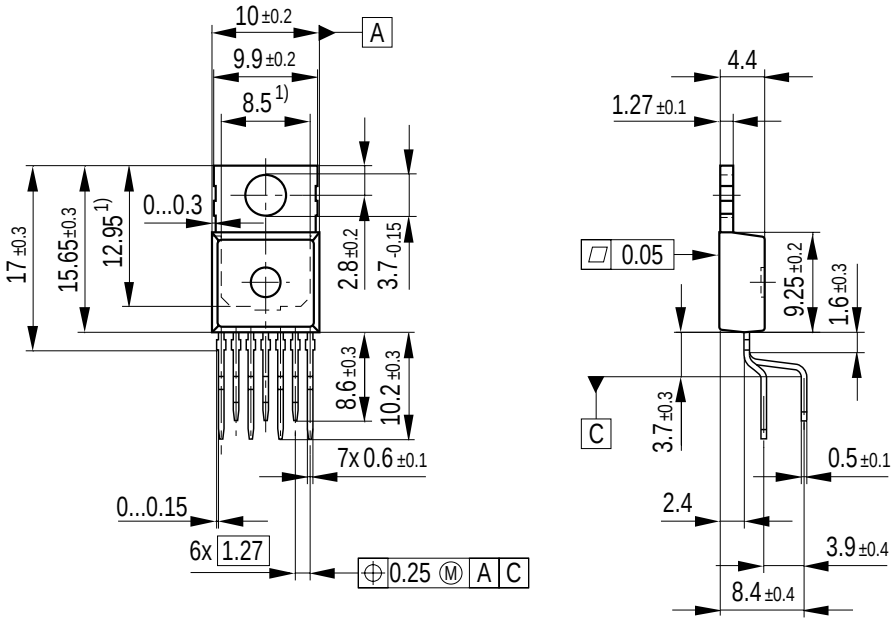
Error-Flag Saturation Output Voltage V_{EF} versus Junction Temperature T_j



4 Package Outlines

P-TO220-7-11

(Plastic Transistor Single Outline Package)



1) Typical
Metal surface min. X=7.25, Y=12.3
All metal surfaces tin plated, except area of cut.

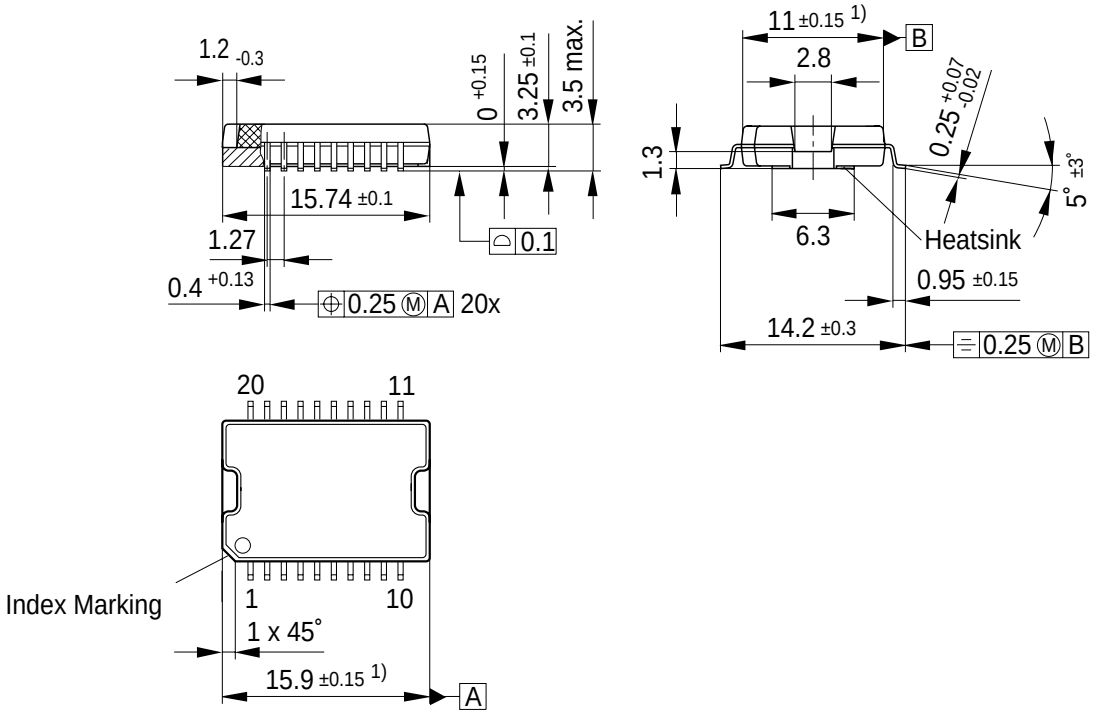
GPT09083

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

Dimensions in mm

P-DSO-20-12
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

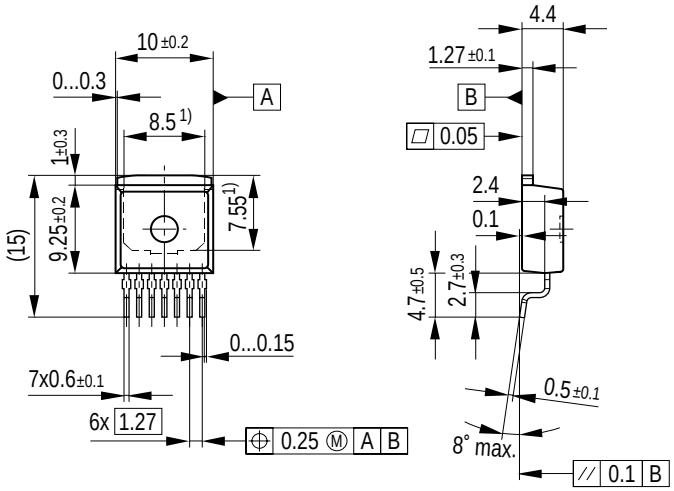
GPS05791

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

P-TO263-7-1 Option E3180
(Plastic Transistor Single Outline Package)



1) Typical
Metal surface min. X=7.25, Y=6.9
All metal surfaces tin plated, except area of cut.

GPT09114

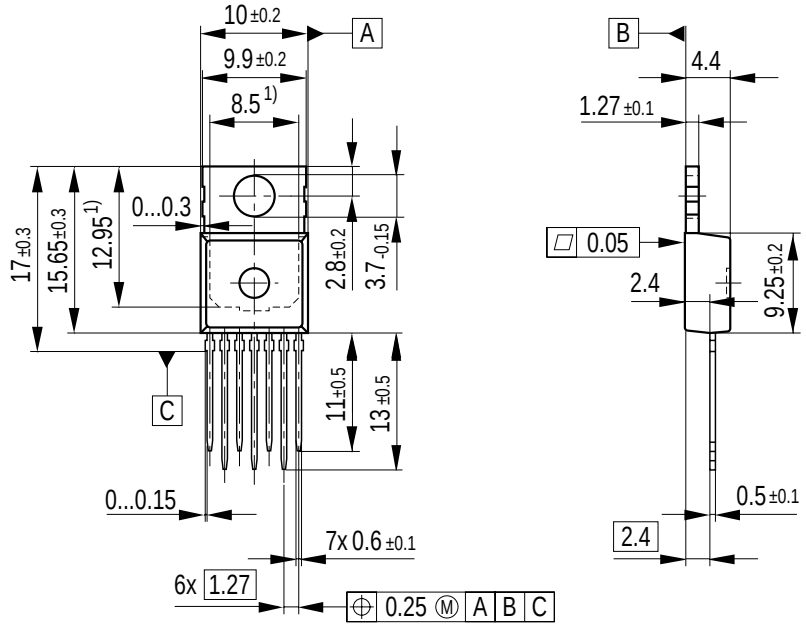
Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

P-TO220-7-12

(Plastic Transistor Single Outline Package)



1) Typical
Metal surface min. X=7.25, Y=12.3
All metal surfaces tin plated, except area of cut.

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

Dimensions in mm