Integrated Circuit Systems, Inc.

ICS9248-112

Preliminary Product Preview

Frequency Generator & Integrated Buffers for Celeron & PII/III™

Recommended Application:
810/810E type chipset.

Output Features:

- 2- CPUs @2.5V, up to 150MHz.
- 9 - SDRAM @ 3.3V, up to150MHz including 1 free running
- 8 - PCICLK @ 3.3V
- 1 - IOAPIC @ 2.5V, PCI or PCI/2 MHz
- 2 - 3V66MHz @ 3.3V, 2X PCI MHz
- 1- 48MHz, @3.3V fixed.
- 1- 24MHz, @3.3V fixed
- 1- REF @3.3V, 14.318MHz.

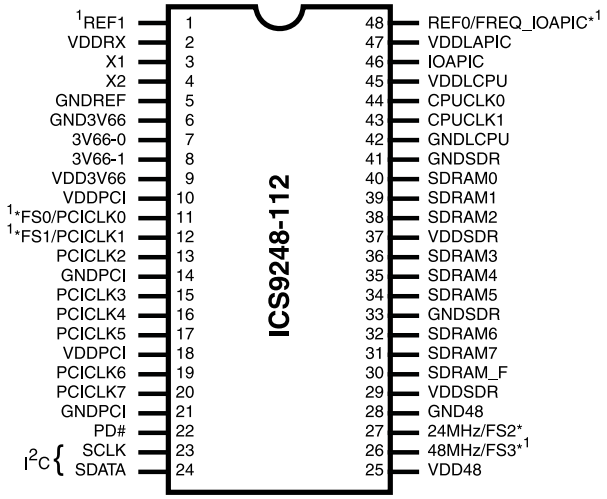
Features:

- Up to 166MHz frequency support
- Support FS0-FS3 strapping status bit for I^2C read back.
- Support power management: Through Power down Mode from I^2C programming.
- Spread spectrum for EMI control (± 0.25% center).
- Spread can be enabled or disabled to all 32 frequencies throuth I^2C.
- Uses external 14.318MHz crystal

Skew Specifications:

- CPU – CPU: <175ps
- SDRAM - SDRAM: < 250ps
- 3V66 – 3V66: <175ps
- PCI – PCI: <500ps
- CPU-SDRAM<500ps
- For group skew specifications, please refer to group timing relationship.

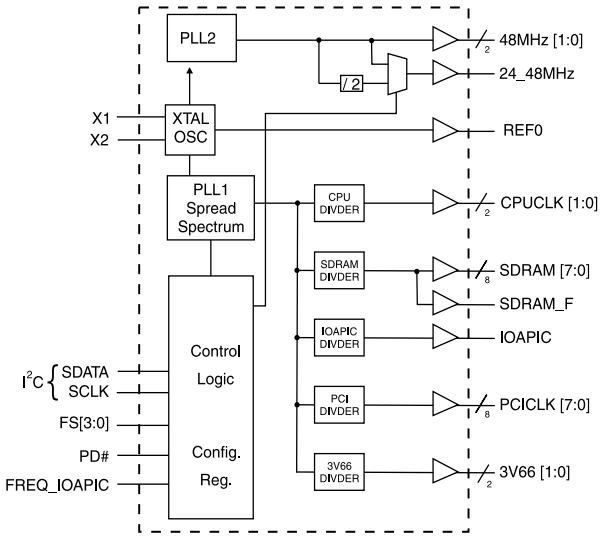
Pin Configuration



48-Pin 300mil SSOP

* These inputs have a 120K pull up to VDD.
1 These are double strength.

Block Diagram



Functionality

FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	3V66 (MHz)	PCICLK (MHz)	IOAPIC 1=PCICLK/2 (MHz)	IOAPIC 0=PCICLK (MHz)
0	0	0	0	66.80	100.20	66.80	33.40	16.70	33.40
0	0	0	1	68.00	102.00	68.00	34.00	17.00	34.00
0	0	1	0	100.30	100.30	66.87	33.43	16.72	33.43
0	0	1	1	103.00	103.00	68.67	34.33	17.17	34.33
0	1	0	0	133.73	100.30	66.87	33.43	16.72	33.43
0	1	0	1	145.00	108.75	72.50	36.25	18.13	36.25
0	1	1	0	133.73	100.30	66.87	33.43	16.72	33.43
0	1	1	1	137.33	103.00	68.67	34.33	17.17	34.33
1	0	0	0	140.00	105.00	70.00	35.00	17.50	35.00
1	0	0	1	140.00	140.00	93.33	46.67	23.33	46.67
1	0	1	0	118.00	118.00	78.67	39.33	19.67	39.33
1	0	1	1	124.00	124.00	82.67	41.33	20.67	41.33
1	1	0	0	133.70	133.70	89.13	44.57	22.28	44.57
1	1	0	1	137.00	137.00	91.33	45.67	22.83	45.67
1	1	1	0	150.00	112.50	75.00	37.50	18.75	37.50
1	1	1	1	72.50	108.75	72.50	36.25	18.13	36.25

Additional frequencies selectable through I^2C programming.

ICS9248-112

Preliminary Product Preview

General Description

The **ICS9248-112** is the single chip clock solution for designs using the 810/810E style chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9248-112** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

Power Groups

GNDREF, VDDREF = REF0, X1, X2
GNDPCI , VDDPCI = PCICLK [9:0]
GNDSDR, VDDSDR = SDRAM [7:0], SDRAM_F, supply for PLL core
GND3V66 , VDD3V66 = 3V66
GND48 , VDD48 = 48MHz, 24_48MHz,
VDDLAPIC = IOAPIC
GNDLCPU , VDDLCPU = CPUCLK [1:0]

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	REF1	OUT	3.3V, 14.318MHz reference clock output.
2, 9, 10, 18, 25, 29, 37	VDD	PWR	3.3V power supply
3	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2
4	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF)
5, 6, 14, 21, 28, 33, 41	GND	PWR	Ground pins for 3.3V supply
7, 8	3V66 (1:0)	OUT	3.3V clock outputs for HUB running at 2XPCI MHz
11	PCICLK0[1]	OUT	3.3V PCI clock outputs, with Synchronous CPUCLKS
	FS0	IN	Logic input frequency select bit. Input latched at power on.
12	PCICLK1[1]	OUT	3.3V PCI clock outputs, with Synchronous CPUCLKS
	FS1	IN	Logic input frequency select bit. Input latched at power on.
13, 15, 16, 17, 19, 20	PCICLK (2:7)	OUT	3.3V PCI clock outputs, with Synchronous CPUCLKS
22	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
23	SCLK	IN	Clock input of I^2C input
24	SDATA	IN	Data input for I^2C serial input.
26	48MHz	OUT	3.3V Fixed 48MHz clock output for USB
	FS3	IN	Logic input frequency select bit. Input latched at power on.
27	FS2	IN	Logic input frequency select bit. Input latched at power on.
	24MHz	OUT	3.3V fixed 24MHz output
30	SDRAM_F	OUT	3.3V free running SDRAM not affected by I^2C
40, 39, 38, 36, 35, 34, 32, 31	SDRAM (7:0)	OUT	3.3V outputs
42	GNDL	PWR	Ground for 2.5V power supply for CPU & APIC
43, 44	CPUCLK (1:0)	OUT	2.5V Host bus clock output.
45, 47	VDDL	PWR	2.5V power supply for CPU, IOAPIC
46	IOAPIC	OUT	2.5V clock output
48	REF0[1]	OUT	3.3V, 14.318MHz reference clock output.
	FREQ_IOAPIC	IN	"If FREQ_APIC = 0, APIC Clock = PCICLK If FREQ_APIC = 1, APIC Clock = PCICLK/2 (default)"

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description												PWD
	Bit (2, 7:4)					CPUCLK (MHz)	SDRAM (MHz)	3V66 (MHz)	PCICLK (MHz)	FREQ_IOAPIC (MHz)		Spread Precentage	
										1	0		
Bit 2, Bit 7:4	0	0	0	0	0	66.80	100.20	66.80	33.40	16.70	33.40	+/- 0.25% Center	XXX Note1
	0	0	0	0	1	68.00	102.00	68.00	34.00	17.00	34.00	+/- 0.25% Center	
	0	0	0	1	0	100.30	100.30	66.87	33.43	16.72	33.43	+/- 0.25% Center	
	0	0	0	1	1	103.00	103.00	68.67	34.33	17.17	34.33	+/- 0.25% Center	
	0	0	1	0	0	133.73	100.30	66.87	33.43	16.72	33.43	+/- 0.25% Center	
	0	0	1	0	1	145.00	108.75	72.50	36.25	18.13	36.25	+/- 0.25% Center	
	0	0	1	1	0	133.73	100.30	66.87	33.43	16.72	33.43	+/- 0.25% Center	
	0	0	1	1	1	137.33	103.00	68.67	34.33	17.17	34.33	+/- 0.25% Center	
	0	1	0	0	0	140.00	105.00	70.00	35.00	17.50	35.00	+/- 0.25% Center	
	0	1	0	0	1	140.00	140.00	93.33	46.67	23.33	46.67	+/- 0.25% Center	
	0	1	0	1	0	118.00	118.00	78.67	39.33	19.67	39.33	+/- 0.25% Center	
	0	1	0	1	1	124.00	124.00	82.67	41.33	20.67	41.33	+/- 0.25% Center	
	0	1	1	0	0	133.70	133.70	89.13	44.57	22.28	44.57	+/- 0.25% Center	
	0	1	1	0	1	137.00	137.00	91.33	45.67	22.83	45.67	+/- 0.25% Center	
	0	1	1	1	0	150.00	112.50	75.00	37.50	18.75	37.50	+/- 0.25% Center	
	0	1	1	1	1	72.50	108.75	72.50	36.25	18.13	36.25	+/- 0.25% Center	
	1	0	0	0	0	75.00	112.50	75.00	37.50	18.75	37.50	+/- 0.25% Center	
	1	0	0	0	1	83.00	83.00	27.67	13.83	6.92	13.83	+/- 0.25% Center	
	1	0	0	1	0	110.00	110.00	73.33	36.67	18.33	36.67	+/- 0.25% Center	
	1	0	0	1	1	120.00	120.00	80.00	40.00	20.00	40.00	+/- 0.25% Center	
	1	0	1	0	0	125.00	125.00	83.33	41.67	20.83	41.67	+/- 0.25% Center	
	1	0	1	0	1	69.25	103.88	69.25	34.63	17.31	34.63	+/- 0.25% Center	
	1	0	1	1	0	70.00	105.00	70.00	35.00	17.50	35.00	+/- 0.25% Center	
	1	0	1	1	1	76.67	115.00	76.67	38.33	19.17	38.33	+/- 0.25% Center	
	1	1	0	0	0	145.00	145.00	96.67	48.33	24.17	48.33	+/- 0.25% Center	
	1	1	0	0	1	66.50	99.75	66.50	33.25	16.63	33.25	+/- 0.25% Center	
	1	1	0	1	0	150.00	150.00	100.00	50.00	25.00	50.00	+/- 0.25% Center*	
	1	1	0	1	1	99.75	99.75	66.50	33.25	16.63	33.25	+/- 0.25% Center*	
	1	1	1	0	0	155.00	155.00	103.33	51.67	25.83	51.67	+/- 0.25% Center	
	1	1	1	0	1	166.50	166.50	111.00	55.50	27.75	55.50	+/- 0.25% Center	
	1	1	1	1	0	153.33	115.00	76.67	38.33	19.17	38.33	+/- 0.25% Center	
	1	1	1	1	1	133.00	99.75	66.50	33.25	16.63	33.25	+/- 0.25% Center*	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 2, 7:4												0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled ± 0.25% Center Spread												1
Bit 0	0 - Running 1- Tristate all outputs												0

Note 1: Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

* These frequencies with spread enabled are equal to original Intel defined frequency with -0.5% down spread.

I^2C is a trademark of Philips Corporation

Byte 1: Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS3#
Bit 6	-	X	FS0#
Bit 5	-	X	FS2#
Bit 4	27	1	24MHz
Bit 3	-	1	(Reserved)
Bit 2	26	1	48MHz
Bit 1	-	1	(Reserved)
Bit 0	30	1	SDRAM_F

Byte 2: SDRAM, Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	31	1	SDRAM7
Bit 6	32	1	SDRAM6
Bit 5	34	1	SDRAM5
Bit 4	35	1	SDRAM4
Bit 3	36	1	SDRAM3
Bit 2	38	1	SDRAM2
Bit 1	39	1	SDRAM1
Bit 0	40	1	SDRAM0

Byte 3: PCI, Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	20	1	PCICLK7
Bit 6	19	1	PCICLK6
Bit 5	17	1	PCICLK5
Bit 4	16	1	PCICLK4
Bit 3	15	1	PCICLK3
Bit 2	13	1	PCICLK2
Bit 1	12	1	PCICLK1
Bit 0	11	1	PCICLK0

Byte 4: Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	(Reserved)
Bit 6	8	1	3V66_1
Bit 5	7	1	3V66_0
Bit 4	-	X	FREQ_IOAPIC#
Bit 3	46	1	IOAPIC
Bit 2	-	X	FS1#
Bit 1	43	1	CPUCLK1
Bit 0	44	1	CPUCLK0

Byte 5: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	1	Reserved
Bit6	-	1	Reserved
Bit5	-	1	Reserved
Bit4	-	1	Reserved
Bit3	-	1	Reserved
Bit2	-	1	Reserved
Bit1	-	1	Reserved
Bit0	-	1	Reserved

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inferted logic load of the input frequency select pin conditions.

Byte 6: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

Note: Don't write into this register, writing into this register can cause malfunction

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-112 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

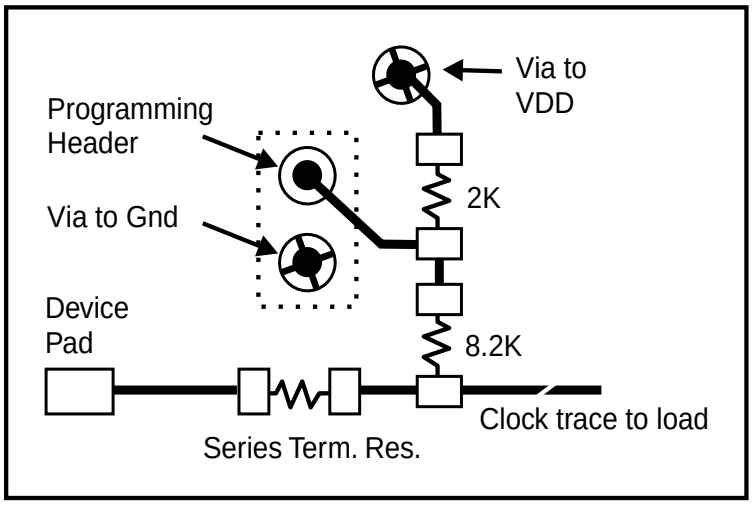
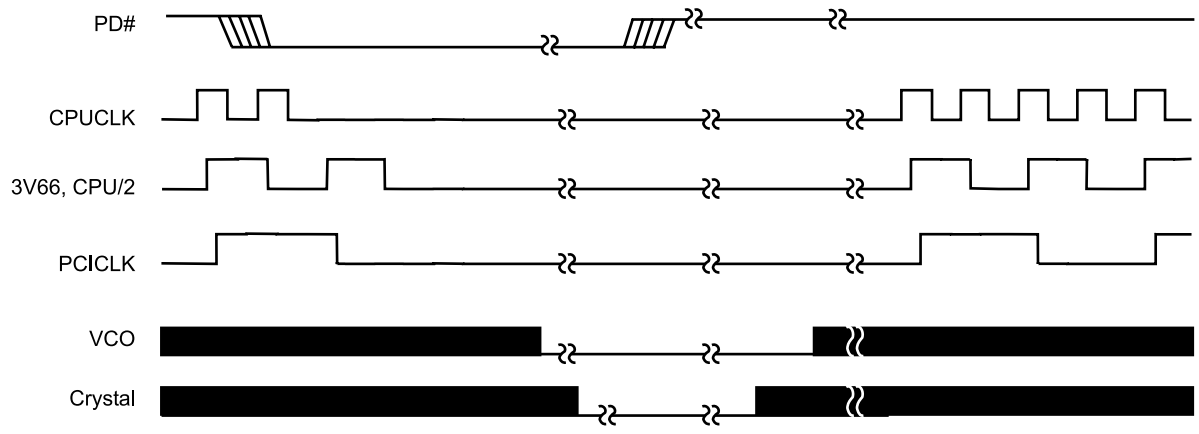


Fig. 1

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

Absolute Maximum Ratings

Core Supply Voltage ..... 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Group Timing Relationship Table

Group	CPU 66MHz		CPU 100MHz		CPU 133MHz	
	Offset	Tolerance	Offset	Tolerance	Offset	Tolerance
CPU to SDRAM	2.5ns	500ps	5.0ns	500ps	0.0ns	500ps
CPU to 3V66	7.5ns	500ps	5.0ns	500ps	0.0ns	500ps
SDRAM to 3V66	0.0ns	500ps	0.0ns	500ps	0.0ns	500ps
3V66 to PCI	1.5-3.5ns	500ps	1.5-3.5ns	500ps	1.5-3.5ns	500ps
PCI to PCI	0.0ns	1.0ns	0.0ns	1.0ns	0.0ns	1.0ns
USB & DOT	Asynch	N/A	Asynch	N/A	Asynch	N/A

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V ±5%, VDDL=2.5 V± 5%(unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66M		60	100	mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; With input address to Vdd or GND		400	600	µA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{out}	Out put pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	mS
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.			3	mS
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS
Delay	t_{PZH},t_{PZH}	output enable delay (all outputs)	1		10	nS
	t_{PLZ},t_{PZH}	output disable delay (all outputs)	1		10	nS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH@MIN}$= 1.0V , $V_{OH@MAX}$= 2.375V	-27		-27	mA
Output Low Current	I_{OL2B}	$V_{OL@MIN}$= 1.2V , $V_{OL@MAX}$= 0.3V	27		30	mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 0.4 V, V_{OL} = 2.0 V	0.4		1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	50	55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V			250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			175	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP4B}[1]	$V_O = V_{DD}*(0.5)$	9		30	Ω
Output Impedance	R_{DSN4B}[1]	$V_O = V_{DD}*(0.5)$	9		30	Ω
Output High Voltage	$V_{OH4\B}$	I_{OH} = -5.5 mA	2			V
Output Low Voltage	V_{OL4B}	I_{OL} = 9.0 mA			0.4	V
Output High Current	I_{OH4B}	$V_{OH@\,min}$ = 1.0 V, $V_{OH@\,MAX}$ = 2.375 V	-27		-27	mA
Output Low Current	I_{OL4B}	$V_{OL@\,MIN}$ = 1.2 V, $V_{OL@\,MAX=}$ 0.3 V	27		30	mA
Rise Time	t_{r4B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time	t_{f4B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4		1.6	ns
Duty Cycle	d_{t4B}[1]	V_T = 1.25 V	45		55	%
Jitter	$t_{jcyc-cyc}$	V_T = 1.25 V			500	ps
Skew	t_{sk4}[1]				250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP3}[1]	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output Impedance	R_{DSN3}[1]	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH3}	$V_{OH\,@MIN}$= 2.0 V, $V_{OH@\,MAX}$=3.135 V	-54		-46	mA
Output Low Current	I_{OL3}	$V_{OL@\,MIN}$= 1.0 V, $V_{OL@\,MAX}$=0.4 V	54		53	mA
Rise Time	T_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4		1.6	ns
Fall Time	T_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4		1.6	ns
Duty Cycle	D_{t3}[1]	V_T = 1.5 V	45		55	%
Skew	T_{sk3}[1]	V_T = 1.5 V			250	ps
Jitter	$t_j$cyc-cyc	V_T = 1.5 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			500	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps

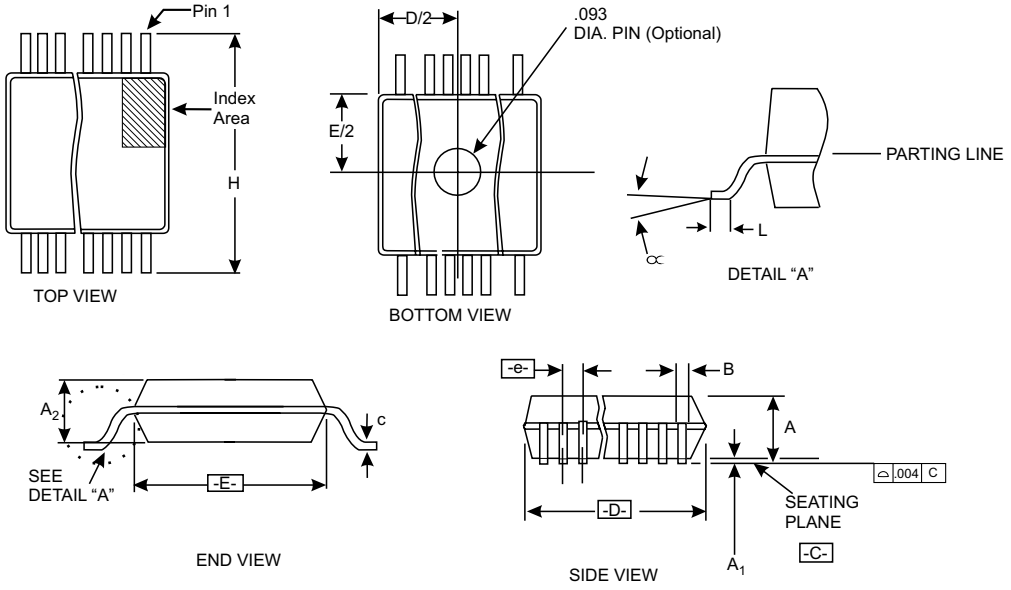
[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - REF, 48MHz

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 10 -20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output Impedance	R_{DSN5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = 1 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = -1 mA			0.4	V
Output High Current	I_{OH5}	$V_{OH@MIN}$=1 V, $V_{OH@MAX}$= 3.135 V	-29		-23	mA
Output Low Current	I_{OL5}	$V_{OL@MIN}$=1.95 V, $V_{OL@MIN}$=0.4 V	29		27	mA
Rise Time	t_{r5}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.8	4	nS
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.7	4	nS
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	45		55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V; Fixed Clocks			500	pS
	$t_{jcyc-cyc}$[1]	V_T = 1.5 V; Ref Clocks			1000	pS
Skew	T_{sk}	V_T = 1.5 V			250	pS

[1]Guarenteed by design, not 100% tested in production.



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.102	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.087	.090	.094					
B	.008	-	.0135					
c	.005	-	.010					
D	See Variations							
E	.291	.295	.299					
e	0.025 BSC							
H	.395	-	.420					
h	.010	.013	.016					
L	.020	-	.040					
N	See Variations							
∝	0°	-	8°					

"For current dimensional specifications, see JEDEC 95."

Dimensions in inches

48 Pin 300 mil SSOP Package

Ordering Information

ICS9248yF-112-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device