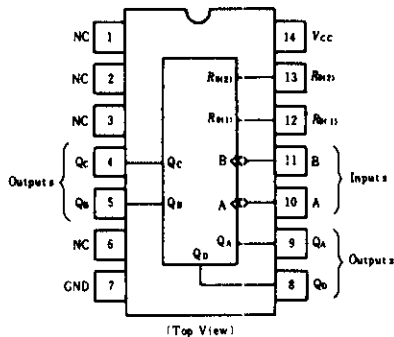


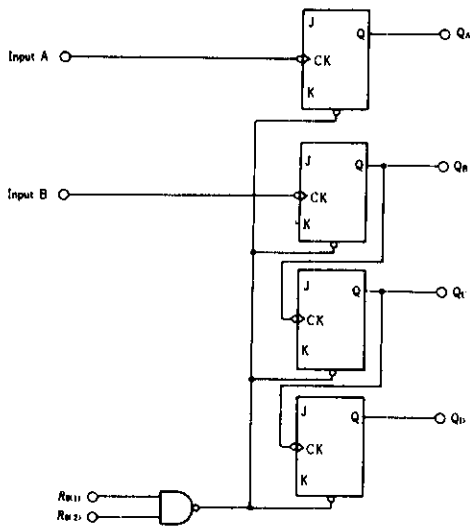
HD74LS293 ● 4-bit Binary Counters

This counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and divide-by-eight counter. This counter has a gated zero reset. To use the maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.

■ PIN ARRANGEMENT



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7.0	V
Input voltage	R_0 Inputs	7.0	V
	A, B Inputs	5.5	V
Operating temperature range	T_{op}	-20 ~ +75	°C
Storage temperature range	T_{stg}	-65 ~ +150	°C

■ FUNCTION TABLE

● Reset/Count

Reset Input		Outputs			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	Count			
X	L	Count			

● BCD Count Sequence

Count	Outputs				Count	Outputs			
	Q_D	Q_C	Q_B	Q_A		Q_D	Q_C	Q_B	Q_A
0	L	L	L	L	8	H	L	L	L
1	L	L	L	H	9	H	L	L	H
2	L	L	H	L	10	H	L	H	L
3	L	L	H	H	11	H	L	H	H
4	L	H	L	L	12	H	H	L	L
5	L	H	L	H	13	H	H	L	H
6	L	H	H	L	14	H	H	H	L
7	L	H	H	H	15	H	H	H	H

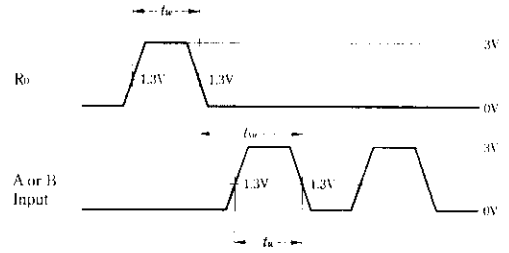
- Notes) 1. H; high level, L; low level, X; irrelevant.
2. Output Q_A is connected to input B.

HD74LS293

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit	
Output current	I_{OH}	—	—	-400	μA	
Output current	I_{OL}	—	—	8	mA	
Count frequency	A input	f_{count}	0	—	32	MHz
	B input		0	—	16	
Pulse width	A input	t_w	15	—	—	ns
	B input		30	—	—	
	Reset inputs		15	—	—	
Setup time	t_{su}	25	—	—	ns	

TIMING DEFINITION



ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ C$)

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	V_{IH}		2.0	—	—	V	
	V_{IL}		—	—	0.8	V	
Output voltage	V_{OH}	$V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = -400\mu A$	2.7	—	—	V	
	V_{OL}	$V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V$	$I_{OL} = 4mA^{**}$	—	—	0.4	V
			$I_{OL} = 8mA^{**}$	—	—	0.5	
Input current	Any Reset	I_{IL}	$V_{CC} = 5.25V, V_I = 0.4V$	—	—	-0.4	mA
	A input			—	—	-2.4	
	B input			—	—	-1.6	
	Any Reset	I_{IH}	$V_{CC} = 5.25V, V_I = 2.7V$	—	—	20	μA
	A input			—	—	40	
	B input			—	—	40	
	Any Reset	I_I	$V_{CC} = 5.25V$	$V_I = 7V$	—	—	0.1
A input	—				—	0.2	
B input	—				—	0.2	
Short-circuit output current	I_{OS}	$V_{CC} = 5.25V$	-20	—	-100	mA	
Supply current***	I_{CC}	$V_{CC} = 5.25V$	—	9	15	mA	
Input clamp voltage	V_{IK}	$V_{CC} = 4.75V, I_{IN} = -18mA$	—	—	-1.5	V	

* $V_{CC} = 5V, T_a = 25^\circ C$

** Q_A output is tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

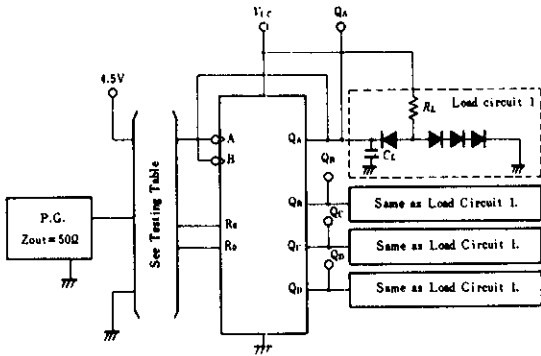
*** I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V, T_a = 25^\circ C$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum count frequency	f_{max}	A	Q_A	$C_L = 15pF, R_L = 2k\Omega$	32	42	—	MHz
		B	Q_B		16	—	—	
Propagation delay time	t_{PLH}	A	Q_A		—	10	16	ns
			Q_D		—	12	18	
	t_{PHL}	A	Q_D		—	46	70	ns
			Q_B		—	46	70	
	t_{PLH}	B	Q_B		—	10	16	ns
			Q_C		—	14	21	
	t_{PHL}	B	Q_C		—	21	32	ns
			Q_D		—	23	35	
	t_{PLH}	B	Q_D	—	34	51	ns	
				—	34	51		
t_{PHL}	Set-to-0	$Q_A \sim Q_D$	—	26	40	ns		

■ TESTING METHOD

1) Test Circuit



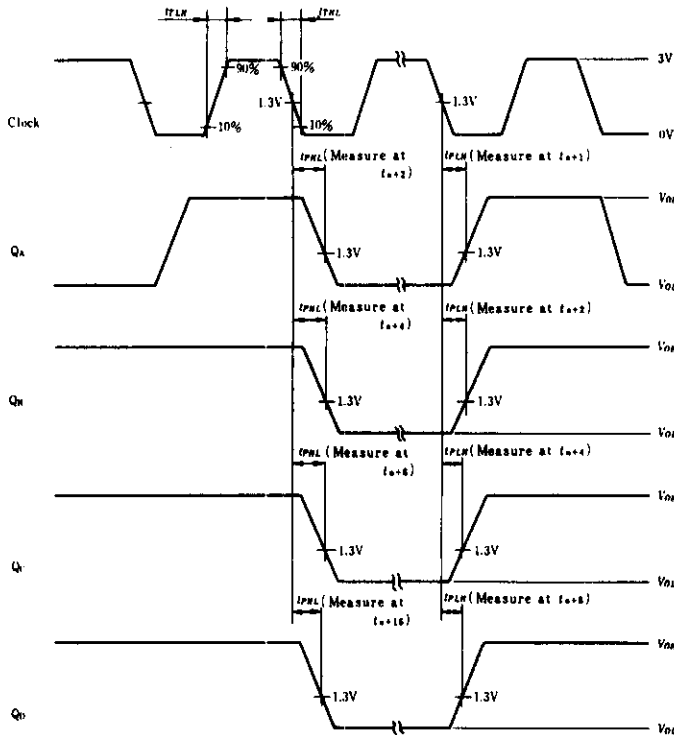
- Notes) 1. C_L includes probe and jig capacitance.
 2. All diodes are 1S2074 (H).

2) Testing Table

Item	From input to output	Inputs			Outputs			
		A	B	R_0	Q_A	Q_B	Q_C	Q_D
f_{max}	A→Q	IN	to Q_A	GND	OUT	OUT	OUT	OUT
	B→Q	4.5V	IN	GND	—	OUT	OUT	OUT
t_{PLH}	A→ Q_A	IN	to Q_A	GND	OUT	—	—	—
	A→ Q_D	IN	to Q_A	GND	—	—	—	OUT
t_{PHL}	B→ Q_B	4.5V	IN	GND	—	OUT	—	—
	B→ Q_C	4.5V	IN	GND	—	—	OUT	—
	B→ Q_D	4.5V	IN	GND	—	—	—	OUT
	R_0 → Q^{**}	IN*	to Q_A	IN	OUT	OUT	OUT	OUT

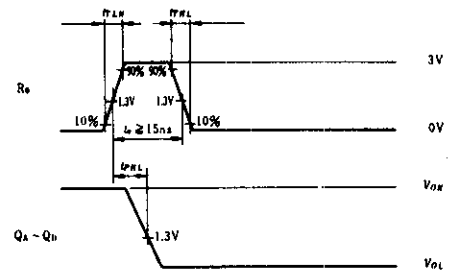
- * For initialized.
 ** Measured with each input and unused inputs at 4.5V.

Waveform 1. f_{max} , t_{PLH} , t_{PHL} (Clock→Q)

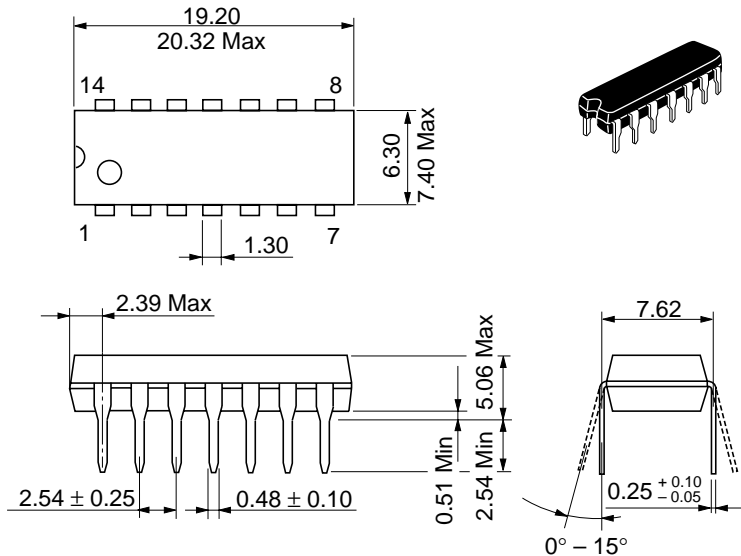


- Notes) 1. Input pulse: $t_{TLH} \leq 15ns$, $t_{THL} \leq 5ns$, $PRR=1MHz$, duty cycle=50% and: for f_{max} , $t_{TLH} = t_{THL} \leq 2.5ns$.
 2. t_m is reference bit time when all outputs are low.

Waveform 2. t_{PHL} (R_0 →Q)



- Note) $t_{TLH} \leq 15ns$, $t_{THL} \leq 5ns$



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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