VCO + phase comparator IC for PLL system

BU2374FV

BU2374FV is a VCO+phase comparator IC used to construct PLL system. PLL system is constructed and low jitter clocks can be generated by adopting external LPF and divider. Through a mechanism incorporated in this IC the output could be switched into quarter. Another function can set in the center point of frequency by adjusting external resistance.

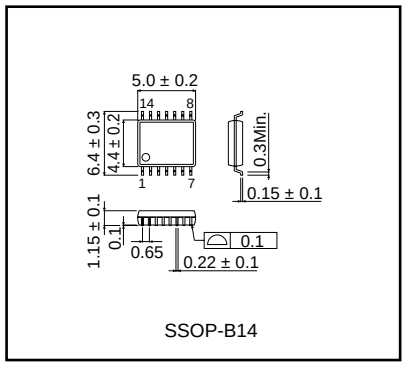
●Applications

TV

●Features

1) V_{DD}=3.3V±5% operating guaranteed
2) Oscillating range of VCO is 37MHz~60MHz
3) High-speed edge trigger type phase comparator
4) VCO can be fine-adjusted by external resistor.
5) VCO and phase comparator can be controlled independently.
6) Small SSOP-B14 package

●External dimensions (Unit : mm)



SSOP-B14

●Absolute maximum ratings (Ta=25°C)

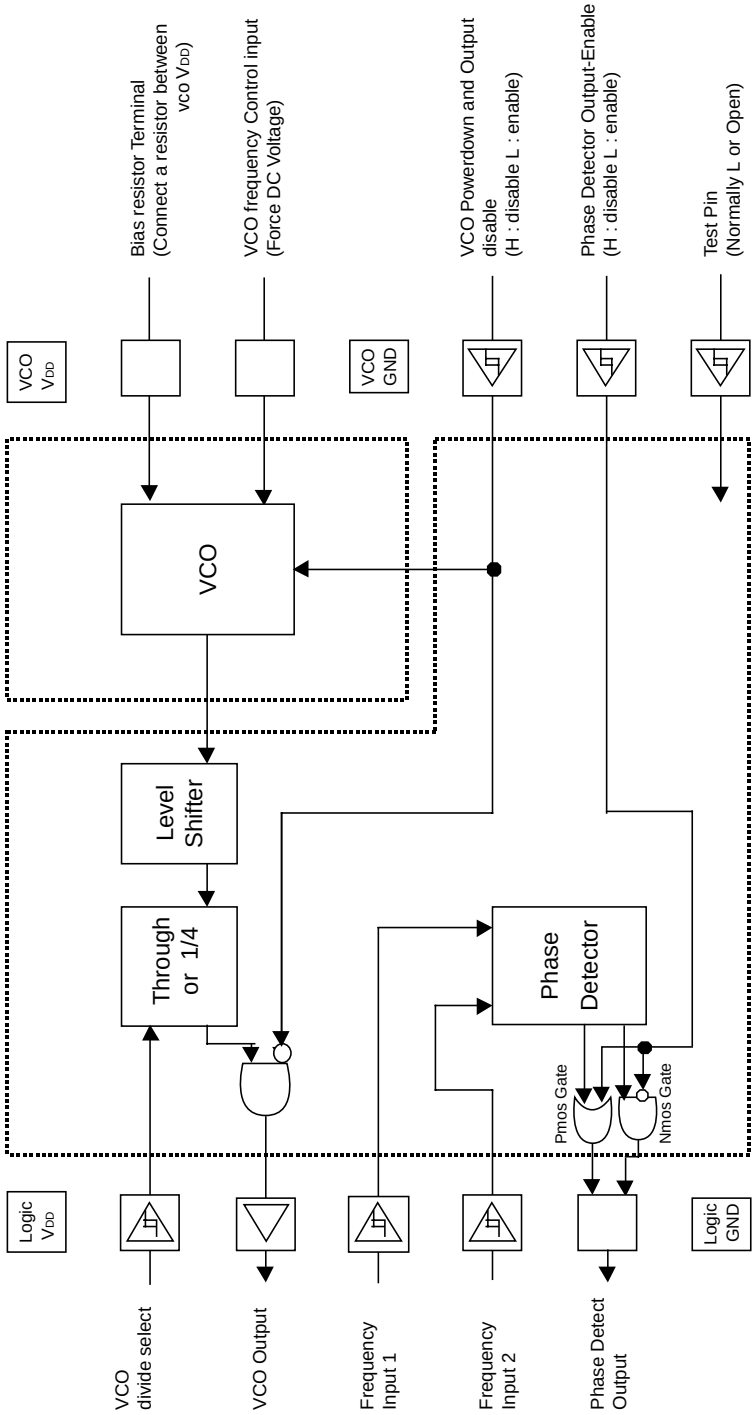
Parameter	Symbol	Limits	Unit
Applied voltalge	V_{DD}	–0.5 to +7.0	V
Inpuit voltage	V_{IN}	–0.5 to V_{DD}+0.5	V
Power dissipation	Pd	400*	mW
Storage temperature	Tstg	–30 to +125	°C

∗An operation is not guaranteed.
∗In case it is used at Ta=25°C or more, 4.0mW is reduceed at every 1°C.
∗Radiation resistance design is not used.
∗Power dissipation is measured when BU2374FV is placed on the board.

●Recommended operating conditions(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	3.15	–	3.45	V
Input H voltage range	V_{IH}	0.8V_{DD}	–	V_{DD}	V
Input L voltage range	V_{IL}	0	–	0.2V_{DD}	V
Operating temperature	Topr	–20	–	+75	°C
Output load	C_L	–	–	15	pF

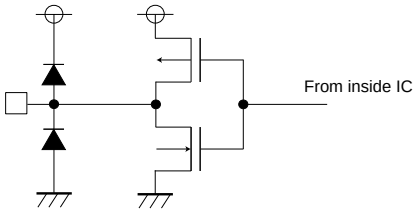
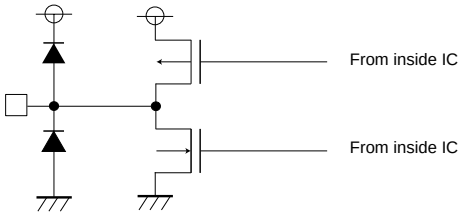
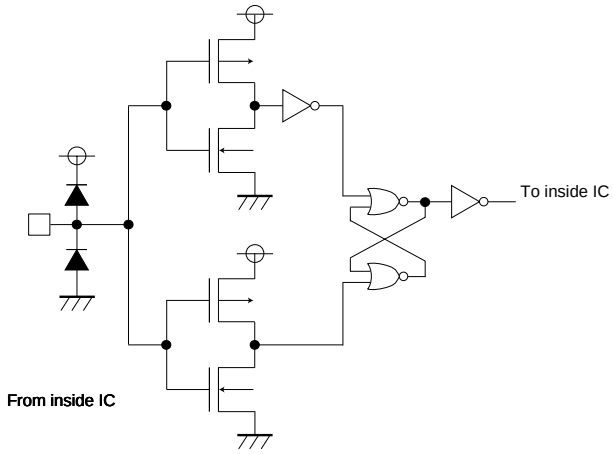
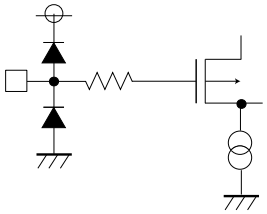
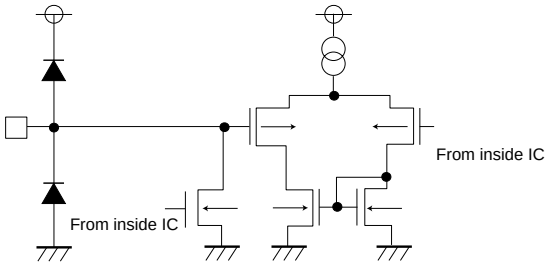
●**Block diagram**



●Pin descriptions

Pin No.	Pin name	Functions
1	LOGIC V_{DD}	Digital V_{DD}
2	SELECT	VCO output frequency select (H:1/4 output, L:1/1 output)
3	VCO OUT	VCO output
4	FIN-A	Input reference frequency is applied to Fin A
5	FIN-B	Input for VCO external counter output frequency
6	PFD_OUT	PD output
7	LOGIC_GND	Digital GND
8	TEST	TEST input with Pull-down resistor (Normaly OPEN or 'L')
9	PFD_INHIBIT	Contorol Pin for PD (H:PD disable (Hi impedance state), L:PD enable)
10	VCO_INHIBIT	VCO mode select (H:VCO OUT disable (L Fix), L:VCOOUT enable)
11	VCO_GND	GND for VCO (Analog GND)
12	VCO_IN	VCO control voltage input
13	BIAS	For adjusting VCO output frequency range (An external resistor connect between VCO_V_{DD} and BIAS)
14	VCO_V_{DD}	V_{DD} for VCO (Analog V_{DD})

●Input / output circuits

Pin No.	Equivalent circuit
Output Pin (Pin3)	
Output Pin (Pin6)	
Input Pin (Schmitt triger) (Pin2, 4, 5, 8, 9, 10) Pin8 : with pull-down resistance	
Input Pin (Pin12)	
Input Pin (Pin13)	

●**Electrical characteristics** (Unless otherwise noted,Ta=25°C, V_{CC}=3.3V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
VCO section						
VCO_OUT Output H voltage	V_{OH}	3.0	–	–	V	I_{OH}=–2.0mA
VCO_OUT Output L voltage	V_{OL}	–	–	0.3	V	I_{OL}=2.0mA
input current (VCO_INHIBIT, SELECT)	IIH, IIL	–	–	±1	μA	
input impedance (VCO_IN)	Zi	–	10	–	MΩ	
VCO current consumption (inhibit)	I_{DD}(INH)	–	–	1	μA	at VCO_INHIBIT=V_{DD} PFD_INHIBIT=V_{DD}
VCO current consumption (normal operation)	I_{DD}(vco)	–	12.5	–	mA	Output 50MHz
VCO control voltage	VI(vco_in)	0.5	–	V_{DD}–0.5	V	
VCO frequency range	frange	37	–	60	MHz	
Bias Resistor range	Rbias	2.0	–	3.0	KΩ	＊1
Frequency sersibility	β1	–	23	–	MHz/V	＊2
Output duty	Duty	45	50	55	%	at 1/2 V_{DD} point
Output Rise-time	tr	–	2.5	–	nsec	Time is from V_{DD}＊0.2 to vdd＊0.8
Output Fall-time	tf	–	2.5	–	nsec	Time is from V_{DD}＊0.8 to vdd＊0.2

＊1 Value of design guarantee (all guarantee range)
Bias R=2.0kΩ 37MHz to 54MHz
Bias R=2.4kΩ 45MHz to 58MHz
Bias R=3.0kΩ 53MHz to 60MHz

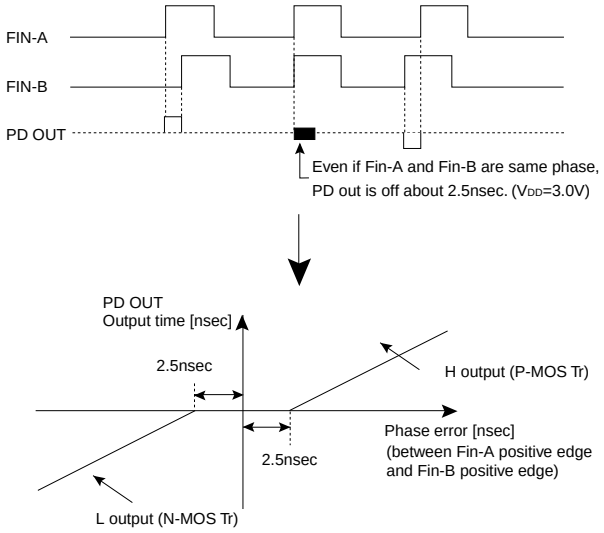
＊2 Frequency sersibility { f1(VCOIN=2.0V)–f2(VCOIN=1.0V)} / 1.0V

＊3 When FSEL is H and output frequency is 1/4, culculate

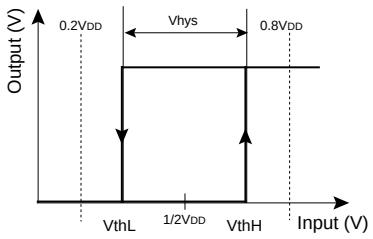
(Unless otherwise noted, Ta=25°C, V_{CC}=3.3V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
PFD section						
PFD_OUT Output H voltage	V_{OH}	3.0	–	–	V	I_{OH}=–2.0mA
PFD_OUT Output L voltage	V_{OL}	–	–	0.3	V	I_{OL}=2.0mA
input current (PFD_INHIBIT, FIN A, FIN B)	IIH, IIL	–	–	±1	μA	
PFD current consumption (inhibit)	I_{DD}(INH)	–	–	1	μA	at VCO_INHIBIT=V_{DD} PFD_INHIBIT=V_{DD} FIN_A and B=GND
PFD current consumption (normal operation)	I_{DD}(vco)	–	0.5	–	mA	FIN_A and FIN_B=1MHz
PFD Function	–	–	–	–	–	∗4

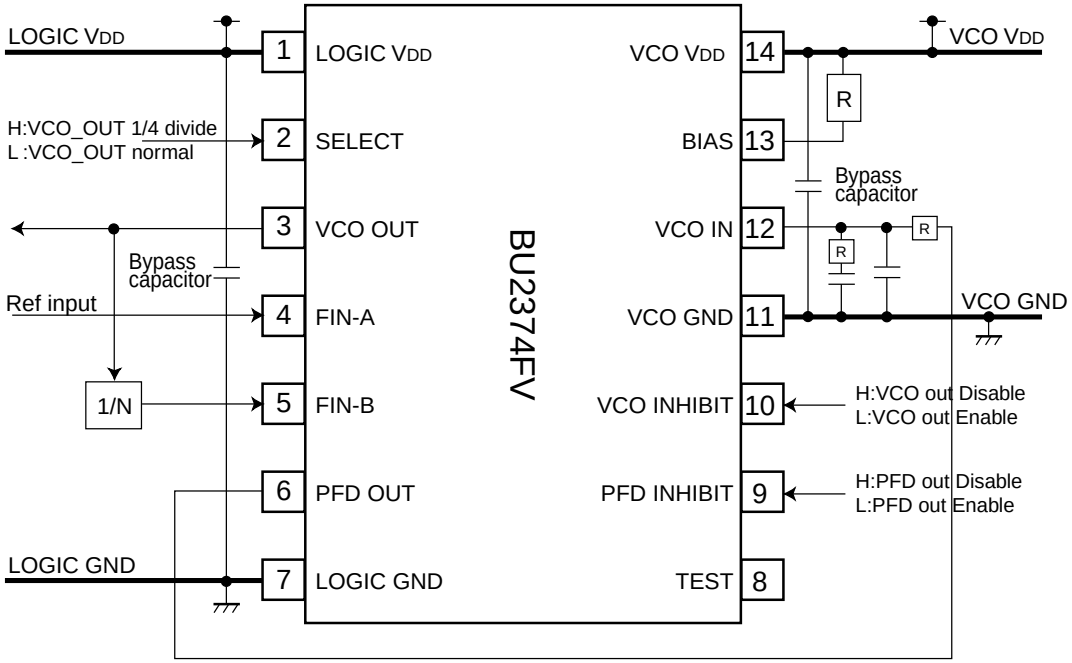
∗4



Input pin (FIN_A, FIN_B, VCO_INHIBIT, PFD_INHIBIT, SELECT)



●**Application example**



VCO_V_{DD},VCO_GND	Please take care this Power line. Because this line is most weak in digital noise. So this line must be separated from LOGIC_V_{DD}, GND. And place bypass capacitor (0.1µF) for power pin as close to BU2374FV as possible.
LOGIC_V_{DD}, LOGIC_GND	This line is noise source. So it should be separated from AV_{DD} (AGND). And place bypass capacitor (0.1µF) for power pin as close to BU2374FV as possible. And this line should be connected V_{DD} of external voc-out divide.
Bias	Please take care because the bias is weak in digital noise. And place capacitor (0.1µF) close to BU2374FV.

∗Recommend to use capacitor that is better to reduce high frequency noise.
∗Recommend to control (SELECT, PFD_INHIBIT, VCO_INHIBIT) by power line (LOGIC_V_{DD}, LOGIC_GND).

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