HIGH PERFORMANCE SYNCHRONOUS BUCK CONTROLLER WITH LDO FOR PORTABLE POWER

SC1401

November 21, 2000

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DESCRIPTION

The SC1401 is a synchronous buck regulator designed to power the latest generation microprocessors in battery operated systems. The SC1401 may be used to provide both the I/O and core voltages utilizing synchronous rectification for the core supply voltage and an LDO N-Channel MOSFET controller for the I/O supply voltage. A 1.25 volt reference allows lower output voltages required by today's portable microprocessors.

The synchronous buck regulator is capable of achieving efficiencies up to 95%. The gate drive circuitry can deliver 2.0A peak currents, allowing the use of N-channel MOSFETs for lower switching and conduction losses.

A digital soft start is provided to ensure orderly start up of the power supply without the need for external components. At light load in power save mode, the controller changes mode of operation by missing gate drive cycles, thus reducing gate drive current and improving efficiency. A logic high on PSAVE disables the power saving mode thus reducing noise. The SC1401 is fabricated in a high performance BiCMOS process. This process reduces the power dissipation in low current and shutdown operation modes and improves efficiency.

The LDO controller is a high performance positive voltage regulator designed to provide a low noise power source to the microprocessor peripherals by driving a low cost external N-Channel MOSFET.

FEATURES

- >90% Efficiency (SMPS)
- 6.0V to 30V Input range
- 1.25V to 5.5V Adjustable output (SMPS)
- PWM and LDO regulator outputs
- High output gate drive of 2 Amps (SMPS)
- Power save mode for light load operation
- 200kHz/300kHz fixed-frequency PWM operation
- 2mA Typical quiescent current
- 2µA Typical shutdown current

APPLICATIONS

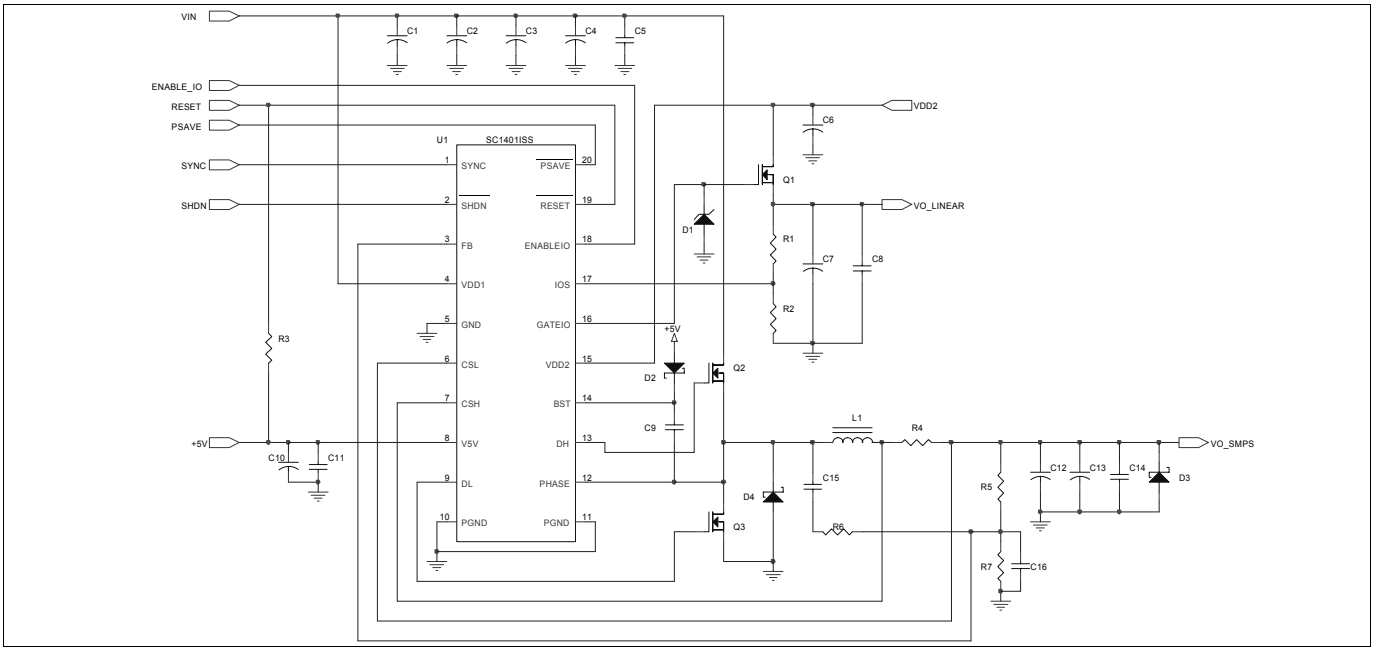
- Notebook and palmtop computers
- LCD monitors
- Internet appliances

ORDERING INFORMATION

DEVICE	PACKAGE	TEMP. (T_A)
SC1401ISS	SSOP-20	-40°C - +85°C

Notes
(1) Add suffix "TR" for tape and reel.

TYPICAL APPLICATION CIRCUIT



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PIN DESCRIPTION

Pin #	Pin Name	Pin Function
1	SYNC	Oscillator control/synchronization input. Connect to V5V for 300kHz. Connect to GND for 200kHz. For external clock synchronization in the 240kHz to 350kHz range. A high-to-low transition causes a new cycle start.
2	$\overline{\text{SHDN}}$	Logic Low shuts down the switching regulator.
3	FB	Feedback input for the SMPS. FB selects fixed 1.25V output voltage setting when tied to V_{OUT}. Connect FB to a resistor divider for adjustable output mode. $V_O(\text{SMPS}) = 1.25 \bullet \left(1 + \frac{R_8}{R_9}\right)$ Refer to page 9.
4	VDD1	Supply input from battery (6V to 30V).
5	GND	Low noise analog ground and feedback reference point.
6	CSL	Inverting input to current sense amplifier. Also serves as the feedback input in fixed output mode.
7	CSH	Non-Inverting input to current sense amplifier. Current limit level is 120mV referenced to CSL.
8	V5V	5 volt external supply used to power the gate drives, internal control and reference of the SC1401.
9	DL	Gate drive output for low side synchronous rectifier MOSFET.
10	PGND	Device power ground.
11	PGND	Device power ground.
12	PHASE	Inductor switching node connected to the source of high side MOSFET and drain of low side MOSFET.
13	DH	Gate drive output for high side N-Channel MOSFET. DH is a floating driver output driven from the floating voltage across BST to PHASE.
14	BST	Boost capacitor connection for the high side driver.
15	VDD2	Supply voltage input for the linear FET controller.
16	GATEIO	Gate drive output for the linear FET controller.
17	IOS	Sense input voltage for the adjustable voltage linear FET controller. $V_O(\text{Linear}) = 1.25 \bullet \left(1 + \frac{R_5}{R_6}\right)$ Refer to page 9.
18	ENABLEIO	Logic low shuts down the linear FET controller.
19	$\overline{\text{RESET}}$	Active-Low reset output.
20	$\overline{\text{PSAVE}}$	A logic low enables power saving mode.

Note: All logic level inputs and outputs are open collector TTL compatible.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	MAXIMUM	UNITS
VDD1 to GND	-0.3 to +36	V
PGND to GND	- 0.3 to 0.3	V
V5V, FB, CSH, CSL, IOS to GND	-0.3 to +6	V
SYNC, SHDN, PSAVE, ENABLEIO to GND	-0.3 to +6	V
BST to GND	-0.3 to +36	V
BST to PHASE	-0.3 to 6	V
VDD2 to GND	-0.3 to +36	V
GATEIO to GND	9	V
Junction operating temperature (T_J)	-40 to +125	°C
Thermal resistance junction to ambient (θ_{JA})	50	°C/W
Storage temperature	-65 to +150	°C
Lead soldering temperature	+300, 10 seconds	°C

ELECTRICAL CHARACTERISTICS

Unless specified: VDD1 = 12V, VDD2 = 12V V5V = 5V, SHDN = PSAVE = 5V, T_A = -40 °C to +85 °C . Typical values are at T_A = +25°C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SMPS CONTROLLER					
VDD1 Input Voltage Range		6.0		30.0	V
VOUT SMPS		VREF		5.5	V
Internal BandGap Voltage, VREF	Measured at the Feedback pin	1.225	1.250	1.275	V
Load Regulation	0mV < CSH - CSL < 100mV		2		%
Line Regulation	6V < VDD1 < 30V		0.03		%/V
Overcurrent-Limit Threshold	CSH - CSL	100	130	160	mV
PSAVE Mode Threshold	CSH - CSL, PSAVE = 0 V		30		mV
Soft-Start Ramp Time	From enable to 95% full current limit with respect to f_{OSC}		512		clks
Oscillator Frequency	SYNC = V5V SYNC = 0V	265 165	300 200	335 235	kHz
Maximum Duty Factor	SYNC = V5V SYNC = 0V	85 90	87 93		%

Note 1: This device is ESD sensitive. Use of standard ESD handling precautions is required.

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ELECTRICAL CHARACTERISTICS (continued)

Unless specified: VDD1 = 12V, V5V = 5V, VDD2 = 12V SHDN = PSAVE = 5V, T_A = -40 °C to +85 °C. Typical values are at T_A = +25°C.

LINE PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gate Driver Sink/Source	DL, DH, forced to 2V		2.0		A
Gate Driver On-Resistance	High or low		1.0		Ω
SYNC Input High Pulse[1]		200			ns
SYNC Input Low Pulse Width[1]		200			
SYNC Rise/Fall Time[1]				200	
SYNC Input Frequency Range		240		350	kHz
Current-Sense Input Leakage	CSL = CSH = 5.5V			20	µA
FB Input Leakage Current	FB = 1.25V			1	µA
LINEAR REGULATOR					
VDD2 Input Voltage Range		5.0		30.0	V
VOUT Linear		VREF		5.5	V
GATEIO Source current	VDD2=12V, GATEIO=0V		2.6		mA
IOS Input Leakage Current	IOS = 1.25V			1	µA
Line Regulation	ILOAD=0.5A		0.03		%/V
Load Regulation	Vin=12V, ILOAD = 0.1A to 1A		0.85		%
SUPPLY CURRENTS					
VDD1 Operating Supply			5	50	µA
Shutdown Supply Current	VDD1 = 6V to 30V, V5V = 5V, SHDN = 0V		15	25	µA
V5V Operating Supply Current	V5V = 5V, no load on DH/DL, PSAVE = 0V		1.5	4	mA
VDD2 Supply Current	VDD2 = 12V			5	mA

Note 1: Not tested.

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ELECTRICAL CHARACTERISTICS (continued)

Unless specified: VDD1 = 12V, VDD2 = 12V V5V = 5V, SHDN = PSAVE = 5V, T_A = -40 °C to +85 °C. Typical values are at T_A = +25°C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FAULT DETECTION					
Thermal Shutdown Threshold	Typical hysteresis = +10°V		150		°C
VDD1 Undervoltage Reset Threshold	Falling edge of VDD1, hysteresis = 1%	4.2	4.5	4.8	V
V5V Undervoltage Reset Threshold	Falling edge of V5V, hysteresis = 1%	3.75	4.0	4.25	V
FB Overvoltage Reset Threshold	With respect to unloaded output voltage, typ. Hysteresis = 1%		10		%
FB Undervoltage Reset Threshold	With respect to unloaded output voltage, typ. Hysteresis = 1%		-10		%
RESET Propagation Delay	FB Over/Under Voltage condition		1.5		µs
IOS Undervoltage Reset Threshold	With respect to unloaded linear output voltage		-10		%
RESET Delay Time	With respect to f_{OSC}	27,000	32,000	37,000	clks
LOGICAL INPUTS AND OUTPUTS					
Logic Input High	SHDN,ENABLEIO	1.8			V
Logic Input Low	PSAVE,SYNC			1.6	
Input Leakage Current	SHDN,ENABLEIO, PSAVE, SYNC	-1.0		1.0	µA
Logic Output Low Voltage	RESET, ISINK = 4mA			0.4	V

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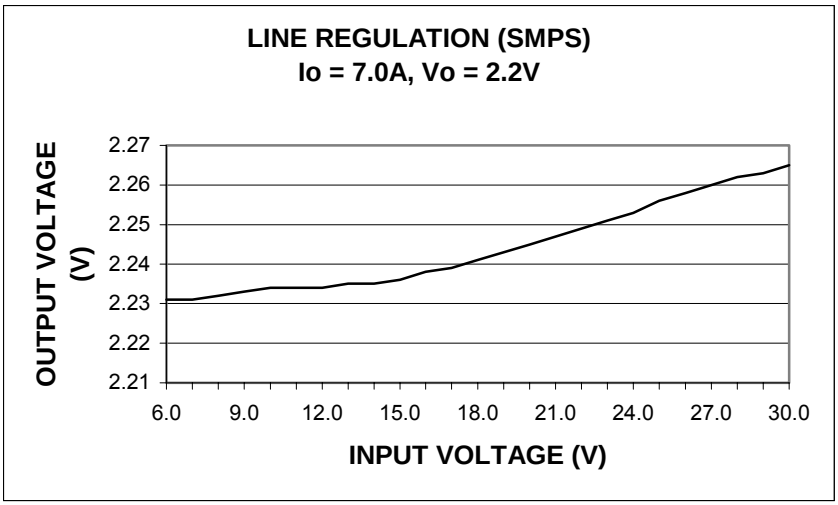

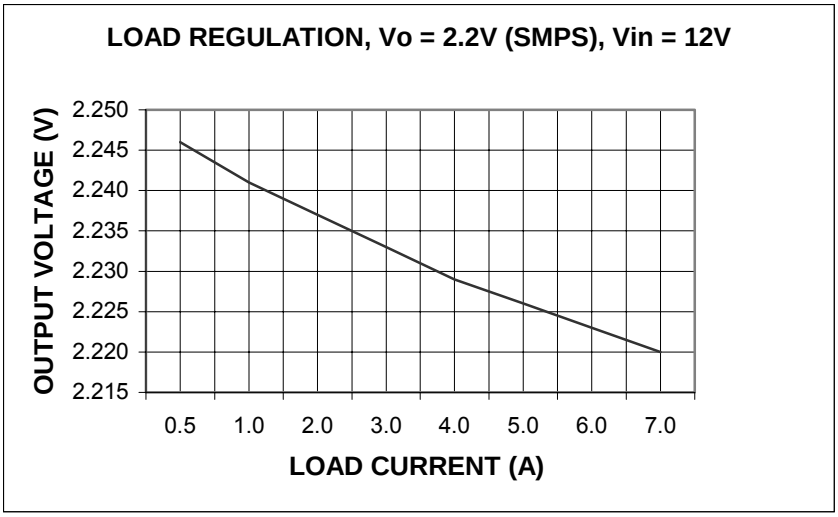

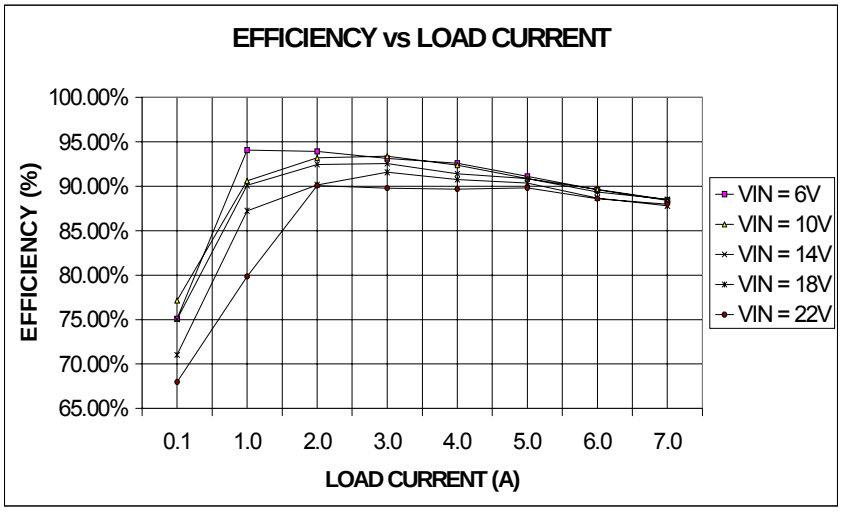

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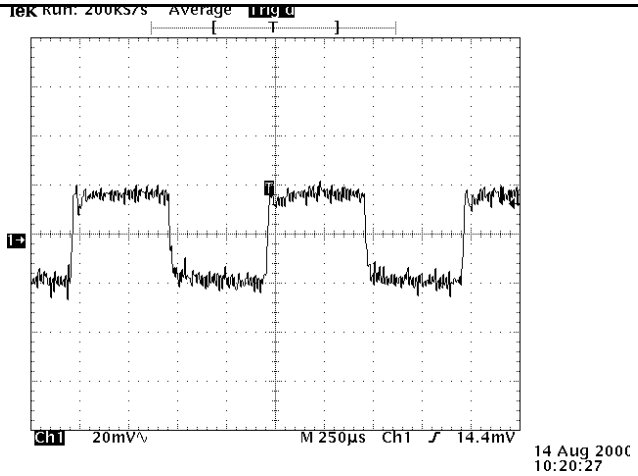
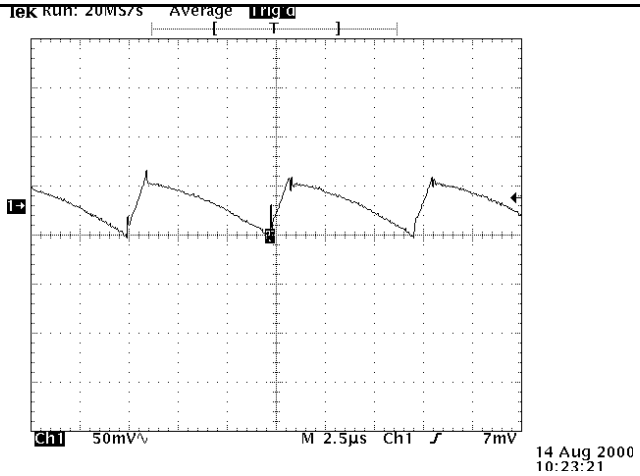
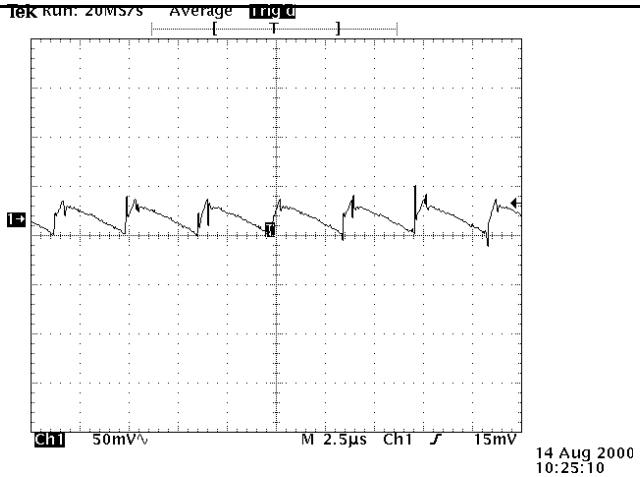


LOAD TRANSIENT: Vin = 16V, Vo = 2.0V, I = 1A to 7A



RIPPLE VOLTAGE: 200KHZ



RIPPLE VOLTAGE: 300KHZ

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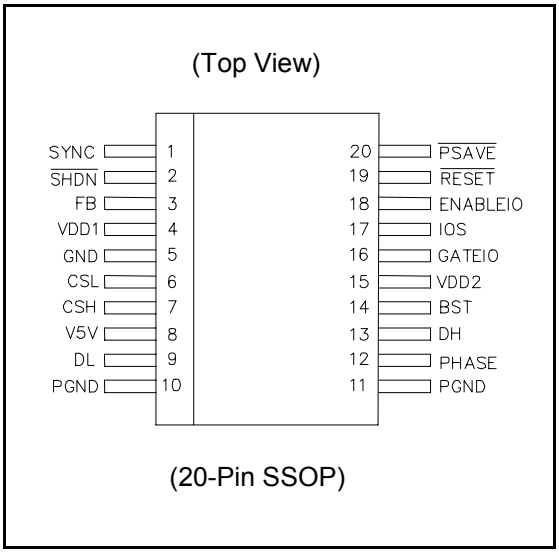
PIN CONFIGURATION



V_O (SMPS)	V_O (Linear)	R7 (current sense resistor)	R10
$V_O = 1.25 \bullet \left(1 + \frac{R_8}{R_9}\right)$	$V_O = 1.25 \bullet \left(1 + \frac{R_5}{R_6}\right)$	$R_7 = \frac{120mV}{I_{MAX}}$	5 Ω

Table 1

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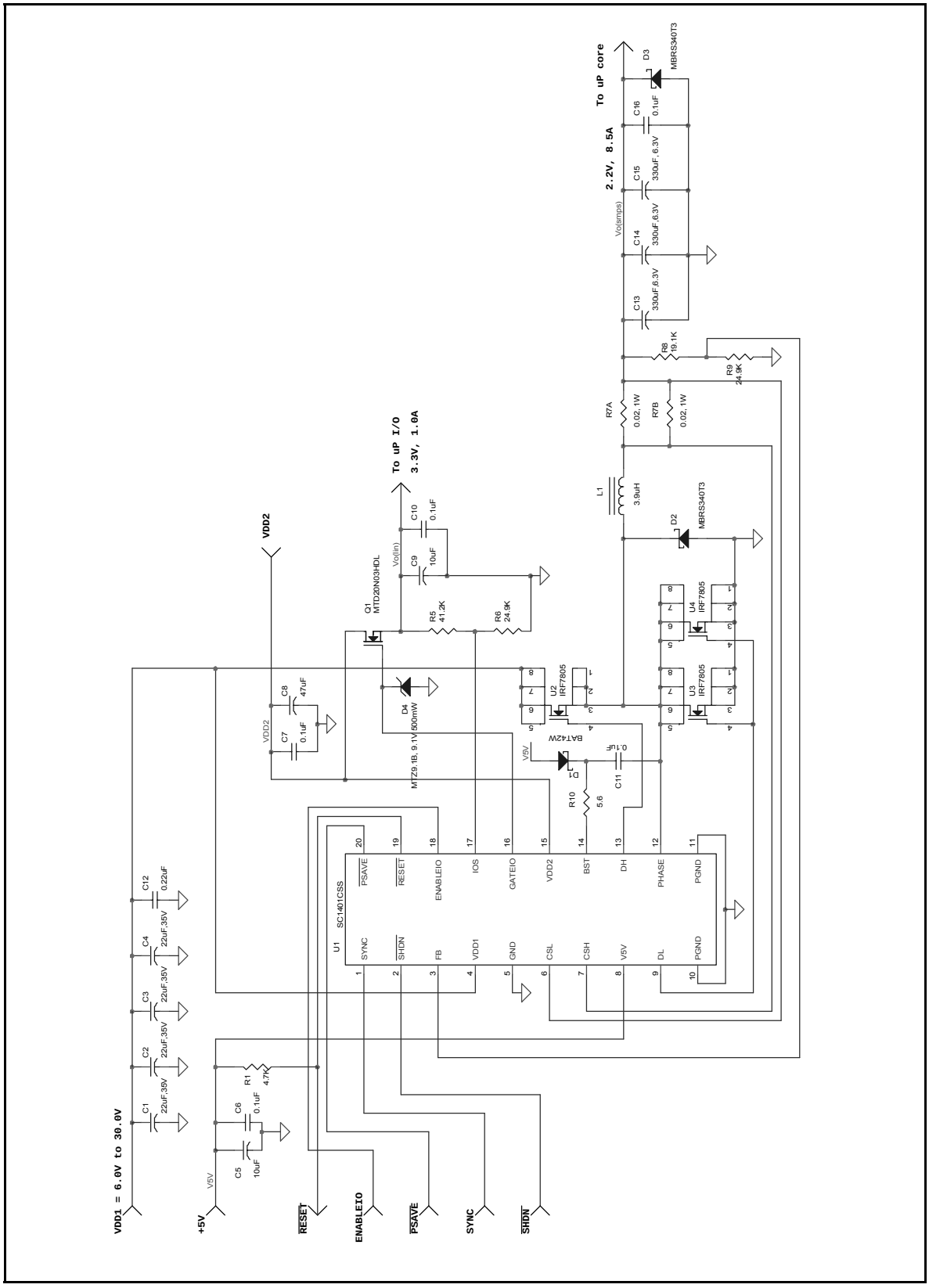
TYPICAL NOTEBOOK CPU APPLICATION CIRCUIT FOR V_{CORE} = 2.2V & $V_{I/O}$ = 3.3V



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EVALUATION BOARD SCHEMATIC

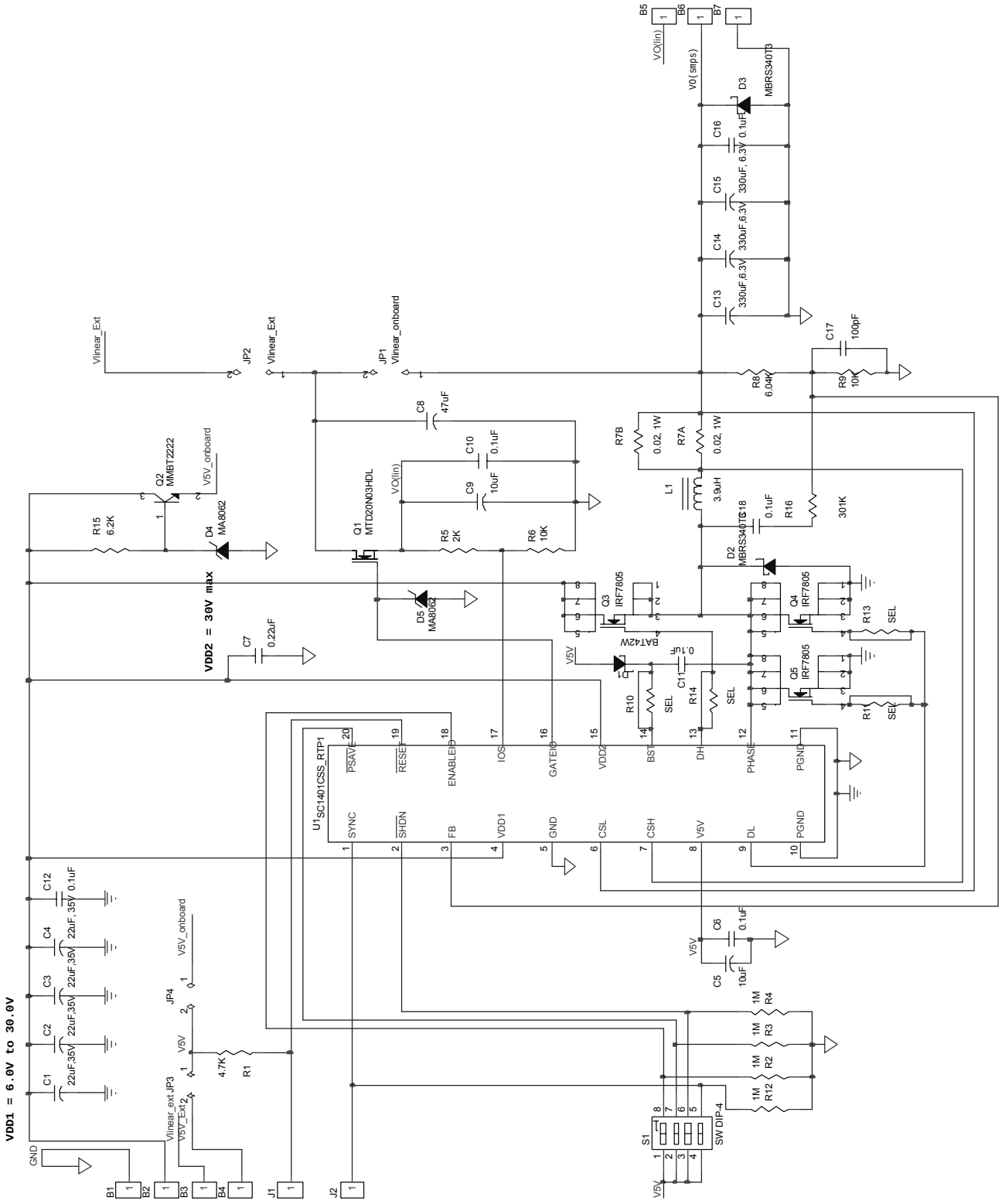


Figure 1: SC1401 Block Diagram

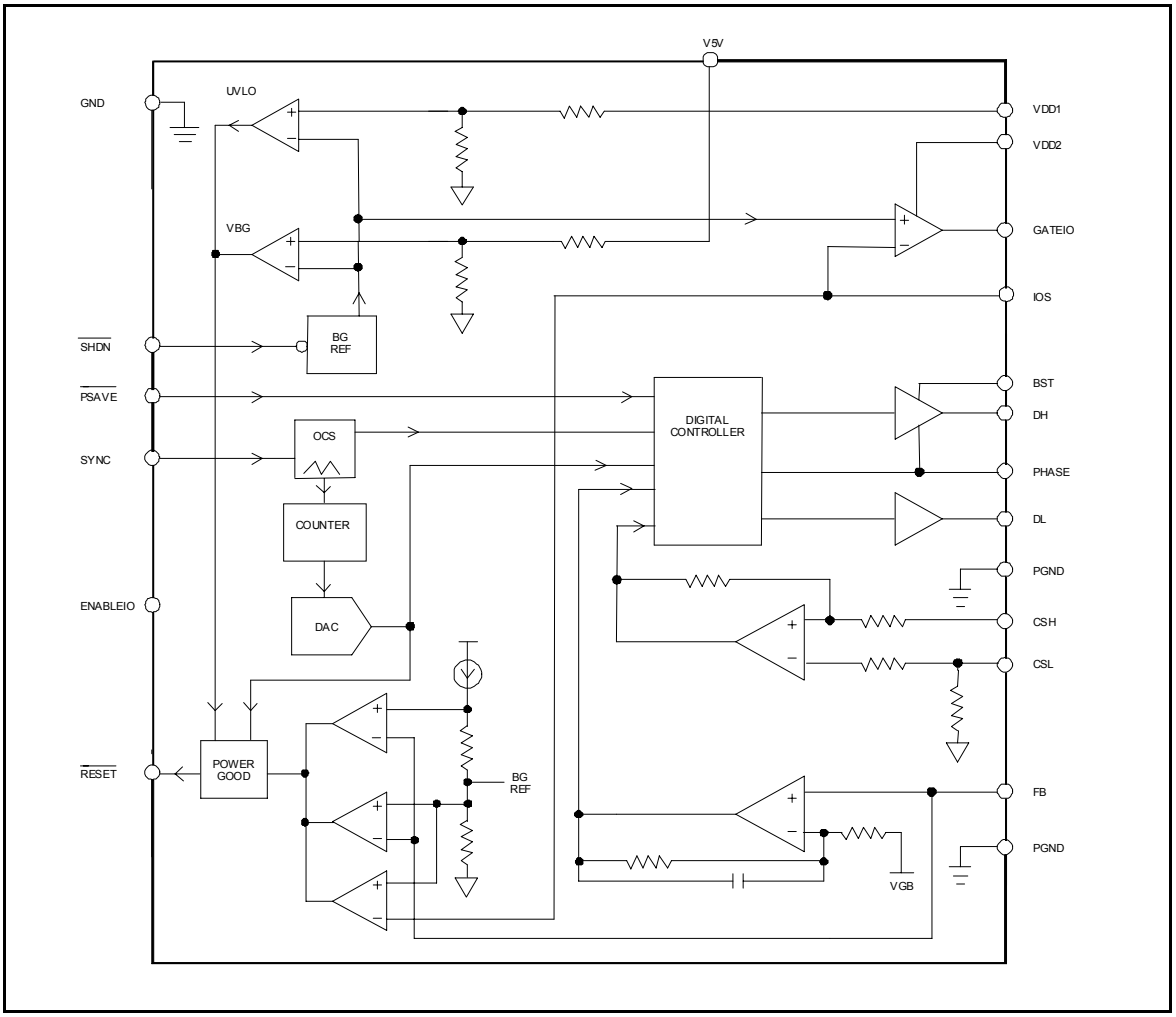
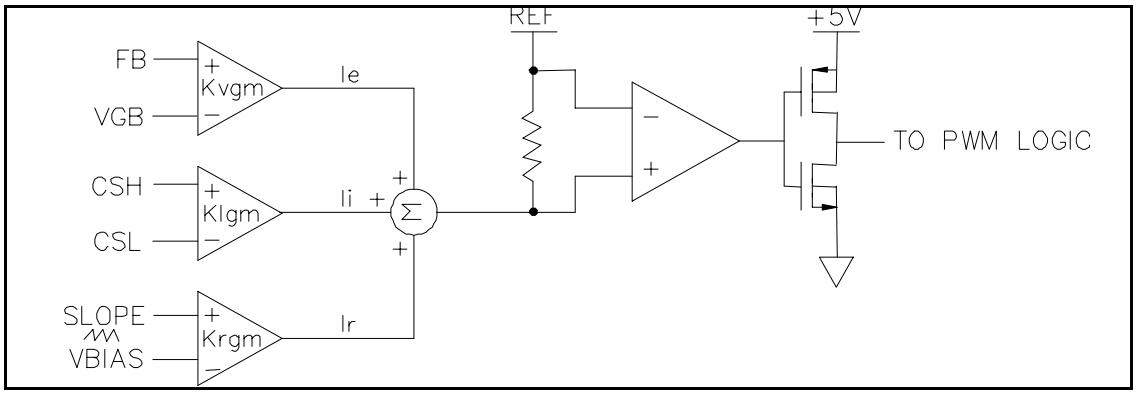


Figure 2: Main PWM Modulator Control Block



Detailed Description

The SC1401 is a high performance, high efficiency, PWM synchronous buck controller, designed to power the latest generation microprocessors in battery operated systems. Two high-current gate drive outputs are supplied to control both MOSFETs in the synchronous rectified buck converter. This power supply can be programmed to operate at either fixed (1.25V) or adjustable output voltages. The power save feature enables high efficiency over a wide range of load current. The control and fault monitoring circuitry associated with the PWM controller includes digital softstart, turn-on sequencing, frequency compensation, power save, overcurrent and over and under voltage fault protection. An LDO NMOS linear regulator is also generated by the SC1401. A block diagram of the SC1401 is shown in Figure 1.

PWM Control Block

The SC1401 employs peak-current-mode control with slope compensation to provide fast output response to load and line transients. The PWM control block consists of an analog PWM modulator followed by PWM logic control. The analog modulator combines the current output, slope compensation signal and error voltage to generate a PWM pulse train. The PWM logic uses the pulse train from the modulator and other control signals to generate the output states for the high and low side gate driver outputs. A block diagram of the PWM control block is shown in Figure 2.

An error amplifier generates the difference signal between the reference voltage and the feedback voltage to generate the control voltage for the peak current mode comparator. A nominal gain of 8 is used in the error amplifier to further increase the system loop-gain and reduce the load regulation error typically seen with low loop-gain current mode controllers. The increased gain in the voltage loop is compensated by pole-zero-pole response of the voltage error amplifier. The current feedback signal is summed with the slope compensation signal and compared to the control voltage by the PWM comparator.

When the power supply is operating in continuous conduction mode with current > 25% of its peak value, the high side MOSFET is turned on at the beginning of each switching cycle. The high-side MOSFET is turned off when the desired duty cycle is reached. Active shoot-through protection delays the turn-on of the low-side power device until the PHASE node drops below 1.25V. The low-side devices remains on until the beginning of the next switching cycle. Again, active shoot-through protection ensures that the gate to the low-side power device is low before the high-side device is turned on.

When PSAVE is enabled (low) and the output current drops below 25% of its peak level, the PWM logic will automatically enter PSAVE mode to improve efficiency. When the controller enters power save, it increases the regulation point by 0.8%, typically issuing one more high side pulse as the converter enters PSAVE. The PWM control then disables switching cycles until the FB falls below the reference. At light loads the effective switching frequency will drop dramatically and efficiency will increase because of the reduced gate charge current required to switch the power stage. Boosting the regulation point when entering PSAVE gives the output improved dynamic regulation because the output voltage is not allowed to droop below the nominal regulation point. Load current steps, that cause the converter to come out of PSAVE, will not cause as large a negative dip in the output voltage.

The PSAVE threshold is a function of the load and peak-to-peak inductor current. It can be calculated by the following equations:

$$V_{THPSAVE} = \left(I_O - \frac{\Delta I_L}{2}\right) \bullet R_S$$

$$\Delta I_L = \frac{(V_{IN} - V_O)}{L} \bullet \frac{D}{f}$$

$\triangle I_L$ = peak-to-peak inductor current

I_O = Load Current

V_{IN} = Input Voltage

V_O = Output Voltage

D = Duty Cycle

f = Frequency

L = Inductance

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Gate Drive and Control

The gate drivers on the SC1401 are designed to switch large MOSFETs at up to 350kHz. The high-side gate drivers are required to drive the gates of the high-side MOSFETs above the V5V input. The supply for these gate drivers is generated by charging a bootstrap capacitor from a supply when the low side driver is on. Monitoring circuits ensure that the bootstrap capacitor is charged when coming out of shutdown or fault conditions where the bootstrap capacitor may be depleted.

In continuous conduction mode, the low side driver outputs that control the synchronous rectifier in the power stage is on when the high side driver is off. Under light load conditions the ripple current will approach the point where it reverses polarity. This is detected by the low side driver control and the synchronous rectifier is turned off before the current reverses, preventing energy drain from the output.

Current Sense (CSH,CSL)

The output current of the power supply is sensed as the voltage drop across an external resistor between the CSH and CSL pins. Over current is detected when V(CSH,CSL) exceeds +/-130mV. An over current will turn off the high side driver on a cycle by cycle basis. CSH and CSL are also used for peak current feed back in the main PWM loop and to determine the current level for entering power save mode and the turn-off time for the synchronous rectifier.

Oscillator

The SC1401 oscillator frequency is trimmed to +/-10%. When the SYNC pin is high the oscillator runs at 300kHz; when sync is low the frequency is 200kHz. The oscillator can also be synchronized to the falling edge of a clock on the SYNC pin with a frequency between 240kHz and 350kHz. The 200kHz operation state is used for highest efficiency, and 300kHz for minimum output ripple and/or smaller inductor and output capacitor values.

Fault Protection

In addition to cycle-by-cycle current limit, the SC1401 monitors over temperature, power supply output over and under-voltage and input supply under-voltage conditions. The over temperature detect will shut the part down if the die temperature exceeds 150°C with 10°C of hysteresis.

If the SMPS output is greater than 10% of its nominal value, the SMPS is latched off and synchronous NMOS FET is turned on. To prevent the output from ringing below ground a signal level Schottky diode should be placed across the output with its anode at ground. The same results apply if VDD1 or V5V fall below their respective under-voltage thresholds.

If the SMPS or LDO outputs fall 10% below its nominal, the RESET output is pulled low.

Shutdown Mode

Holding the SHDN pin low disables the SC1401, reducing the total supply input current to <10uA. A shutdown condition tri-states the SMPS and pulls the RESET output low. Holding the ENABLEIO pin low disables the LDO.

Output Voltage Selection

If FB is connected to CSL, the SMPS will regulate to the internal bandgap voltage, 1.25V. If external resistors are used, the output is regulated based on a resistor divider and 1.25V at the FB pin.

LDO Regulation Operation

The n-channel LDO regulator is capable of supplying 1A over a 1.25V to 5.5V output range. The input voltage to the LDO is the VDD2 supply with a maximum input voltage of 30V. To set the output voltage, an external resistor divider is used based on 1.25V at the IOS pin.

Power-up and Soft-Start

The SMPS contains its own counter and DAC to gradually increase the current limit at startup to prevent input surge currents. The current limit is increased from 0, 25%, 50%, 75%, to 100% linearly over the course of 512 switching cycles.

A RESET output is also generated at startup. The RESET pin is held low for 32K switching cycles. Another timer is used to enable the undervoltage protection. The undervoltage protection circuitry is enabled after 5000 switching cycles at which time the SMPS should be in regulation.

Evaluation Board

The evaluation board schematic shown on page 10 is configured to output 2.0V at 7.0A on the main switcher and 1.5V at 1A on the linear regulator. In addition, the main switcher has a compensation circuit consisting of C18, R16 and C17. This circuit aids in the stability of the supply for variability in output filter components

and output voltage and current ranges. This compensation circuit is necessary for proper operation of the SC1401. This will eliminate any uncertainties in stability with respect to various output configurations that may be implemented using the part.

Having JP1 in place will enable the linear regulator to derive power from the main switching supply. The switcher must have a higher output voltage than the linear to allow this option to work properly. Further information of the evaluation board and it operation is described in the SC1401 Evaluation Board Manual.

LDO

The evaluation board schematic shows that the LDO regulator is set up to derive its power from the output of the SMPS. The GATEIO, pin 16 is the gate drive for an N-Channel MOSFET, Q1. This output has a breakdown voltage of 12V so it is imperative the gate does not exceed 12V and Q5, a nine volt zener diode is added to prevent this from happening. In addition, IOS, pin 17 is the input from the resistive divider formed by R5 and R6. The LDO MOSFET should be chosen to carry the load current and dissipate the power required by the conditions of the load current and voltage drop across the MOSFET. Capacitors C9 and C10 were added for filtering purposes.

Gate Drive Power

JP4 enables the gate drive power to operate off of the onboard zener follower which supplies 5 volts, formed by components Q2, R15 and D4. This takes the input voltage and produces 5V for the bootstrap diode D1 that supplies the gate drive power for the upper MOSFET of the Q3 SMPS. Alternatively, you could also bring in an external voltage for the gate drive voltage by moving the jumper from JP4 to JP3. Consult the SC1401 Evaluation Board Manual for further details of the evaluation board operation.

APPLICATIONS INFORMATION

Introduction

The SC1401 is a versatile switching regulator providing an adjustable output from 1.25V to 5.5V. In addition, there is one on-chip adjustable linear regulator capable of supplying 1 amp of output current. The SC1401 is designed for notebook applications but has applications anywhere high efficiency, small size and low cost are required.

The Semtech SC1401 EVAL board consists of a 2.0V, 7A switcher and a 1.5V, 1A linear regulator.

Design Guidelines

The schematic for the EVAL board is shown on page 10. The EVAL board is configured as follows:

Switching Regulator 1	Vout1 = 2.0V, 7A
Linear Regulator 1	Vout2 = 1.5V, 1A

Designing the Output Filter

Before calculating the output filter inductance and output capacitor, an acceptable amount of output ripple current is to be determined. The ESR of the output capacitor multiplied by the ripple current sets the maximum allowable ripple voltage. So once the ripple voltage specification is selected, the capacitor ESR is chosen usually based on capacitor cost and size constraints. This then sets the maximum output ripple current through the capacitor and inductor.

For the EVAL board 2.0V switcher, we selected a maximum ripple voltage of 50mV. Choosing three 330uF, 6.3V tantalum capacitors C13,C14 and C15 each having an ESR of 100 milliohms, their combined ESR equaling 33 milliohms, sets the maximum ripple current as follows:

$$\Delta I_O = \frac{\Delta V_O}{ESR} \qquad \Delta I_O = \frac{0.05}{0.033} = 1.5Amp$$

Be sure that the three output capacitors can handle this ripple current. Ripple current specifications are found in the capacitor data sheet for high quality capacitors intended for use in switching power supplies.

The inductance can now be found:

$$L1 = \frac{(V_{INMAX} - V_O) \bullet D \bullet t}{\Delta I_O}$$

The inductance and duty cycle equation excludes

any resistive drops due to winding resistance and MOSFET on resistance.

Where: $D = \frac{V_O}{V_{IN}}$, $t = \frac{1}{f}$, and $f = 300kHz$

$$L1 = \frac{(28 - 2.0) \bullet \frac{2.0}{28} \bullet 3.33 \bullet 10^{-6}}{1.5}$$

L1 = 4µH

From this calculation we choose L1 to be 3.9uH.

For a lower operating frequency, f = 200kHz, L1 calculates to be 6uH.

Choosing Inductor & FET Current Rating

The current carrying capability of the inductor and MOSFETs should be sized to handle the maximum current of the supply set by the current sense resistor. For the SC1401 EVAL board Rsense equals the parallel combination of R7A & R7B. Here we use the minimum current threshold value:

$$R_{SENSE} = \frac{100mV}{I_{PEAK}}$$

Where I_{PEAK} equals:

$$I_{PEAK} = I_O + \frac{\Delta I_O}{2}$$

I_{PEAK} = 7 + 0.75

I_{PEAK} = 7.75 Amps

Here we chose a sense resistor of 13.5 milliohms. Now we can determine FET and inductor current carrying capability by using the maximum current limit threshold:

$$I_{PEAK} = \frac{0.14}{0.0135} = 10.4 Amps$$

From this value choose an inductor with Isat > 10.4 Amps, and for the FET choose a continuous conduction current rating Ic > 10.4 Amps.

Input Capacitor Selection

Input capacitor is selected based upon the input ripple current demands of the converter. First determine the input ripple current expected and then choose a capacitor to meet that demand.

The input RMS ripple current can be calculated as follows:

$$I_{RMS} = \frac{I_O}{V_{IN}} \sqrt{V_O \bullet (V_{IN} - V_O)}$$

$$I_{RMS} = \frac{7}{6} \bullet \sqrt{2 \bullet (6 - 2)}$$

I_{RMS} = 3.3 Amps

The worse case input RMS ripple current occurs at 50% duty cycle (D = 0.5 or Vin = 2 Vout) and therefore under this condition the IRMS ripple current can be approximated by:

$$I_{RMS} = \frac{I_O}{2}$$

However, this condition will not occur because the duty cycle is set by Vo/Vin, 2/6 = 0.33. If the output voltage is changed where D approaches 50% the input capacitor ripple current may need to be recalculated and capacitors added.

Therefore, for a maximum load current of 7 amps, the input capacitors should be able to safely handle 3.3 amps of ripple current.

For the EVAL board, we chose four 22uF, 35V Tantantalum capacitors. Each capacitor has a ripple current capability of 0.908 amps at 100kHz, 25°C. Four of these capacitors in parallel will meet the requirements.

MOSFET Switches

After selecting the voltage and current requirements of each MOSFET device for the upper and lower switches, the next step is to determine their power handling capability. For the EVAL board the IRF7805 meet the voltage and current requirements. However, the lower FET is a combination of two IRF7805 devices in parallel for improved efficiency

and to handle any possible short circuit condition. These are 30V, 9A FET's. Based on 85°C ambient temperature, 150°C junction temperature and thermal resistance, their power handling is calculated as follows:

Power Limit for Upper & Lower FET:

$T_J = 150^oC$ $T_A = 85^oC$ $\ominus_{JA} = 50^oC/W$

$$P_T = \frac{T_J - T_A}{\theta_{JA}} = \frac{150 - 85}{50} = 1.3W$$

Each FET must not exceed 1.3W of power dissipation.
The conduction losses for the upper & lower FET can be determined. For the calculations below, a nominal input voltage of 12V, for Vout = 2.0V, Iout = 7A and f = 300kHz. The Rdson value for the upper & lower FET is 11milliohms. We will calculate the conduction losses and switching losses for each FET. From the calculations below we are well within the 1.3 watt dissipation limit as calculated above.

Conduction Losses Upper FET:

$$P_{CU} = R_{DS} \bullet D \bullet I^2$$

$$P_{CU} = 0.011 \bullet \frac{2}{12} \bullet 7^2$$

$P_{CU} = 0.090W$

Conduction Losses Lower FET:

$$P_{CU} = R_{DS} \bullet (1-D) \bullet I^2$$

$$P_{CL} = 0.0055 \bullet \left(1-\frac{2}{12}\right) \bullet 7^2$$

$P_{CL} = 0.225W$

Switching Losses Upper FET:

Note: switching losses exist on the upper FET only because the clamp diode across the lower FET will turn on prior to the lower FET turning on.

$$P_{SU} = \frac{C_{RSS} \bullet V_{IN}{}^2 \bullet F \bullet I_O}{I_G} = \frac{215 \bullet 10^{-12} \bullet 12^2 \bullet 300000}{1} \bullet 7$$

$P_{SU} = 0.065W$

Crss is the reverse transfer capacitance of the FET; in this case it equals 215pF for the IRF7805.

Where Ig is the gate driver current. This is equal to 2A for the SC1401.

So the total FET losses equate to:

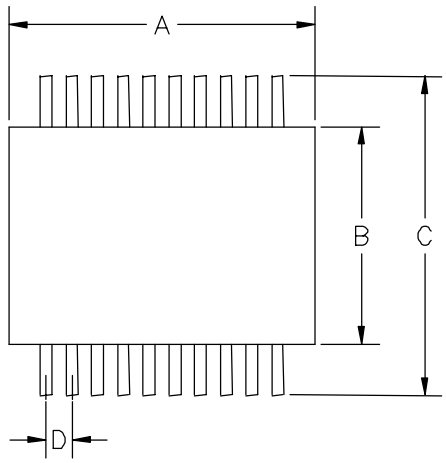
$P_{FETS} = 0.09 + 0.225 + 0.065 = 0.38W.$

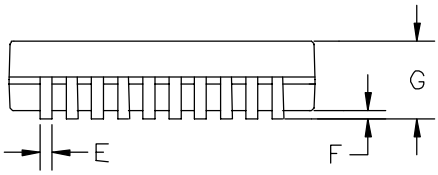
Note that as Vin increases, the power dissipation from switching losses will also increase. This is especially important if the input to the supply is from an AC adapter. Therefore, it is necessary to check the calculations with your maximum input voltage specification. In addition, the distribution of power in the upper and lower FET will change as input voltage increases.

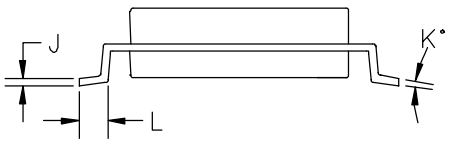
Other losses to consider are gate charge losses, inductor switching and copper losses, and losses in the input and output capacitors. All these items will decrease efficiency and need to be carefully analyzed to obtain the highest efficiency possible, especially if running off battery power.

November 21, 2000

OUTLINE DRAWING - SSOP-20







DIMENSIONS [1]					
DIM^N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.2716	.2953	6.90	7.50	[2]
B	.205	.209	5.20	5.38	[2]
C	.291	.323	7.40	8.20	–
D	.026 BSC		.65 BSC		–
E	.009	.015	.22	.38	–
F	.0020	.0080	.05	.21	–
G	.068	.078	1.73	2.00	–
J	.0040	.0100	.09	.20	–
K	0°	8°	0°	8°	–
L	.022	.037	.55	.95	–

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Jedec MO-150AE