CMOS 4-BIT MICROCONTROLLER

TMP47C337AN

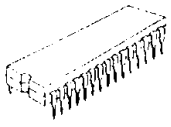
The 47C337A is based on the TLCS-47 CMOS series. The 47C337A has On-screen display (OSD) circuit to display bar which indicate channel or volume on TV screen, A/D converter input, D/A converter output which is suitable for application to the digital tuning system such as TV.

PART No.	ROM	RAM	PACKAGE	PIGGY BACK (adaptor socket)
TMP47C337AN	3072 x 8-bit	192 x 4-bit	SDIP30	TMP47C937AE (BM1103)

FEATURES

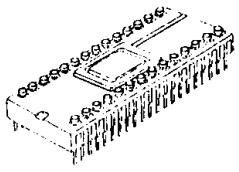
- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 1.9μs (at 4.2MHz)
- ◆89 basic instructions.
  Table look-up instructions
- ◆Subroutine nesting : 15 levels max.
- ◆5 interrupt sources (External : 2, Internal : 3)
  All sources have independent latches, and multiple interrupt control is available.
- ◆I/O port (24 pins)
  - Input 2 ports 5 pins
  - I/O 5 ports 19 pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counter
  Timer, event counter, and pulse width measurement mode
- ◆On-screen display circuit (bar display)
  - Variable display position : horizontal / vertical 256 steps each
  - display bar length : vertical 256 steps
  - 2 display bar width
  - 3 colors
- ◆3-bit A/D converter input.
  Auto frequency control signal (S-shaped curve) detection
- ◆Pulse width modulation outputs
  - 14-bit resolution 1 channel
  - 6-bit resolution 1 channel
- ◆High current outputs
  LED direct drive capability (typ. 10mA x 4bit)
- ◆Hold function
  Battery / Capacitor back-up
- ◆Real Time Emulator : BM47C337A

SDIP30



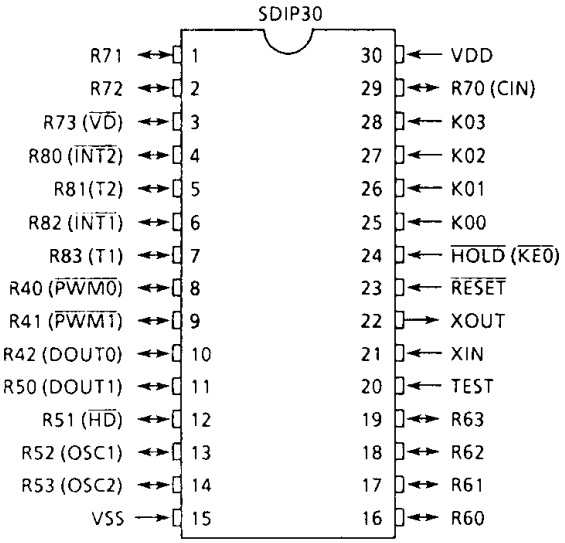
TMP47C337AN

SDIC42

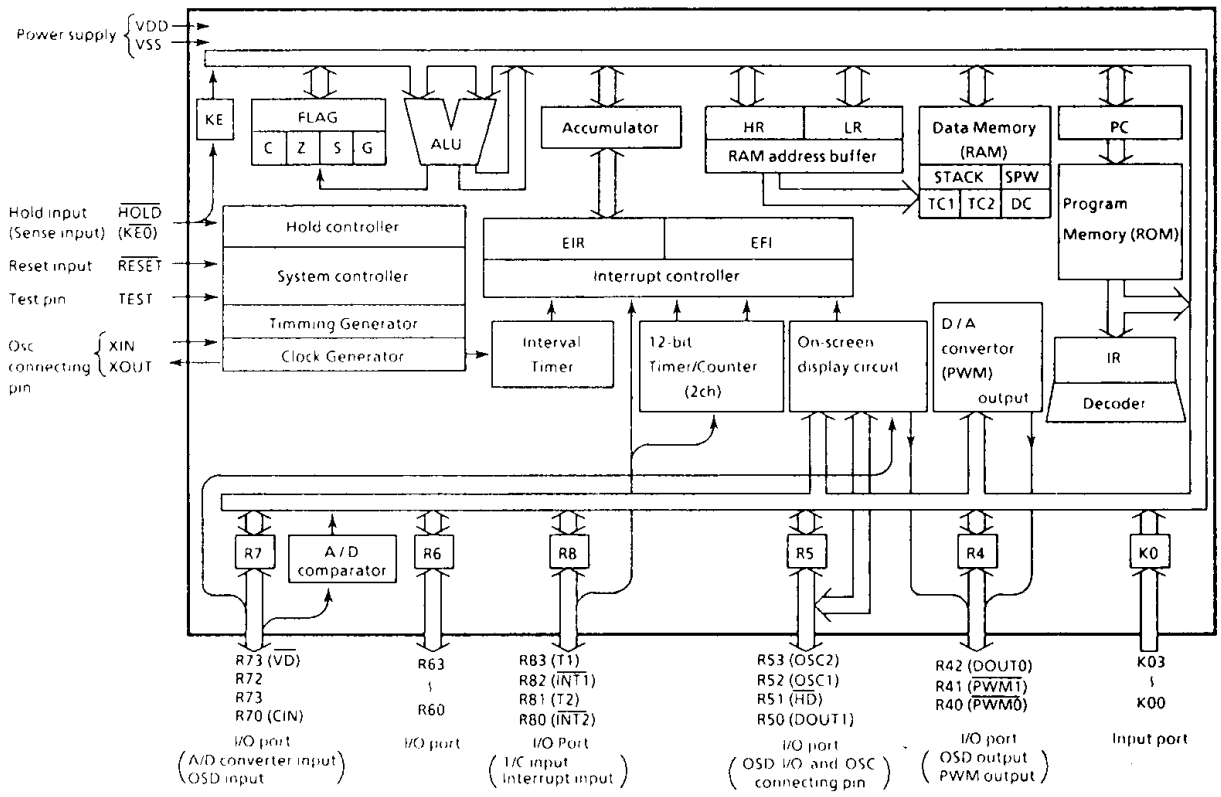


TMP47C937AE

PIN ASSIGNMENT (TOP VIEW)



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03-K00	Input	4-bit input port	
R42 (DOUT0)	I/O (Output)	3-bit I/O port with latch. When used as input port, D/A converter output pin and OSD output pin, the latch must be set to "1".	OSD output
R41 ($\overline{PWM1}$)			6-bit D/A converter output
R40 ($\overline{PWM0}$)			14-bit D/A converter output
R53 (OSC2)	I/O (Output)	4-bit I/O port with latch. When used as input port, resonator connectting pin, horizontal sync signal input pin and OSD output pin, the latch must be set to "1".	Resonator connecting pin for OSD
R52 (OSC1)	I/O (Input)		
R51 ($\overline{HD}$)	I/O (Input)		Horizontal sync signal input
R50 (DOUT1)	I/O (Output)		OSD output
R63-R60	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R73 ($\overline{VD}$)	I/O (Input)	4-bit I/O port with latch. when used as input port, A/D converter input pin and vertical sync signal input pin, the latch must be set to "1".	Vertical sync signal input
R72	I/O		
R71			
R70 (CIN)	I/O (Input)		3-bit A/D converter input
R83 (T1)	I/O (Input)	4-bit I/O port with latch. when used as input port, external interrupt and timer / counter input pin, the latch must be set to "1".	Timer/Counter 1 input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 input
R80 ($\overline{INT2}$)			External interrupt 2 input
XIN, XOUT	Input, Output	Resonator connecting pin. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	Input	Reset signal input.	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	Hold request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	

OPERATIONAL DESCRIPTION

Concerning the 47C337A, the configuration and functions of hardwares are described.
As the description is provided with priority on those parts differing from the 47C200A, the technical data sheets for the 47C200A shall also be referred to.

Note : The 47C337A has no serial port, differing from the 47C200A.

1. SYSTEM CONFIGURATION

(1) Internal CPU function

The 47C337A is similar to the 47C200A except ROM and RAM capacity.

(2) Peripheral Hardware function

① I/O Port
② Interval Timer
③ Timer / counter
④ A / D converter input
⑤ D / A converter (Pulse width Modulation)output
⑥ On-screen display (OSD) circuit

This section describes the function ①, the function ④ to ⑥ and ROM, RAM capacity which are changed from the 47C200A.

2. INTERNAL CPU FUNCTION

2.1 PROGRAM MEMORY (ROM)

The 47C337A has 3072 × 8bits (address 000-BFF$_H$) of program memory (mask ROM).
The table look-up instructions ([LDH A, @DC +], [LDL A @DC]) store into the accumulator fixed data of program memory (address 000-BFF$_H$).
The instruction [OUTB @HL] cannot be used.

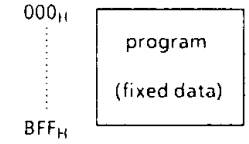


Figure 2-1. Program Memory

2.2 DATA MEMORY (RAM)

Data memory contained 192 × 4bit (address 00-7F$_H$, C0-FF$_H$) capacity.
There is no physical RAM in address 80-BF$_H$.
Therefore, when address 80-BF$_H$ are accessed on a program, RAM equivalent to address C0-FF$_H$ is accessed.
The relationship between RAM capacity and address is shown in Figure2-2.

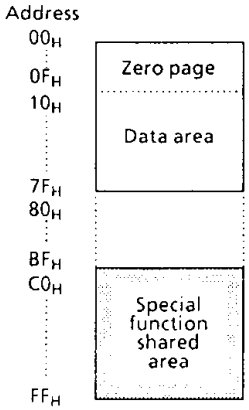


Figure 2-2. Data Memory Capacity and Address Assignment

3. PERIPHERAL HARDWARE FUNCTION

3.1 I/O Port

The 47C337A has 7 I/O Ports (24 Pins) each as follows.

① K0 port ; 4-bit input
② R4 port ; 3-bit input/output (R42 pin is shared by OSD output. R41, R42 pins is shared by D/A converter output)
③ R5 port ; 4-bit input/output (R53, R52 pins is shared by Resonator connecting pin for OSD R51, R50 pins is shared by I/O pin for OSD.)
④ R6 port ; 4-bit input/output
⑤ R7 port ; 4-bit input/output (R73 pin is shared by input pin for OSD, R70 pins is shared by A/D converter input.)
⑥ R8 port ; 4-bit input/output (shared by external interrupt input and timer/counter input)
⑦ KE port ; 1-bit sense input (shared by hold request/release signal input)

This section describes ports of ②, ③, ⑤ which are changed from the 47C200A.
The 47C337A has no P1, P2 and R9, therefore 5-bit to 8-bit data conversion instruction[OUTB @HL]can not use.

Port address (**)	Port		Input/output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A,%p OUT @HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p,b TESTP %p,b	SET @L CLR @L TEST @L
00_H	K0 input port.	—	○	–	–	–	–	○	–
01	—	—	–	–	–	–	–	–	–
02	—	—	–	–	–	–	–	–	–
03	—	—	–	–	–	–	–	–	–
04	R4 input port	R4 output port (OSD,$\overline{PWM}$ output)	○	○	○	–	○	○	○
05	R5 input port (OSD input)	R5 output port (OSD output)	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port (OSD, CIN input)	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	—	—	–	–	–	–	–	–	–
0A	—	OSD data transfer buffer	–	○	○	–	–	–	–
0B	—	OSD data transfer buffer	–	○	○	–	–	–	–
0C	—	OSD control	–	○	○	–	–	–	–
0D	—	OSD data register selector	–	○	○	–	–	–	–
0E	Status input	—	○	–	–	–	–	○	–
0F	—	—	–	–	–	–	–	–	–
10_H	Undefined	HOLD control	–	○	–	–	–	–	–
11	Undefined	—	–	–	–	–	–	–	–
12	Undefined	A/D converter input control	–	○	–	–	–	–	–
13	Undefined	—	–	–	–	–	–	–	–
14	Undefined	—	–	–	–	–	–	–	–
15	Undefined	—	–	–	–	–	–	–	–
16	Undefined	—	–	–	–	–	–	–	–
17	Undefined	PWM buffer selector	–	○	–	–	–	–	–
18	Undefined	PWM data transfer buffer	–	○	–	–	–	–	–
19	Undefined	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	—	–	–	–	–	–	–	–
1B	Undefined	—	–	–	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	—	–	–	–	–	–	–	–
1F	Undefined	—	–	–	–	–	–	–	–

Note 1. Port addresses with "—" mark are reserved addresses and cannot be used at user program.

Table 3-1. Port Address Assignment and Input/Output Instructions

(1) R4 (R42-R40), (R53-R50) port

R4 is 3-bit, R5 is 4-bit I / O port with latch. When used as input port, following control input / output, the latch must be set to "1". The latch is initialized to "1" during reset.

R42 and R50 terminal is shared with the OSD output. When used as OSD output, enable OSD and select DOUT0 / DOUT1 by command register (OP0C).

R53, R52 (0SC2, 0SC1) terminal is shared with resonator connecting pin. when used as resonator connecting pin, enable OSD.

R51 terminal is shared with $\overline{HD}$ (horizontal sync signal) input. $\overline{HD}$ is read when an input instruction is executed.

R41, R40 terminal is shared with PWM (pulse width modulation) output.

"1" is read when an in put instruction is executed for R52/R53 during OSD is enable and for R42/R50 during DOUT0/DOUT1 is selected.

Note that R43 pin does not exist actually but "1" read when an input instruction is executed.

R4 Port (Port address OP04 / IP04)

3	2	1	0
	R42 (DOUT0)	R71 ($\overline{PWM1}$)	R70 ($\overline{PWM0}$)

R5 Port (Port address OP05 / IP05)

3	2	1	0
R53 (OSC2)	R52 (OSC1)	R51 ($\overline{HD}$)	R50 (DOUT1)

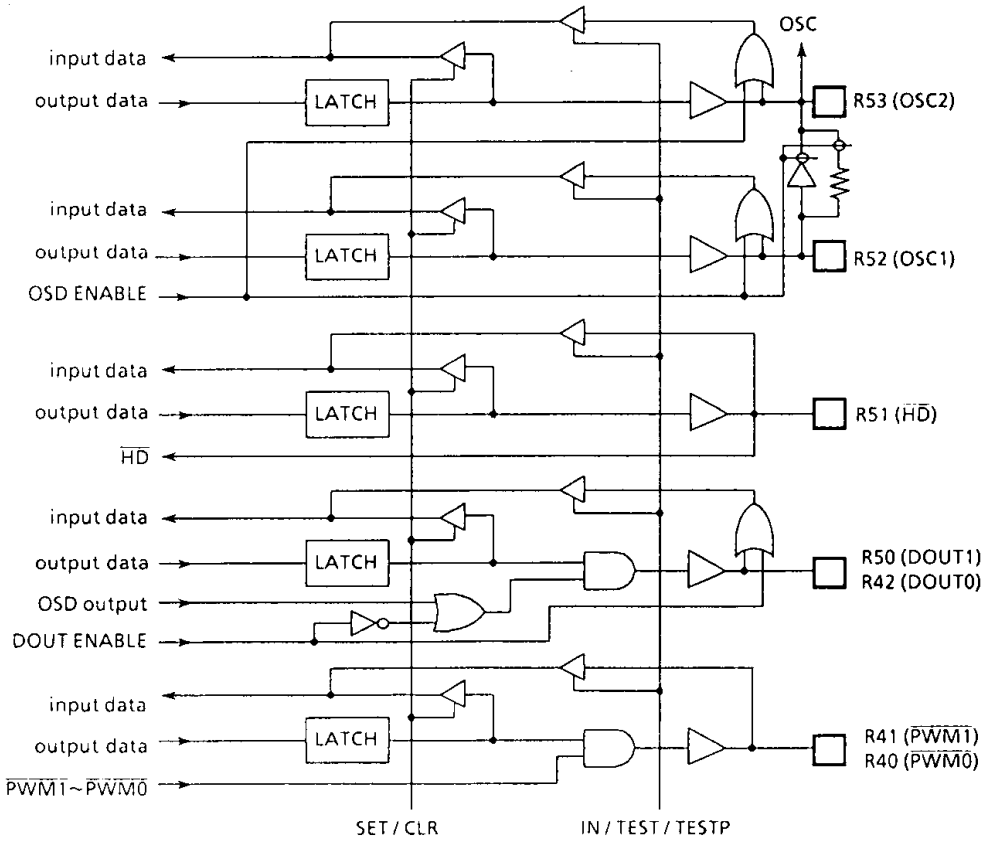


Figure 3-1. R4, R5 port

(2) R7 (R73-R70) Port

4-bit I/O port with latch. When used as input port, the latch must be set to "1".
The latch is initialized to "1" during reset.
R73 terminal is shared with $\overline{VD}$ (vertical sync signal) input. $\overline{VD}$ is read when an input instruction is executed during OSD enabled. When used as $\overline{VD}$ input, the latch must be set to "1".
R70 terminal is shared with the A/D converter input for to detect the AFC (Auto Frequency Control) signal. When used as A/D converter input, the latch must be set to "1", and bit 3 of command register must be set enable. IN input is comparator for input read from bit 0 of IP07 and uses the programable 3-bit D/A converter output as the reference voltage.

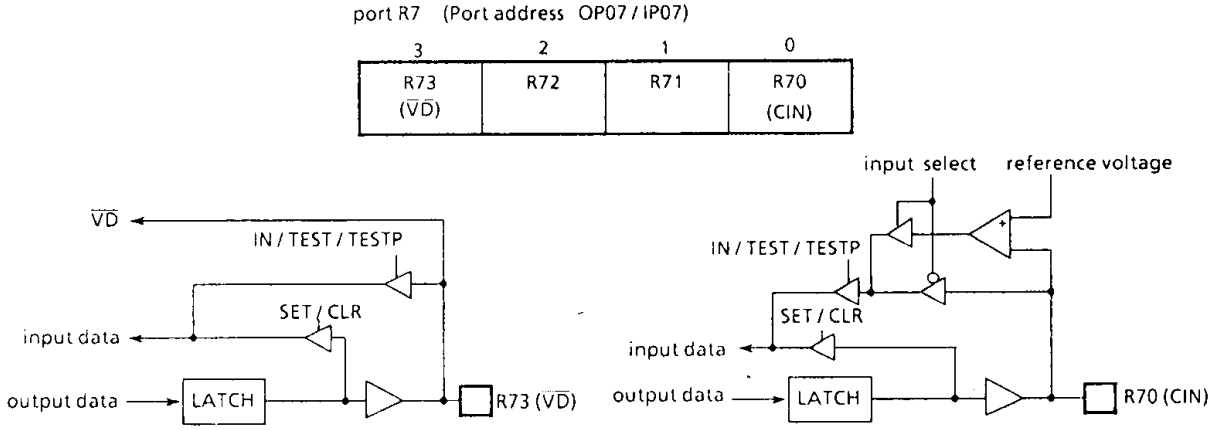


Figure 3-2. PORT R7

3.2 3-bit A/D converter (comparator) input

Comparator input consists of a comparator and a 3-bit D/A converter. AFC input voltage can be detected in 8 steps by sensing bit 0 of IP07 while changing the reference voltage (D/A converter output voltage) with the command register (OP12).
R70 pin is also used for comparator input. The comparator is initialized to disable. The latch should be set to "1" when pin R70 is used for comparator input.

Figure 3-3 shows the configuration of comparator circuit.

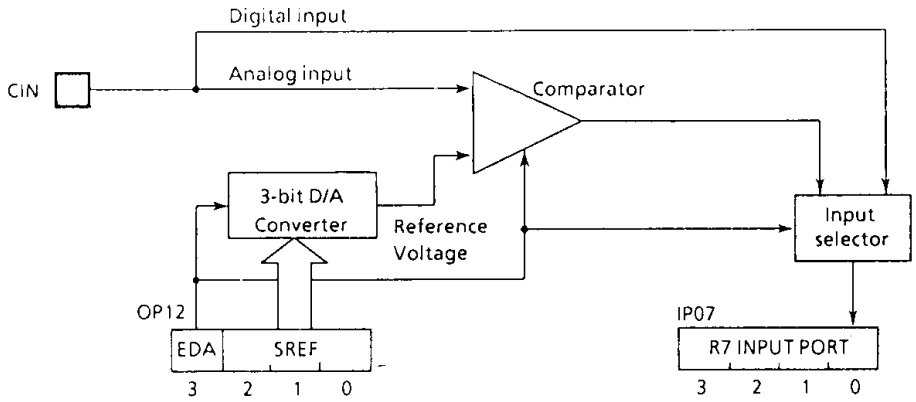


Figure 3-3. Comparator input circuit

The reference voltage of the comparator is set using the lower 3 bits of the command register (OP12) Table 3-2 shows the reference voltage at V_{DD} = 5 V.

Comparator input control command register (port address OP12)

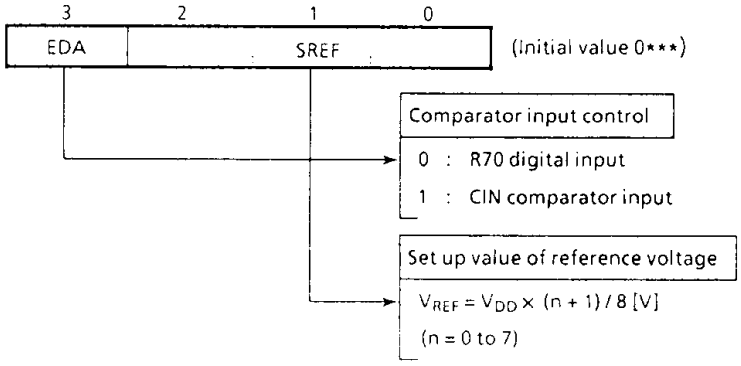


Figure 3-4. Command register

SREF 2 1 0	Reference voltage [V]
0 0 0	0.62
0 0 1	1.25
0 1 0	1.87
0 1 1	2.50
1 0 0	3.12
1 0 1	3.75
1 1 0	4.37
1 1 1	5.00

Table 3-2. Reference Voltage

3.3 D/A converter (Pulse Width Modulation) output

The 47C237A has two D/A converter ($\overline{PWM}$) output channels. PWM output can easily be obtained by connecting an external low pass filter.

$\overline{PWM}$ output is from the R40 ($\overline{PWM0}$) , R41 ($\overline{PWM1}$) pins. R40 ($\overline{PWM0}$) , R41 ($\overline{PWM1}$) pins are used for $\overline{PWM}$ output, the corresponding R40, R41 output latch is set to "1." The R40, R41 output latch is initialized to "1".

$\overline{PWM}$ output is controlled by the buffer selector (OP17) and the data transfer buffer (OP18). $\overline{PWM}$ data written to the data transfer buffer can be sent to the $\overline{PWM}$ data latch by writing "C_H" to the buffer selector to switch to $\overline{PWM}$ output. $\overline{PWM}$ data transferred to the $\overline{PWM}$ data latch remain intact until overwritten.

Resetting and holding clear the buffer selector, data transfer buffer and $\overline{PWM}$ data latch to "0" ($\overline{PWM}$ output is "1" level).

3.3.1 Circuit configuration

Figure 3-5 shows the pulse width modulation circuit.

3.3.2 PWM output wave

(1) $\overline{PWM0}$ output

$\overline{PWM0}$ is a PWM output controlled by 14 bit data.

The basic period of the $\overline{PWM0}$ is $T_M = 2^{15}/fc$. The higher 8 bits of 14 bit data are used to control the pulse width of the pulse output with the period of $T_S = T_M/64$, which is the sub-period of the $\overline{PWM0}$. When the 8 bit data are decimal n($0 \leq n \leq 255$), this pulse width becomes n x to, where to = 2/fc.

The lower 6 bits of 14 bit data are used to control the generation of an additional to wide pulse in each T_S period. When the 6 bit data are decimal m($0 \leq m \leq 63$), the additional pulse is generated in each of m periods out of 64 periods contained in a T_M period. The relationship between the 6 bit data and the position of T_S period where the additional pulse is generated is shown in Table 3-3.

Bit position of 6 bit data	Relative position of T_S where the additional (No. i of T_S is listed)
Bit 0	32
Bit 1	16, 48
Bit 2	8, 24, 40, 56
Bit 3	4, 12, 20, 28, 36, 44, 52, 60
Bit 4	2, 6, 10, 14, 18, 22, 26, 30, ·····, 58, 62
Bit 5	1, 3, 5, 7, 9, 11, 13, 15, ·····, 59, 61, 63

Table 3-3. Correspondence between 6 bit data and the additional pulse generated T_S periods

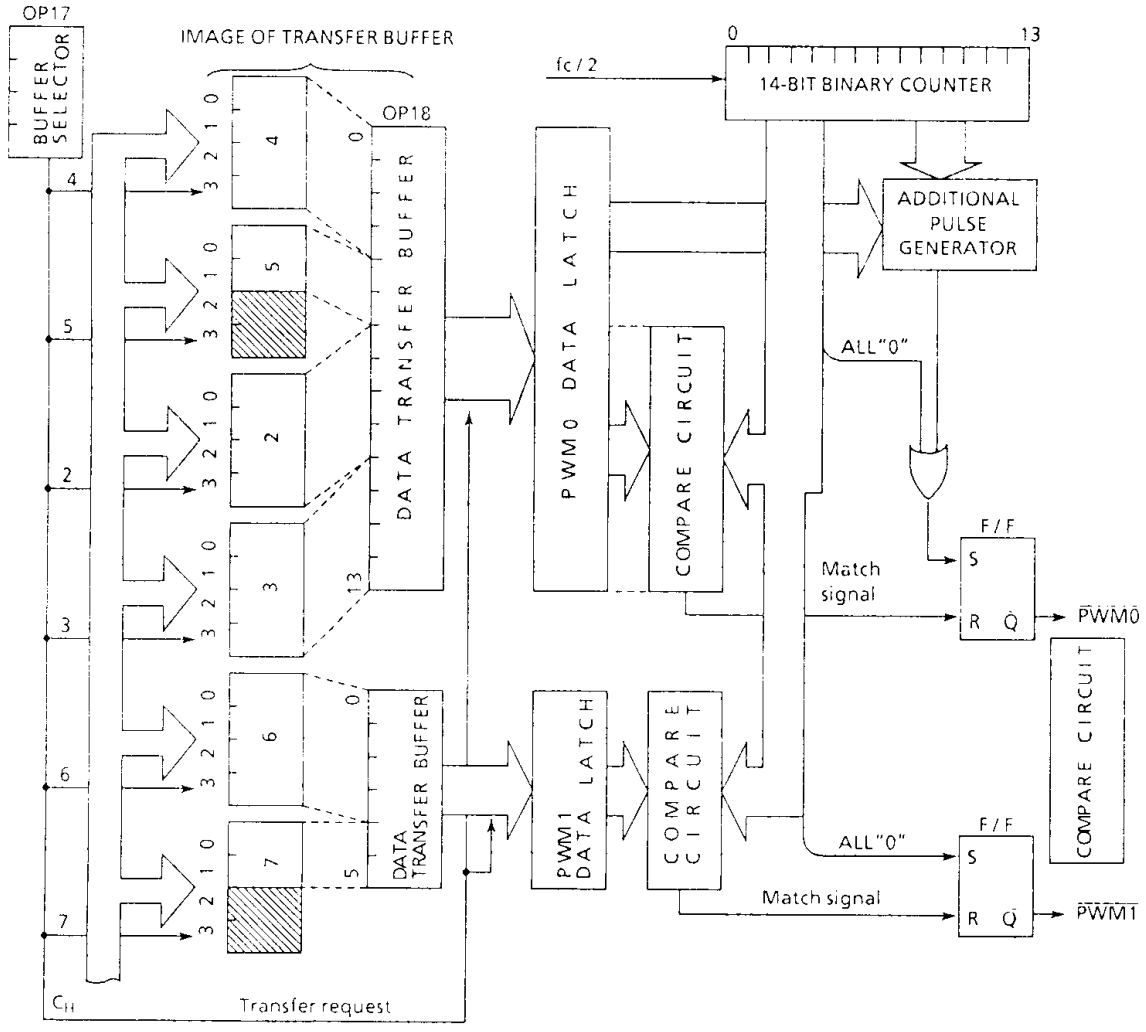


Figure 3-5. Pulse width modulation circuit

(2) $\overline{PWM1}$

$\overline{PWM1}$ is a PWM output controlled by 6 bit data. The 6 period of them is $T_M = 2^7/fc$, When the 6 bit data are decimal k ($0 < k < 63$), the pulse width becomes k x to.

The waveform is also illustrated in Figure 3-6.

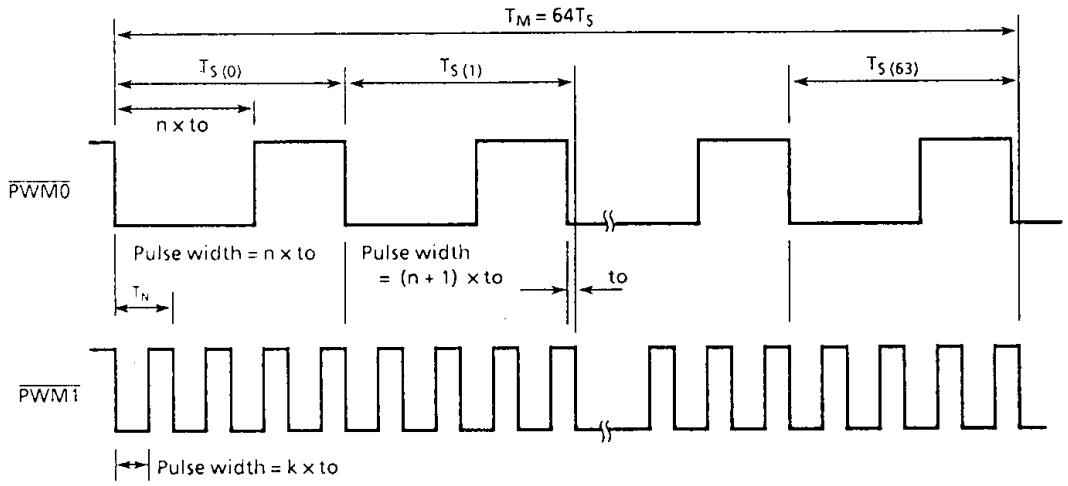


Figure 3-6. PWM Output Waveform

3.3.3 Control of PWM circuit (data transfer)

$\overline{PWM}$ output is controlled by writing the output data to the data transfer buffer (OP18). The output data are written in sections using the buffer selector (OP17). In the data transfer buffer, the respective sections of data are assigned buffer numbers and written as indicated in Table 3-4.

① The buffer number of the buffer to which the data are to be written is written to the buffer selector (OP17).
② The corresponding PWM data are written to the selected buffer.
③ The output data are written to the transfer buffer by repeating the operations in items ① and ② above.
④ When writing is completed, "C_H" is written to the buffer selector (OP17).

While the output data are being written to the transfer buffer, the previous PWM data are being output.
When "C_H" is written to the buffer selector, the output data are sent to the PWM data latch and $\overline{PWM}$ output is enabled.
The time from when "C_H" is written to the buffer selector until $\overline{PWM0}$ output is enabled is 2^{15}/fc (8192μs at 4 MHz) maximum, $\overline{PWM1}$ output is enabled is 2^9/fc (128μs at 4 MHz) maximum.

Buffer Number (OP17)	Correspondence to bit (OP18)	Mode	PWM Output
2	Bit of PWM 0 transfer buffer 9 - 6	Write	Preceding data
3	Bit of PWM 0 transfer buffer 13 - 10	Write	Preceding data
4	Bit of PWM 0 transfer buffer 3 - 0	Write	Preceding data
5	Bit of PWM 0 transfer buffer 5 - 4	Write	Preceding data
6	Bit of PWM 1 transfer buffer 3 - 0	Write	Preceding data
7	Bit of PWM 1 transfer buffer 5 - 4	Write	Preceding data
C	None	Transfer	Present data

Table 3-4. The bit and buffer number of data transfer buffer

3.4 On-screen display (OSD) circuit

The TMP47C337A contains an on-screen display circuit to indicate the channel number and present volume level on a TV screen bar display. The bar display's horizontal and vertical position and its vertical length are changed in accordance with the values stored in the data register.

3.4.1 Circuit Configuration

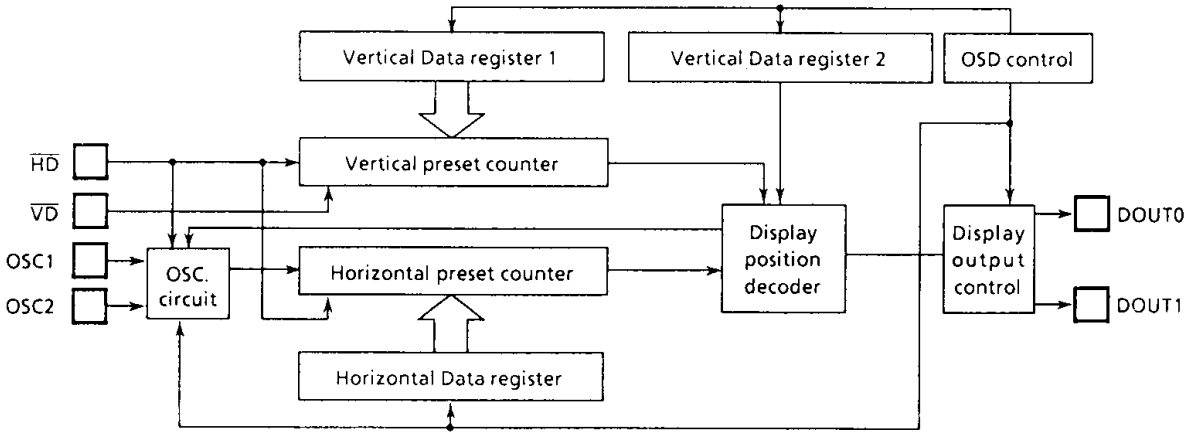


Figure 3-7. On-screen dispay circuit

3.4.2 Controlling the on-screen display

The on-screen displays are controlled by means of the command registers OP0C and OP0D, the horizontal data register, vertical data register 1, vertical data register 2, and data transfer buffers OP0A and OP0B.

The bar display's position and length are changed by the values data stored in these registers. The 8 bits of data are synchronized with vertical sync signals and are then transferred to each data register by the selection of the data register to be set through the use of OP0D and the writing of the upper four data bits into OP0B and the lower four data bits into OP0A.

Display of bar width, selection of OSD output and enabling or inhibiting of the display are performed by OP0C.

Data register selector
(Port address : OP0D) (Initial value 00**)

3	2	1	0
SHVR			

SHVR	Selection of data register
00 : Horizontal data register	
01 : Vertical data register 1	
10 : Vertical data register 2	
11 : inhibition	

OSD control command register
(Port address : OP0C) (Initial value 0000)

3	2	1	0
EOSD	WIDTH	EDOUT1	EDOUT0

EOSD	OSD control
0 : OSD disable	
1 : OSD enable	

WIDTH	Selection of display bar-width
0 : $2^3 \times 10^6$ / fosc [μsec]	
1 : $2^4 \times 10^6$ / fosc [μsec]	

EDOUT1	Selection of R50 pin function
0 : digital I/O (R50)	
1 : OSD output (DOUT1)	

EDOUT0	Selection of R42 pin function
0 : digital I/O (R42)	
1 : OSD output (DOUT0)	

Figure 3-8. Control command register

(1) Controlling OSD output

OSD is output to the DOUT1 and DOUT0 pins, each of which can be independently enabled. The bar display is enabled by the setting of EDOUT1 and EDOUT0 at EOSD = 1. If these pins are not used for OSD output, clearing EDOUT1 and EDOUT0 makes them ordinary I/O pins. The two types of display bar width in the horizontal direction are selected through the use of WIDTH.

(2) Specifying the display's horizontal start position

The display's horizontal position is determined by values stored in the horizontal data register. The display's start position after reset is at the TV screen's left edge.

Use the following equation to derive the display's horizontal start position (HS).

$HS = TOSC (HSR + 1)$

Note. T_{OSC} *: one OSD clock pulse cycle*
HSR : value stored in horizontal data register

(3) Specifying the display's vertical start position

The disiplay's vertical start position is determined by values that are stored in the vertical data register1. The display's start position after reset is at the TV screen's top edge. The display's start position is moved in 256 steps from top to bottom of the TV screen through the incrementation of values stored in the vertical data register 1.Use the following equation to derive the display's vertical start position (VS).

$VS = 2THD (VSR + 1)$

Note. T_{HD} *: one vertical sync signal cycle*
VSR : value stored in vertical data register 1

(4) Specifying vertical display bar length

Bar length is determined by values stored in the vertical data register 2.

The display bar length is increased in 256 steps from the top of the screen through the incrementation of values stored in vertical data register 2. Use the following equation to derive the display bar length (VL).

$VL = THD (VLR = 0)$
$VL = 2THD \times VLR (VLR \geqq 1)$

Where,

Note. *VL = THD (VLR = 0) VL = 2THD x VLR (VLR> = 1) THD = one vertical sync signal cycle*
VLR = value stored in vertical data register 2

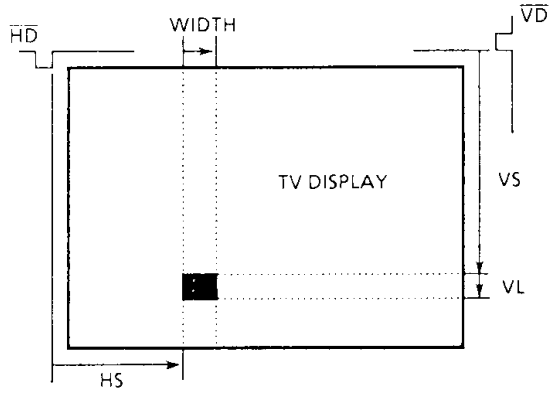


Figure 3-9.

Note. *Because the display position is moved by the access of OP0A, the rewrite order is OP0B to OP0A.*

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.3 to 7	V
Input Voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Port R5, R6, R7, XOUT	− 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Port R4, R8	− 0.3 to 10	
Output Voltage(Per 1 pin)	I_{OUT1}	Port R6	10	mA
	I_{OUT2}	Port R4, R5, R7, R8	3.2	
Output Voltage(Total)	ΣI_{OUT1}	Port R6	40	mA
Power Dissipation[Topr = 70°C]	PD		600	mW
Soldering Temperature(Time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 20 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 20 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal mode	4.5	6.0	V
			in the Hold mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	4.2	MHz
	fosc	OSC1, OSC2		2	6	

Note. Input Voltage V_{IH3}, V_{IL3} : in the HOLD mode

D.C.CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = − 20 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.7	−	V
Input Curreut	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	−	−	± 2	μA
	I_{IN2}	Ports R (Open drain)					
Input Resistance	R_{IN1}	Port K0 with pull-up		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leak Current	I_{LO}	Open drain output ports	V_{DD} = 5.5V, V_{OUT} = 5.5V	−	−	2	μA
Output High Voltage	V_{OH}	Port R6	V_{DD} = 4.5V, I_{OH} = − 200μA	2.4	−	−	V
Output Low Voltage	V_{OL}	Excepet Port R6, Xout	V_{DD} = 4.5V, I_{OL} = − 1.6mA	−	−	0.4	V
Output Low Current	I_{OL}	Port R6	V_{DD} = 4.5V, V_{OL} = 1.0V	−	10	−	mA
Suply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	−	3	6	mA
Suply Current (in the Hold mode)	I_{DDH}		V_{DD} = 5.5V	−	0.5	10	μA

Note 1. TYP. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. When the K0 port has a built-in input resistor, current by resistor is excluded. V_{IN} = 5.3V/0.2V

Note 3. When K0 port has a built-in input resistor, current value is that at time of open. Further, voltage level at R port is valid.

A/D CONVERSION

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Input Voltage	V_{AIN}	CIN		V_{SS}	−	V_{DD}	V
A/D Conversion Error	−			−	−	$\pm\frac{1}{4}$	LSB

A.C.CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = − 20 to 70°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	−	20	μs
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	−	−	ns
Low level Clock Pulse Width	t_{WCL}					

RECOMMENDED OSCILLATING CONDITIONS (V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, T_{opr} = – 20 to 70°C)

(1) 4MHz

Ceramic Resonator

CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF

KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF

Crystal Oscillator

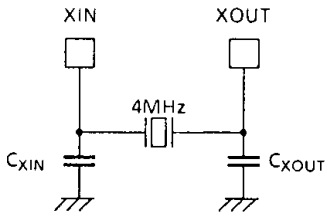
204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20pF

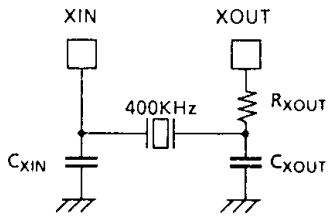
(2) 400KHz

Ceramic Resonator

CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8KΩ

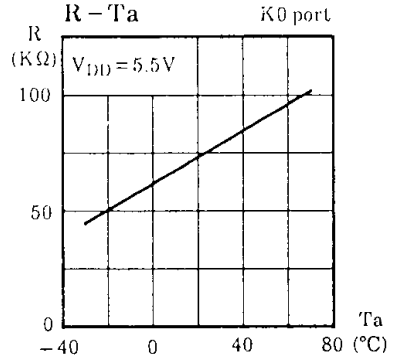
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10KΩ



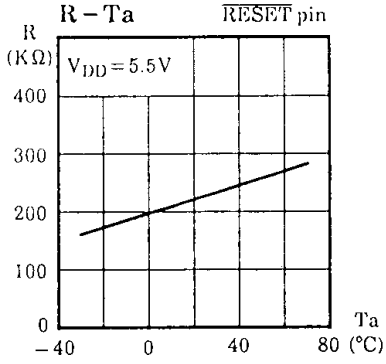


TYPICAL CHARACTERISTICS

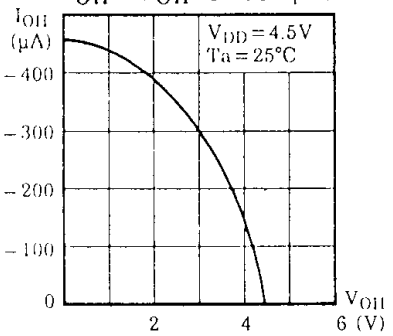
R – Ta K0 port



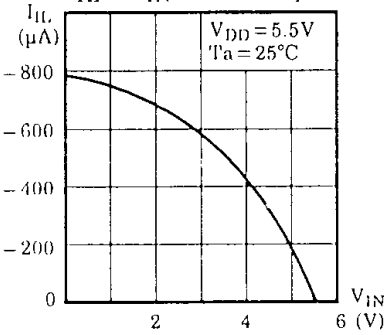
R – Ta $\overline{\text{RESET}}$ pin



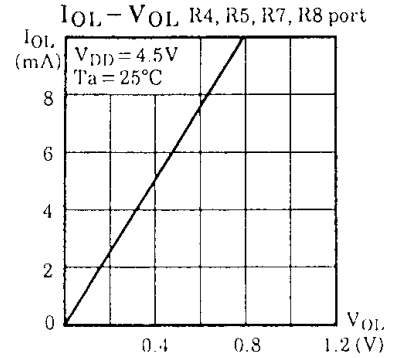
$I_{OH} - V_{OH}$ CMOS R port



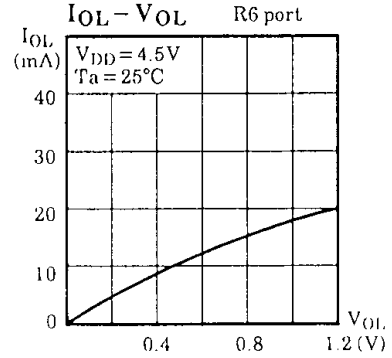
$I_{IL} - V_{IN}$ CMOS R port



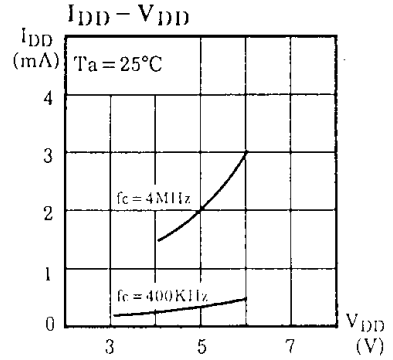
$I_{OL} - V_{OL}$ R4, R5, R7, R8 port



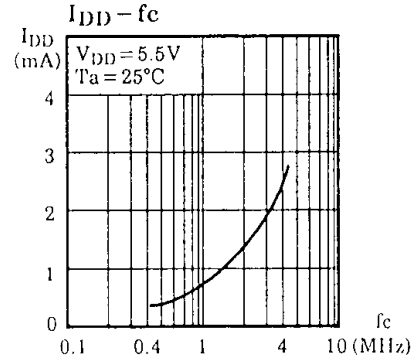
$I_{OL} - V_{OL}$ R6 port



$I_{DD} - V_{DD}$



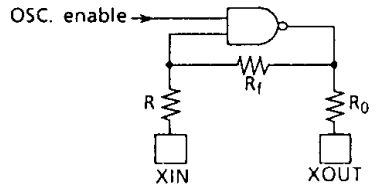
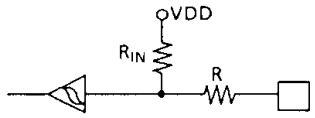
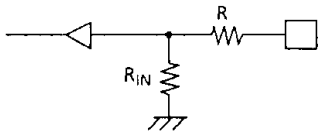
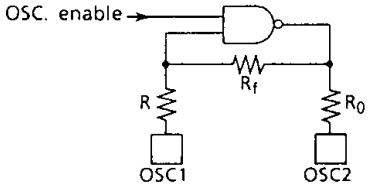
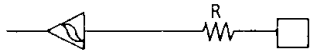
$I_{DD} - fc$



INPUT/OUTPUT CIRCUITRY

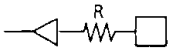
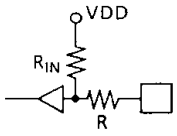
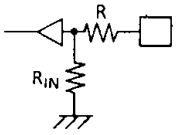
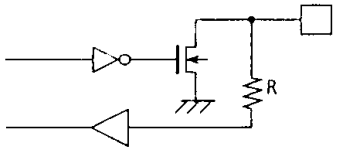
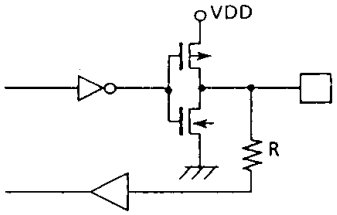
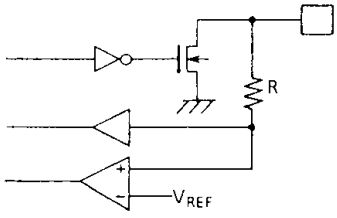
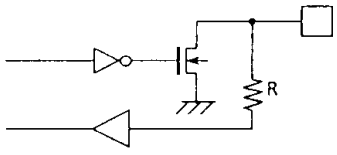
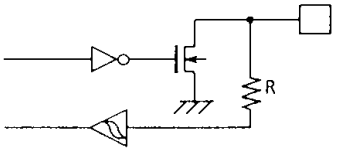
(1) Control pins

Input/Output circuitreis of the 47C337A control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output		Resonator connecting pins R = 1KΩ (typ.) R_f = 1.5MΩ (typ.) R_O = 2KΩ (typ.)
$\overline{RESET}$	Input		Hysteresis input Contained pull-up resistor R_{IN} = 220KΩ (typ.) R = 1KΩ (typ.)
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)		Hysteresis input (Sence input) R = 1KΩ (typ.)
TEST	Input		Contained pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
OSC1 OSC2	Input Output		Resonator connecting pin for OSD R = 1KΩ (typ.) R_f = 1.5MΩ (typ.) R_O = 2KΩ (typ.)
$\overline{HD}$ $\overline{VD}$	Input		Sync signal input pin Hysteresis input R = 1KΩ (typ.)

(2) I/O port

The input/output circuitries of the 47C337A I/O port are shown below, any one of the circuitries can be chosen by a code (PA-PC) as a mask option.

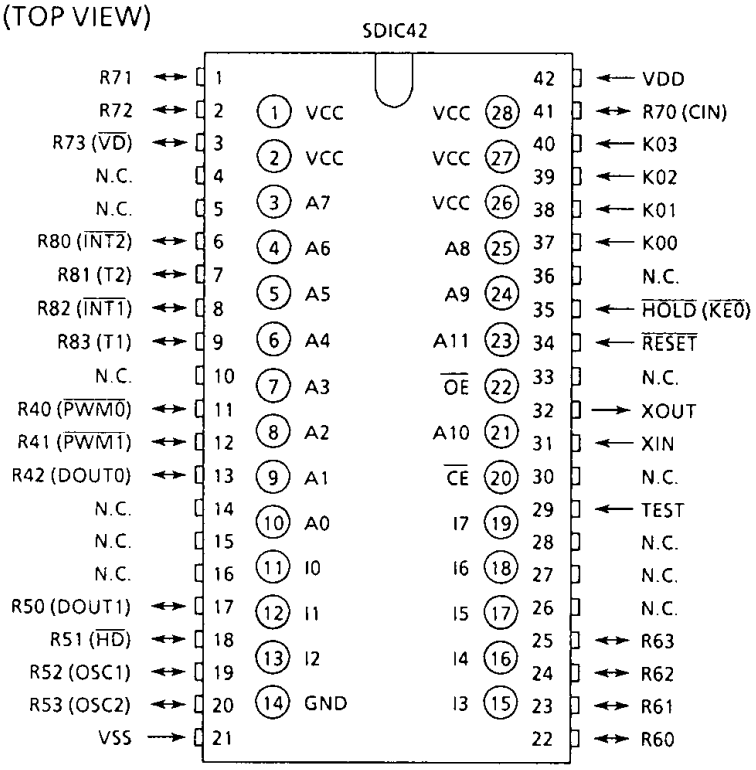
PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE	REMARKS
K0	Input	PA:  PB:  PC: 	Pull-up/Pull-down resistor R_{IN} = 70kΩ (typ.) R = 1kΩ (typ.)
R4 R5	I/O		Sink open drain output Initial "Hi-Z" R = 1kΩ (typ.)
R6	I/O		Push-pull output Initial "High" High drive current output I_{OL} = 10mA (typ.) R = 1kΩ (typ.)
R7	I/O	R70:  R71-R73: 	Sink open drain output Initial "Hi-Z" Comparator input (R70) R = 1kΩ (typ.)
R8	I/O		Sink open drain output Initial "Hi-Z" Hysteresis input R = 1kΩ (typ.)

CMOS 4-BIT MICROCONTROLLER

TMP47C937AE

The 47C937A, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C337A application systems (programs).
The 47C937A has a 42-pin package and can be made pin compatible with the mask ROM 47C337A by using the 42-to -30 pin conversion adapter (BM1103). The 47C937A which is equipped with an EPROM written the program operates like the 47C337A.

PIN ASSIGNMENT (TOP VIEW)



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A11 - A0	Output	Program memory address output
I7 - I0	Input	Program memory data input
$\overline{CE}$	Output	Chip enable signal output
$\overline{OE}$		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	t_{AD}	V_{SS} = 0V, V_{DD} = 4.5 to 6.0V C_L = 100pF Topr = – 30 to 70°C	–	–	150	ns
Data Setup Time	t_{IS}		150	–	–	ns
Data Hold Time	t_{IH}		50	–	–	ns

NOTES FOR USE

(1) Program memory
The program area are as shown in Figure 1.

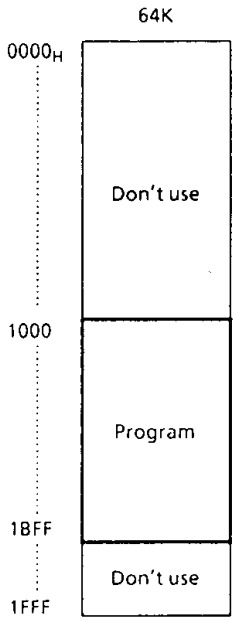
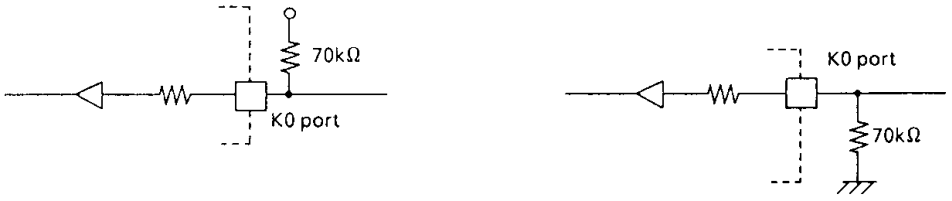


Figure 1. Program Area

(2) I/O ports
Input/Output circuitries of I/O ports in the 47C937A are similar to the code PA of the 47C337A.
When this chip is used as evaluator with other I/O code, it is necessary to provide the external resistors.



(a) Code : PB (b) Code : PC

Figure 2. I/O code and external circuitry