WM8146

12-bit (8+4-bit) Linear Sensor Image Processor

Product Preview, January 2000 Rev 1.1

DESCRIPTION

The WM8146 is a 12-bit analogue front end/digitiser IC, which processes and digitises the analogue output signals from linear CCD sensors at pixel sample rates of up to 6MSPS.

The device includes three analogue signal processing channels each of which contains Reset Level Clamping, Correlated Double Sampling and Programmable Gain and Offset adjust functions. The output from each of these channels is time multiplexed into a single high-speed 12-bit Analogue to Digital Converter. The digital output data is available in 8+4-bit wide multiplexed format, with no missing codes.

The WM8146 is controlled via a configurable serial interface, which is compatible with all of Wolfson's imaging devices.

Powered from an analogue supply voltage of 5V and a digital interface supply of either 5V or 3.3V, the WM8146 typically only consumes 175mW when operating from 5V supplies.

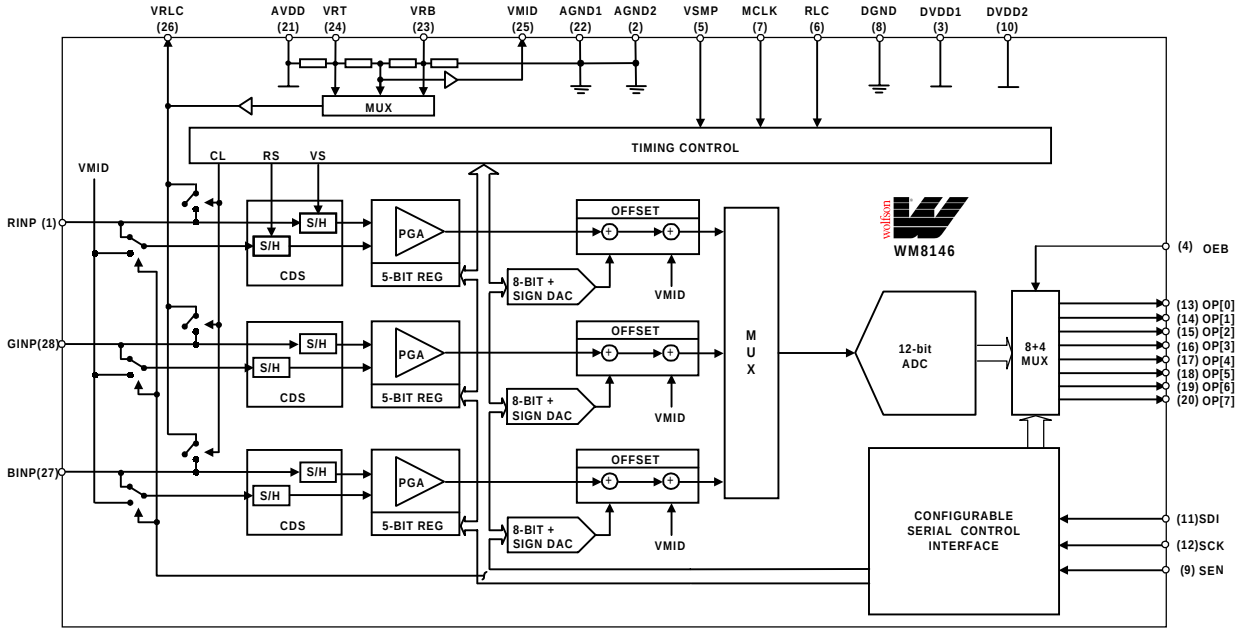
FEATURES

- **No missing codes guaranteed**
- **6MSPS sample rate**
- **Colour pixel by pixel or line by line sampling**
- **Monochrome sampling**
- **Selectable reset level clamp voltage**
- **Pixel by pixel or line by line clamping**
- **Correlated double sampling**
- **5-bit programmable gain amplifier**
- **8-bit + sign offset adjustment**
- **5V or 3.3V digital interface compatibility**
- **Serial control interface**
- **28-pin SOIC package**

APPLICATIONS

- **Flatbed scanners**
- **Multi-function peripherals**
- **Copier scanners**
- **CCD sensor interfaces**

BLOCK DIAGRAM



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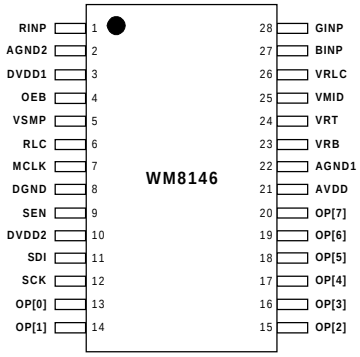
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
XWM8146CDW/V	0 to 70°C	28-pin SOIC

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	RINP	Analogue input	Red channel input video.
2	AGND2	Supply	Analogue ground (0V).
3	DVDD1	Supply	Digital supply (5V) for logic and clock generator. This must be operated at the same potential as AVDD.
4	OEB	Digital input	Output Hi-Z control, all digital outputs disabled when OEB = 1.
5	VSMP	Digital input	Video sample synchronisation pulse.
6	RLC	Digital input	Selects reset level clamp on a pixel-by-pixel basis – active high. Tie high to use on every pixel.
7	MCLK	Digital input	Master clock. This clock is applied at N times the input pixel rate (N = 2, 3, 6, 8 or any multiple of 2 thereafter depending on input sample mode).
8	DGND	Supply	Digital ground (0V).
9	SEN	Digital input	Enables the serial interface when high.
10	DVDD2	Supply	Digital supply (5V/3.3V), all digital I/O pins.
11	SDI	Digital input	Serial interface data input.
12	SCK	Digital input	Serial interface clock.
13	OP[0]	Digital output	Digital multiplexed output data bus. OEB = 0: ADC output data is available in (8+4bit) multiplexed format on pins OP[7] to OP[0]. See Operational Timing diagrams for details. OEB = 1: Output is Hi=Z.
14	OP[1]	Digital output	
15	OP[2]	Digital output	
16	OP[3]	Digital output	
17	OP[4]	Digital output	
18	OP[5]	Digital output	
19	OP[6]	Digital output	
20	OP[7]	Digital output	
21	AVDD	Supply	Analogue supply (5V). This must be operated at the same potential as DVDD1.
22	AGND1	Supply	Analogue ground (0V).
23	VRB	Analogue output	Lower reference point of ADC reference string This pin must be connected to AGND via a decoupling capacitor.
24	VRT	Analogue output	Upper reference point of ADC reference string This pin must be connected to AGND via a decoupling capacitor.
25	VMID	Analogue output	Buffered mid-point of ADC reference string This pin must be connected to AGND via a decoupling capacitor.
26	VRLC	Analogue output	Selectable analogue output voltage for RLC. This pin must be connected to AGND via a decoupling capacitor.
27	BINP	Analogue input	Blue channel input video.
28	GINP	Analogue input	Green channel input video.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

As per JEDEC specifications A112-A and A113-B, this product requires specific storage conditions prior to surface mount assembly.

CONDITION	MIN	MAX
Analogue supply voltage: AVDD	GND - 0.3V	GND + 7V
Digital supply voltages: DVDD1 – 2	GND - 0.3V	GND + 7V
Digital ground: DGND	GND - 0.3V	GND + 0.3V
Analogue grounds: AGND1 – 2	GND - 0.3V	GND + 0.3V
Digital inputs, digital outputs and digital I/O pins	GND - 0.3V	DVDD2 + 0.3V
Analogue inputs (RINP, GINP, BINP)	GND - 0.3V	AVDD + 0.3V
Other pins	GND - 0.3V	AVDD + 0.3V
Operating temperature range: T_A	0°C	+70°C
Storage temperature	-65°C	+150°C
Lead temperature (soldering, 10 sec)		+260°C
Lead temperature (soldering, 2 mins)		+183°C

Notes: 1. GND denotes the voltage of any ground pin.

2. AGND1, AGND2 and DGND pins are intended to be operated at the same potential. Differential voltages between these pins will degrade performance.

RECOMMENDED OPERATING CONDITIONS

CONDITION		SYMBOL	MIN	TYP	MAX	UNITS
Operating temperature range		T_A	0		70	°C
Analogue supply voltage		AVDD	4.75	5.0	5.25	V
Digital core supply voltage		DVDD1	4.75	5.0	5.25	V
Digital I/O supply voltage	5V I/O	DVDD2	4.75	5.0	5.25	V
	3.3V I/O	DVDD2	2.97	3.3	3.63	V

ELECTRICAL CHARACTERISTICS

Test Conditions
AVDD = DVDD1 = DVDD2 =4.75 to 5.25V, AGND = DGND = 0V, T_A = 0 to 70°C, MCLK = 12MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall System Specification (including 12-bit ADC, PGA, Offset and CDS functions) **NO MISSING CODES GUARANTEED**						
Full-scale transition error				±25	±100	mV
Zero-scale transition error				±25	±100	mV
Differential non-linearity	DNL				+1.5	LSB
References						
Upper reference voltage	VRT	AVDD = 5V	3.47	3.5	3.53	V
Lower reference voltage	VRB	AVDD = 5V	1.47	1.5	1.53	V
DAC reference voltage	VMID	AVDD = 5V	2.47	2.5	2.53	V
RLC switching impedance				500		Ω
Reset level clamp options	VRLC	AVDD = 5V	1.46	1.5	1.54	V
		Voltage set by register configuration	2.46	2.5	2.54	V
			3.46	3.5	3.54	V
Impedance VRT to VRB			250	500	750	Ω
Input Multiplexer						
CDS mode full scale input range (V_{VS}-V_{RS})		x denotes the channel selected		$\frac{2}{Gx}$		Vp-p
Channel to channel gain matching				1		%
Offset DAC (monotonicity guaranteed)						
Resolution			8 (+sign)			bits
Zero code voltage			VMID-20		VMID+20	mV
Full scale voltage error			0		20	mV
Differential non-linearity	DNL			0.1	0.5	LSB
Integral non-linearity	INL			0.25	1	LSB
Step size		DACRNG=0		4.9		mV/step
		DACRNG=1		7.4		mV/step
Output voltage		DACRNG=0		+/-1.25		V
		DACRNG=1		+/-1.875		V
Programmable Gain Amplifier (monotonicity guaranteed)						
Resolution			5			bits
Max gain, each channel	G_{MAX}			8.25		V/V
Min gain, each channel	G_{MIN}			0.5		V/V
Gain error, each channel				1		%
DIGITAL SPECIFICATIONS						
Digital Inputs						
High level input voltage	V_{IH}		0.8 * DVDD2			V
Low level input voltage	V_{IL}				0.2 * DVDD2	V
High level input current	I_{IH}				1	µA
Low level input current	I_{IL}				1	µA
Input capacitance	C_I			5		pF
Digital Outputs						
High level output voltage	V_{OH}	I_{OH} = 1mA	DVDD2 - 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			DGND + 0.5	V
High impedance output current	I_{OZ}				1	µA

Test Conditions
AVDD = DVDD1 = DVDD2 =4.75 to 5.25V, AGND = DGND = 0V, T_A = 0 to 70°C, MCLK = 12MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Currents						
Total supply current – active				35		mA
Supply current – full power down mode				5		mA

INPUT VIDEO SAMPLING

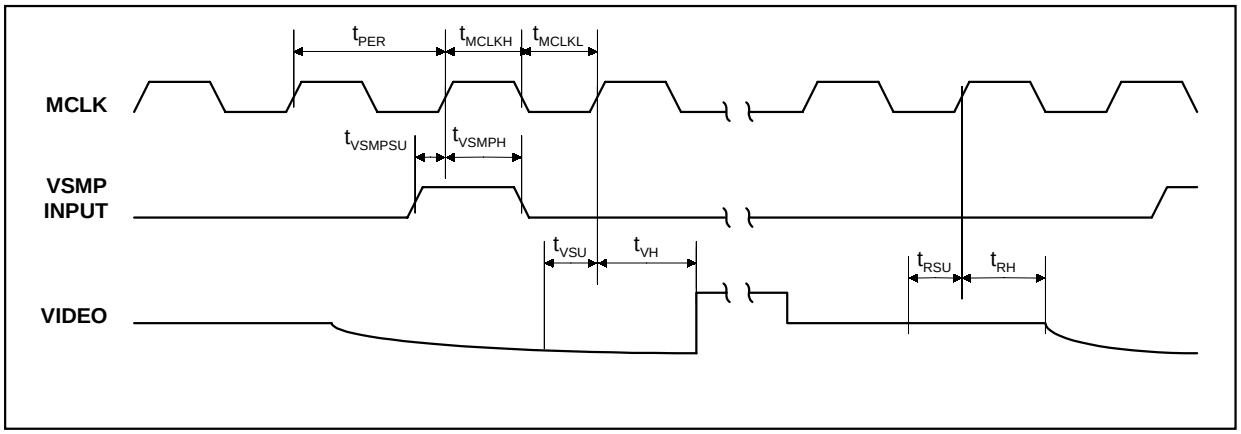


Figure 1 Input Video Timing

Test Conditions
AVDD = DVDD1 = DVDD2 = 4.75 to 5.25V, AGND = DGND = 0V, T_A = 0 to 70°C, MCLK = 12MHz unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MCLK period	t_{PER}		83.3			ns
MCLK high period	t_{MCLKH}		37.5			ns
MCLK low period	t_{MCLKL}		37.5			ns
VSMP set-up time	t_{VSMPSU}		10			ns
VSMP hold time	t_{VSMPH}		10			ns
Video level set-up time	t_{VSU}		10			ns
Video level hold time	t_{VH}		15			ns
Reset level set-up time	t_{RSU}		10			ns
Reset level hold time	t_{RH}		15			ns

Notes: 1. t_{VSU} and t_{RSU} denote the set-up time required after the input video signal has settled.
2. Parameters are measured at 50% of the rising/falling edge.

OUTPUT DATA TIMING

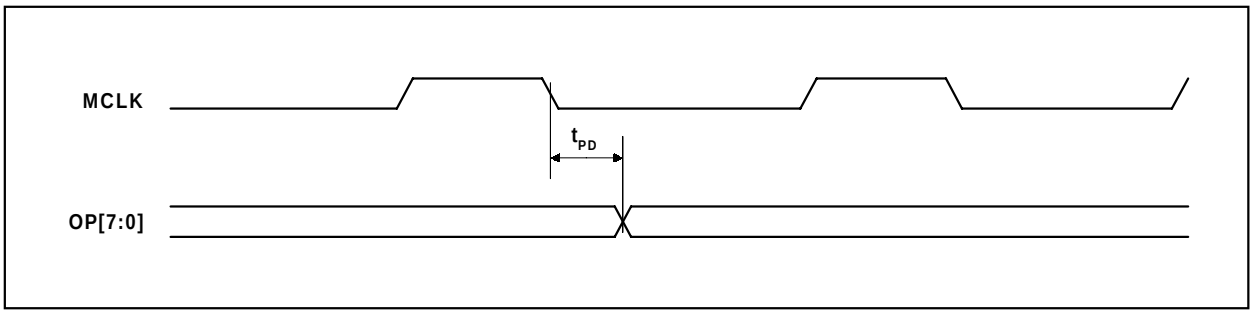


Figure 2 Output Data Timing

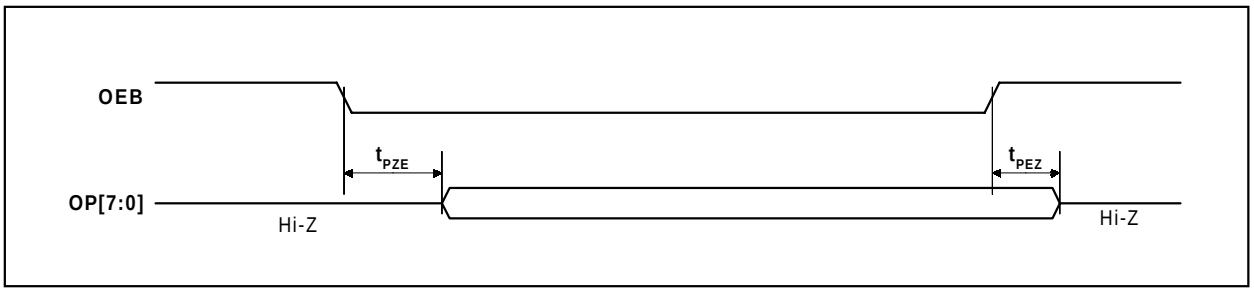


Figure 3 Output Data Enable Timing

Test Conditions
AVDD = DVDD1 = DVDD2 = 4.75 to 5.25V, AGND = DGND = 0V, T_A = 0 to 70°C, MCLK = 12MHz unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output propagation delay	t_{PD}	I_{OH} = 1mA, I_{OL} = 1mA			75	ns
Output enable time	t_{PZE}				50	ns
Output disable time	t_{PEZ}				25	ns

SERIAL INTERFACE

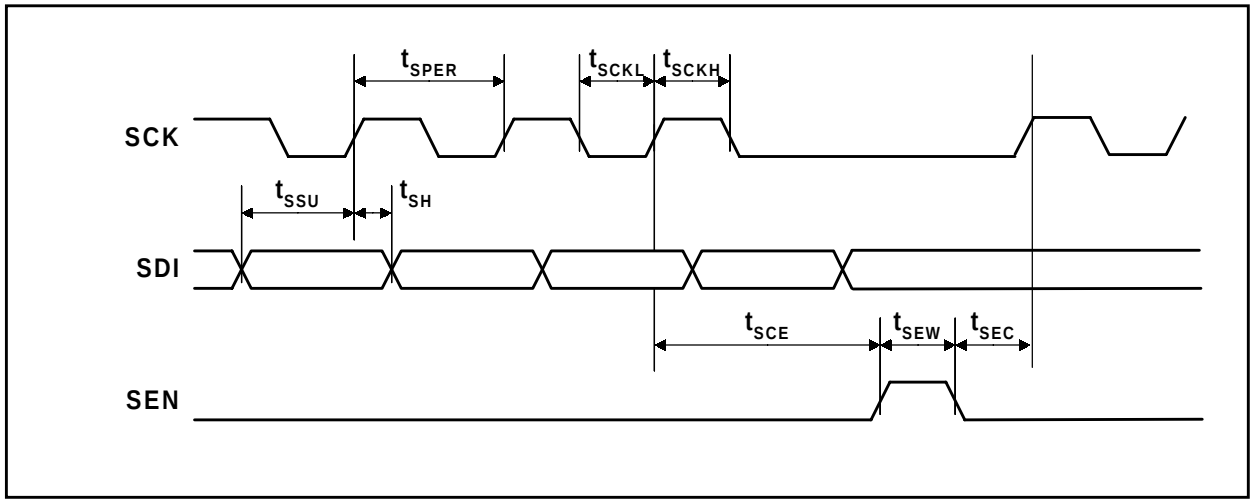


Figure 4 Serial Interface Timing

Test Conditions
AVDD = DVDD1 = DVDD2 = 4.75 to 5.25V, AGND = DGND = 0V, T_A = 0 to 70°C, MCLK = 12MHz unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SCK period	t_{SPER}		83.3			ns
SCK high	t_{SCKH}		37.5			ns
SCK low	t_{SCKL}		37.5			ns
SDI set-up time	t_{SSU}		10			ns
SDI hold time	t_{SH}		10			ns
SCK to SEN set-up time	t_{SCE}		20			ns
SEN to SCK set-up time	t_{SEC}		20			ns
SEN pulse width	t_{SEW}		50			ns

Note: Parameters are measured at 50% of the rising/falling edge.

DEVICE DESCRIPTION

GENERAL OPERATION

A block diagram of the device showing the signal path is presented on Page 1.

The WM8146 samples the three inputs (RINP, GINP and BINP) simultaneously. The device then processes the sampled video signal with respect to the video reset level or the reference level VMID using three processing channels.

Each processing channel consists of an input sampling block with optional reset level clamping (RLC) and correlated double sampling (CDS), a 5-bit programmable gain amplifier (PGA) and an 8-bit (+sign) programmable offset DAC.

For colour operation, the resulting analogue outputs from the three channels are multiplexed into a 12-bit ADC. For monochrome operation the resulting analogue output from the selected channel only is multiplexed into the ADC. The ADC then converts the analogue signal to a 12-bit digital word. The digital output from the ADC is presented on an 8-bit wide output bus, in 8+4-bit multiplexed format.

Internal control registers determine the configuration of the device, including the gain and offset applied to each channel. These registers are programmable via the serial interface.

RESET LEVEL CLAMPING (RLC)

CONFIGURATION

To ensure that the signal applied to the WM8146 lies within its input range, the CCD output signal is usually level shifted by a.c. coupling through a capacitor, $C_{IN.}$ The RLC circuit clamps the WM8146 side of this capacitor to a selected voltage during the CCD reset level. The RLC voltage VRLC, is selected by control bits RLC[1:0] in setup register 3.

A typical input configuration demonstrating reset level clamping and CDS circuitry is shown in Figure 5. A clamp pulse, CL, is generated from MCLK and VSMP by the timing control block. When CL is active the voltage on the WM8146 side of C_{IN}, at RINP, is forced to the RLC voltage VRLC by switch 1. When the CL pulse turns off, the voltage at RINP initially remains at VRLC but any subsequent variation in sensor voltage (from reset to video level) will couple through C_{IN} to RINP.

Reset level clamping is compatible with both CDS and non-CDS operating modes, as selected by switch 2.

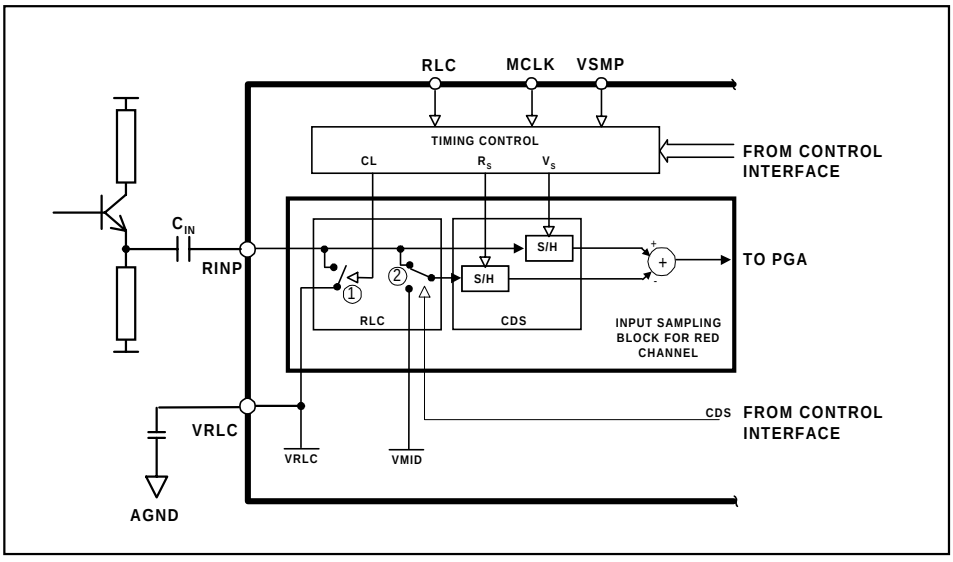


Figure 5 Reset Level Clamping and CDS Circuitry

TIMING

Figure 6 illustrates the use of the RLC pin, MCLK and VSMP to control the timing of the CL pulse for a typical CCD waveform. The CL pulse is applied during the reset period.

The input signal applied to the RLC pin is sampled on the positive edge of MCLK that occurs during each VSMP pulse. The sampled level, high (or low) controls the presence (or absence) of the internal CL pulse on the next reset level. The position of CL can be adjusted by using control bits CDSREF[1:0], as shown in Figure 7.

The VRLC pin outputs the analogue RLC voltage selected via control set-up register 3 bits RLC[1:0].

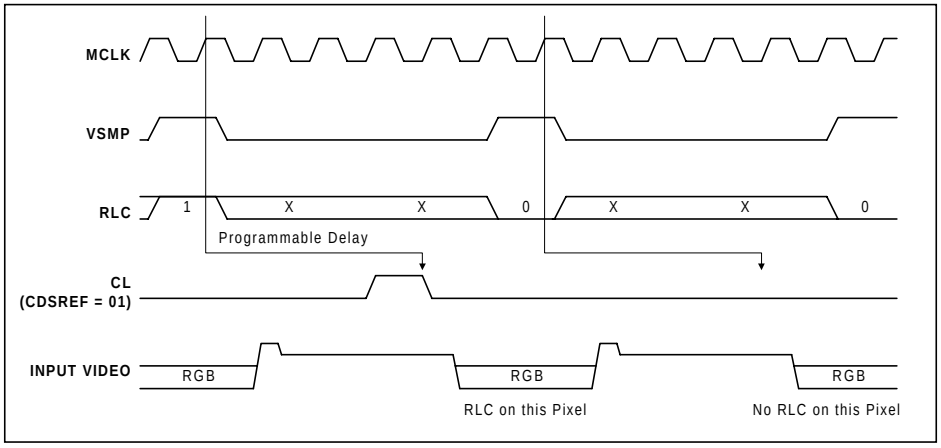


Figure 6 Relationship of RLC Pin, MCLK and VSMP to Internal Clamp Pulse, CL

CDS/NON-CDS PROCESSING

For CCD type input signals, the signal may be processed using CDS, which will remove pixel-by-pixel common mode noise. For CDS operation, the video level is processed with respect to the video reset level, regardless of whether RLC has been performed. To sample using CDS, control bit CDS must be set to 1 (default), this controls switch 2 (Figure 5) and causes the signal reference to come from the video reset level. The time at which the reset level is sampled, by clock R_S/CL, is adjustable by programming control bits CDSREF[1:0], as shown in Figure 7 .

For CIS type sensor signals, non-CDS processing is used. In this case, the video level is processed with respect to the reference voltage VMID.

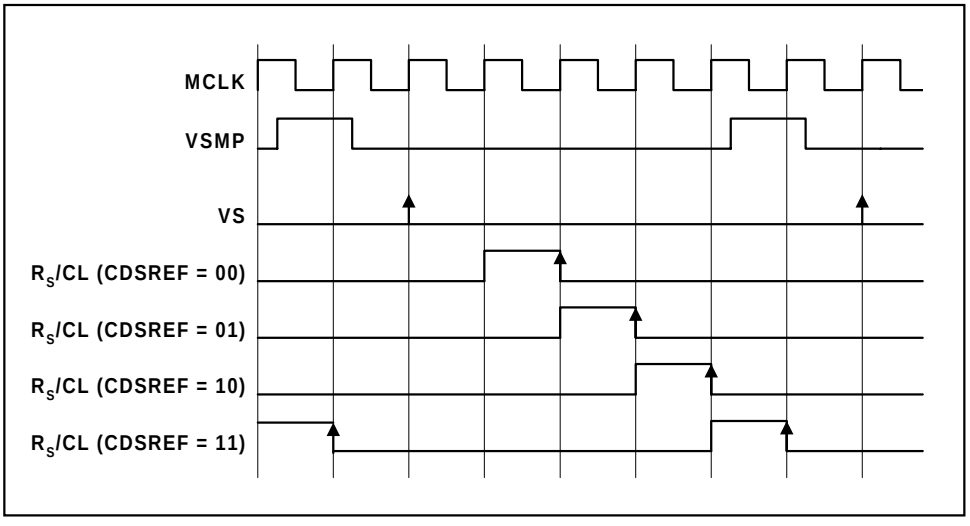


Figure 7 Reset Sample and Clamp Timing

OFFSET ADJUST AND PROGRAMMABLE GAIN

The output from the CDS block is a differential signal, which is amplified by a 5-bit PGA then added to the output of an 8-bit (+sign) offset DAC to compensate for sensor d.c. offsets. The gain and offset for each channel are independently programmable by writing to control bits DAC[7:0] and PGA[4:0]. The following diagram shows the signal path through the device.

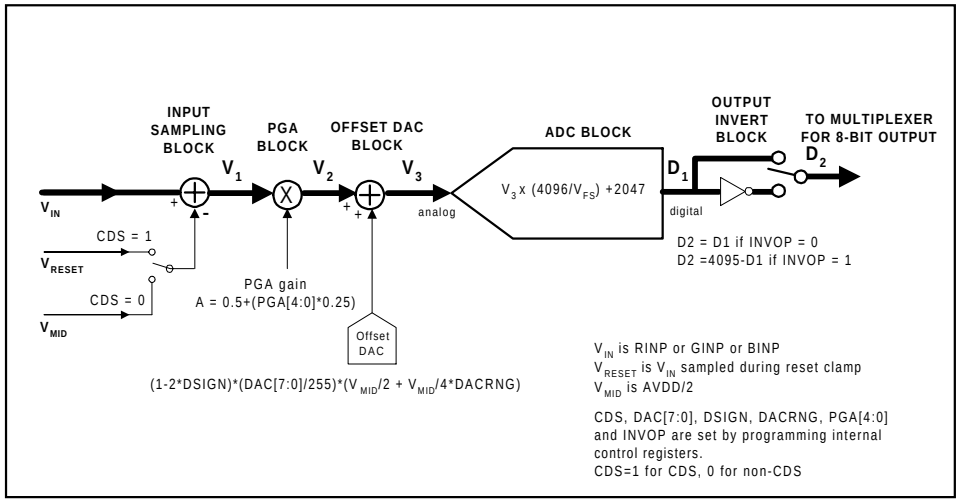


Figure 8 Signal Flow Diagram

The following equations enable the user to calculate the settings required for the PGAs and offset DACs.

INPUT SAMPLING AND REFERENCING

If CDS=1, the previously sampled reset level, V_{RESET}, is subtracted from the input video signal V_{IN} (i.e. CDS operation).

$V_1 = V_{IN} - V_{RESET}$

If CDS=0, the simultaneously sampled V_{MID} is subtracted instead (i.e. non-CDS operation).

$V_1 = V_{IN} - V_{MID}$

GAIN ADJUST

The signal is then multiplied by the PGA gain, approximately 0.5 to 8.25 in 32 equal gain steps.

$V_2 = V_1 * G$

$= V_1 * (0.5+(PGA[4:0]*0.25))$

OFFSET (BLACK-LEVEL) ADJUST

The resultant signal is added to the Offset DAC output which has a range of VMID/2 (or 1.5*VMID/2 if the DACRNG bit is set).

$V_3 = V_2 + V_{DAC}$

$= V_2 + [(1-2*DSIGN) * DAC\_CODE/255 * (VMID/2 + VMID/4 * DACRNG)]$

ANALOGUE TO DIGITAL CONVERSION

The analogue signal is then converted to a 12-bit unsigned number. This is equivalent to a multiplication by $4096/(V_{FS})$, where V_{FS} = 2V .

$D_1 == INT\{ (V_3/V_{FS}) * 4096 \} + 2047$

At this stage, the input to the ADC should be between -1V and +1V, so D_1[11:0] should lie between -2047 and +2048. If the input is over-range, it will be clipped to within the range (-2047,2048).

2047 is added to the ADC output, to give code 2047 for zero input signal to the ADC. This is equivalent to the +VMID shown in the block diagram on page 1.

DIGITAL POLARITY ADJUST

The polarity of the digital output may be inverted by control bit INVOP. If INVOP=0, negative-going input video will give negative-going digital output. If INVOP=1, negative-going video will give positive-going digital output.

$D_2 = D_1$ … (INVOP=0)

$D_2 = 4095 – D_1$ … (INVOP=1)

DIGITAL CONTROL AND I/O FUNCTIONS

OUTPUT DATA

Data appears on the pins **OP[7:0]** and changes after every negative-going **MCLK** edge, as shown in Figure 9 .

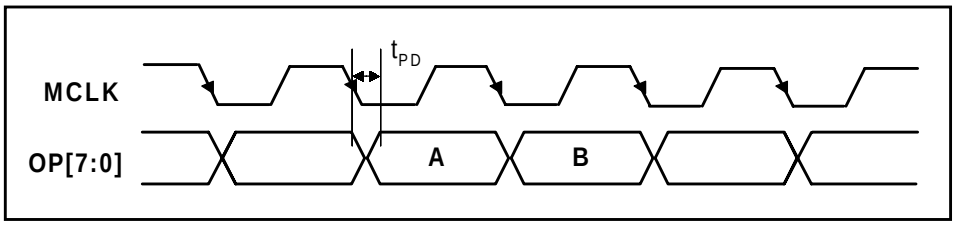


Figure 9 WM8146 Output Timing

A = d11, d10, d9, d8, d7, d6, d5, d4 Pin OP[7] to OP[0]

B = d3, d2, d1, d0, 0, CC[1], CC[0], OVRNG Pin OP[7] to OP[0]

Where

CC1/CC0: These bits show from which channel the current output was taken. 00 = RED, 01 = GREEN, 10 = BLUE.

OVRNG: This bit indicates if the current output pixel has exceeded the maximum or minimum range during processing. 1 = out of range, 0 = within range.

CONTROL INTERFACE

The internal control registers are programmable via the serial digital control interface.

REGISTER WRITE

The serial interface involves three dedicated pins, **SCK, SDI, SEN** (refer to Figure 10). A six-bit address is clocked in through **SDI** MSB first followed by an eight-bit data word, also MSB first. Each bit is latched on the rising edge of **SCK**. Once the data has been shifted into the device, a pulse is applied to **SEN** to transfer the data to the appropriate internal register. Note all valid registers have address bit a4 equal to 0.

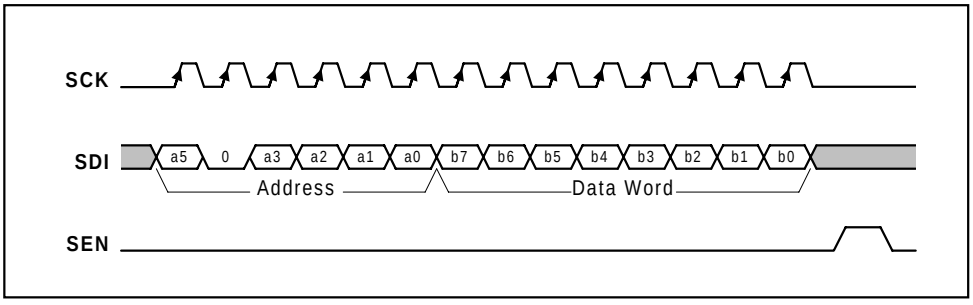


Figure 10 Register Write Timing

TIMING REQUIREMENTS

To use this device a master clock (MCLK) of up to 12MHz and a per-pixel synchronisation clock (VSMP) of up to 6MHz are required. These clocks drive a timing control block, which produces

internal signals to control the sampling of the video signal. MCLK to VSMP ratios and maximum sample rates for the various modes are shown in Table 1.

POWER SUPPLY

The WM8146 can run from a 5V single supply or from split 5V (core) and 3.3V (digital interface) supplies.

OPERATING MODES

Table 1 summarises the most commonly used modes, the clock waveforms required and the register contents required for CDS and non-CDS operation.

MODE	DESCRIPTION	CDS AVAILABLE	MAX SAMPLE RATE	SENSOR INTERFACE DESCRIPTION	TIMING REQUIRE-MENTS	REGISTER CONTENTS WITH CONTROL BIT CDS=1	REGISTER CONTENTS WITH CONTROL BIT CDS=0
1	Colour Pixel-by-Pixel	Yes	2MSPS	The 3 input channels are sampled in parallel. The signal is then gain and offset adjusted before being multiplexed into a single data stream and converted by the ADC, giving an output data rate of 6MSPS max.	MCLK max = 12MHz MCLK:VSMP ratio is 6:1	SetReg1: 03(hex)	SetReg1: 01(hex)
2	Monochrome/ Colour Line-by-Line	Yes	2MSPS	As mode 1 except: Only one input channel at a time is continuously sampled.	MCLK max = 12MHz MCLK:VSMP ratio is 6:1	SetReg1: 07(hex) SetReg3 bits 7:6 determine which input is to be sampled	SetReg1: 05(hex) SetReg3 bits 7:6 determine which input is to be sampled
3	Fast Monochrome/ Colour Line-by-Line	Yes	4MSPS	Identical to mode 2	MCLK max = 12MHz MCLK:VSMP ratio is 3:1	Identical to mode 2 plus SetReg3: bits 5:4 must be set to 0(hex)	Identical to mode 2
4	Maximum speed Monochrome/ Colour Line-by-Line	No	6MSPS	Identical to mode 2	MCLK max = 12MHz MCLK:VSMP ratio is 2:1	CDS not possible	SetReg1: 45(hex) SetReg3 bits 7:6 determine which input is to be sampled
5	Slow Colour Pixel-by-Pixel	Yes	1.5MSPS	Identical to mode 1	MCLK max = 12MHz MCLK:VSMP ratio is 2n:1, $n \geq 4$	Identical to mode 1	Identical to mode 1
6	Slow Monochrome/ Colour Line-by-Line	Yes	1.5MSPS	Identical to mode 2	MCLK max = 12MHz MCLK:VSMP ratio is 2n:1, $n \geq 4$	Identical to mode 2	Identical to mode 2

Table 1 WM8146 Operating Modes

OPERATING MODE TIMING DIAGRAMS

The following diagrams output data, MCLK, VSMP and input video requirements for operation of the most commonly used modes as shown in Table 1 . The diagrams are identical for both CDS and non-CDS operation. Outputs from RINP, GINP and BINP are shown as R, G and B respectively. X denotes invalid data.

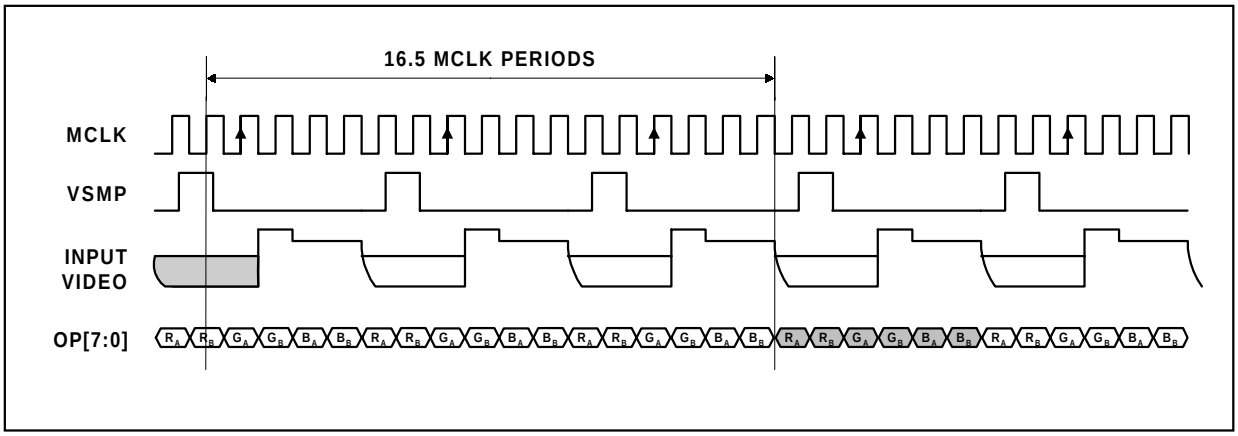


Figure 11 Mode 1 Operation

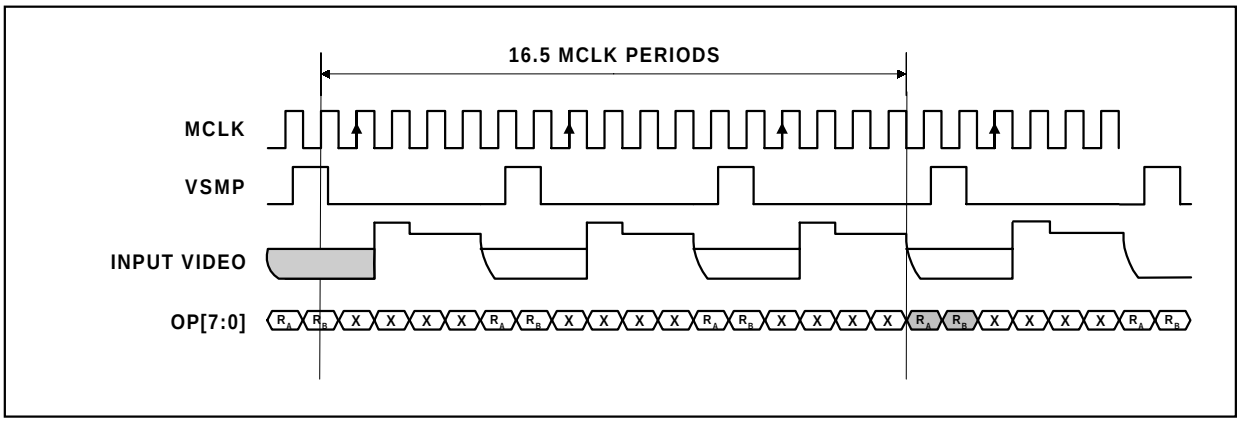


Figure 12 Mode 2 Operation

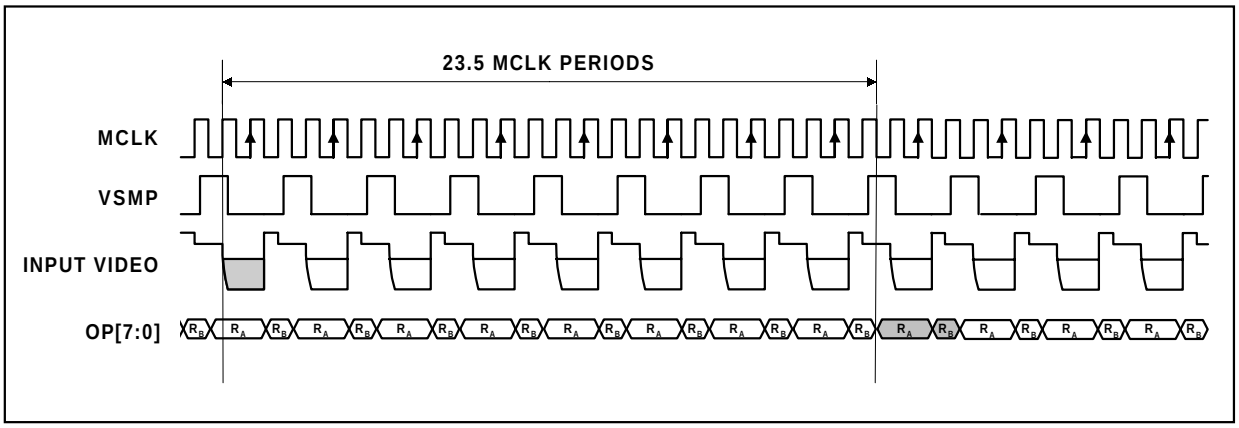


Figure 13 Mode 3 Operation

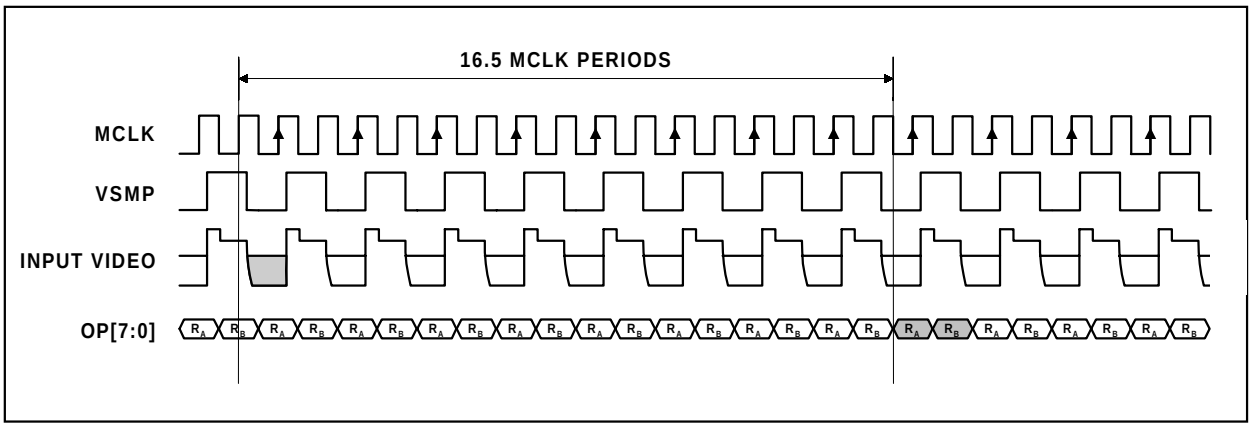


Figure 14 Mode 4 Operation

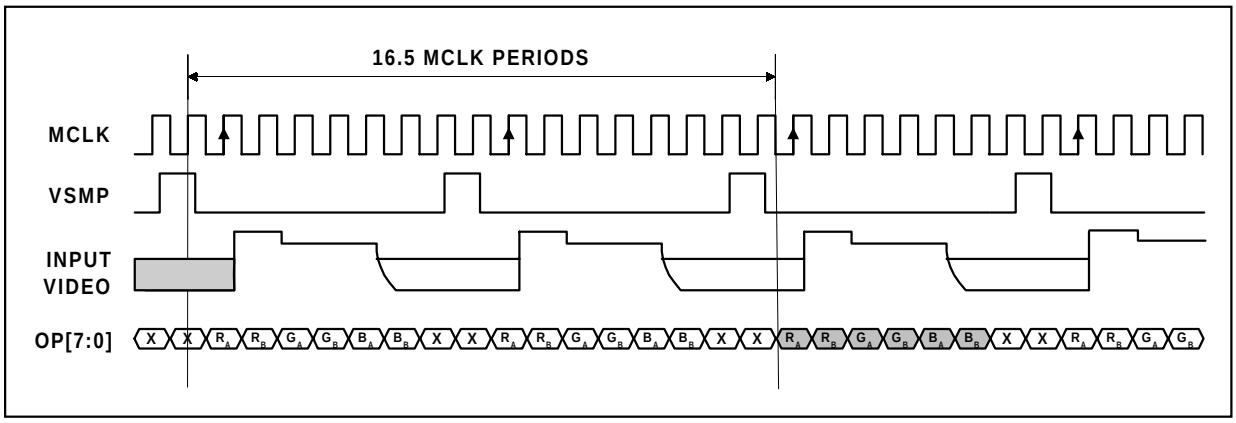


Figure 15 Mode 5 Operation (MCLK:VSMP Ratio = 8:1)

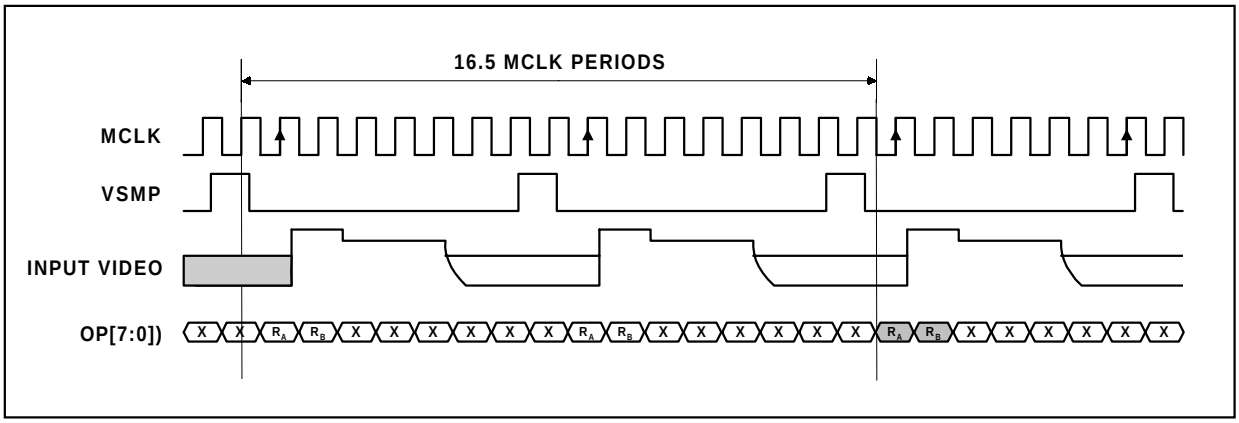


Figure 16 Mode 6 Operation (MCLK:VSMP Ratio = 8:1)

DEVICE CONFIGURATION

REGISTER MAP

Table 2 describes the location of each control bit used to determine the operation of the WM8146. The register map is programmed by writing the required codes to the appropriate addresses via the serial interface.

Address	Description	Def	BIT							
<a5:a0>		(hex)	b7	b6	b5	b4	b3	b2	b1	b0
000001	Setup Register 1	03		VSMP6M				MONO	CDS	ENADC
000010	Setup Register 2	00						INVOP		
000011	Setup Register 3	11	CHAN[1]	CHAN[0]	CDSREF[1]	CDSREF[0]			RLC[1]	RLC[0]
000100	Software Reset	00								
000101	Setup Register 4	00							DACRNG	
100000	DAC Value (Red)	00	DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]
100001	DAC Value (Green)	00	DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]
100010	DAC Value (Blue)	00	DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]
100011	DAC Value (R+G+B)	00	DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]
100100	DAC Sign (Red)	00								DSIGN
100101	DAC Sign (Green)	00								DSIGN
100110	DAC Sign (Blue)	00								DSIGN
100111	DAC Sign (R+G+B)	00								DSIGN
101000	PGA Gain (Red)	00				PGA[4]	PGA[3]	PGA[2]	PGA[1]	PGA[0]
101001	PGA Gain (Green)	00				PGA[4]	PGA[3]	PGA[2]	PGA[1]	PGA[0]
101010	PGA Gain (Blue)	00				PGA[4]	PGA[3]	PGA[2]	PGA[1]	PGA[0]
101011	PGA Gain (R+G+B)	00				PGA[4]	PGA[3]	PGA[2]	PGA[1]	PGA[0]

Table 2 Register Map

REGISTER MAP DESCRIPTION

REGISTER	BIT NO	BIT NAME(S)	DEFAULT	DESCRIPTION
Setup Register 1	0	ENADC	1	ADC standby control : 0=standby, 1=active
	1	CDS	1	Select correlated double sampling mode: 0=single ended mode, 1=CDS mode
	2	MONO	0	Mono/colour select: 0=colour, 1=monchrome operation
	6	VSMP6M	0	Required when VSMP at 6MSPS: 0=other mode, 1=VSMP at 6MSPS
Setup Register 2	2	INVOP	0	Digitally inverts the polarity of input data. 0= negative going video gives negative going output, 1=negative-going video gives positive going output data.
Setup Register 3	1:0	RLC[1:0]	01	Reset Level Clamp Voltage: 00 = 1.5V; 01 = 2.5V; 10 = 1.5V; 11 = Reserved
	5:4	CDSREF[1:0]	01	CDS mode reset timing adjust 00 = advance 1 MCLK period 01 = Normal 10 = Retard 1 MCLK period 11 = Retard 2 MCLK periods
	7:6	CHAN[1:0]	00	Monochrome mode channel select 00 = Red channel select 01 = Green channel select 10 = Blue channel select 11 = Reserved
Software Reset				Write any value to the Software Reset register to cause all cells to be reset.
Setup Register 4	1	DACRNG	0	Offset DAC Output Range: 0 = DAC Output range =VMID/2 = +/-1.25V 1 = DAC output Range = 1.5*VMID/2 = +/-1.875V
Registers 100100 to 100111	0	DSIGN	0	Polarity of Offset DAC output 0 = Positive Output (Offset added) 1 = Negative Output (Offset removed)

Table 3 Register Control Bits

RECOMMENDED EXTERNAL COMPONENTS

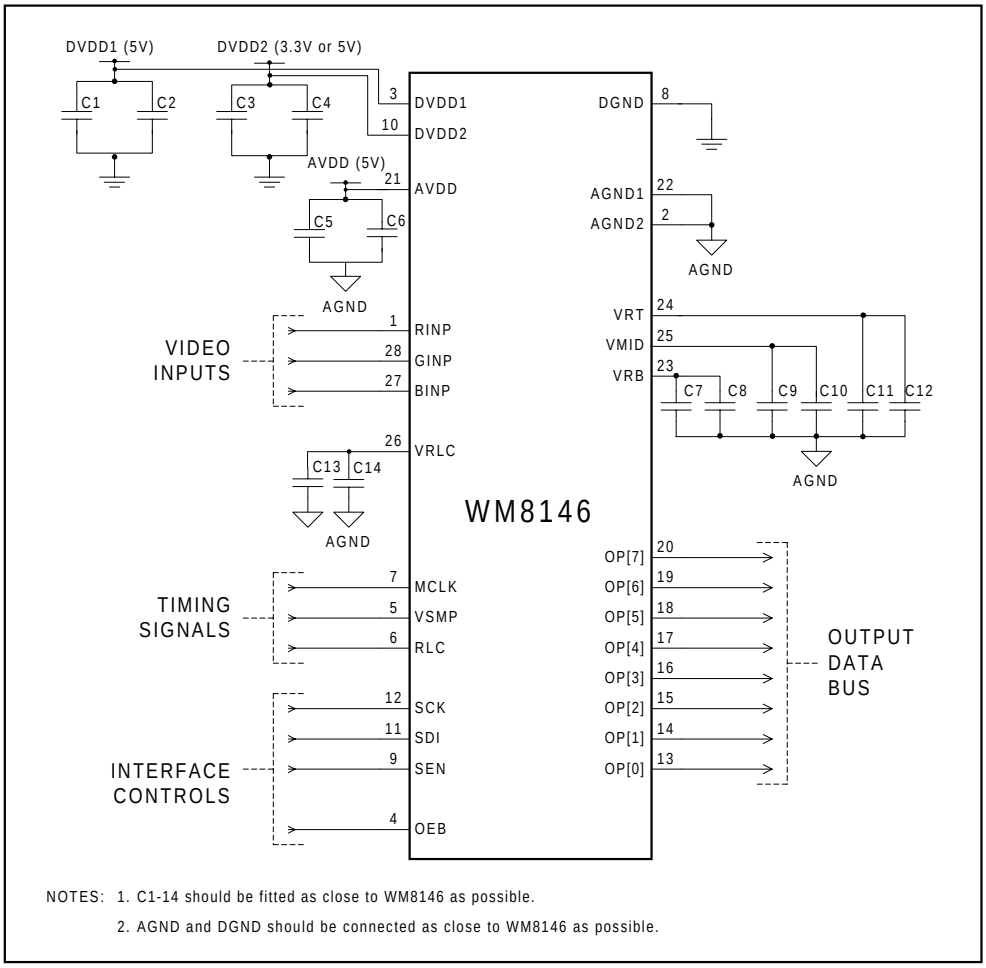


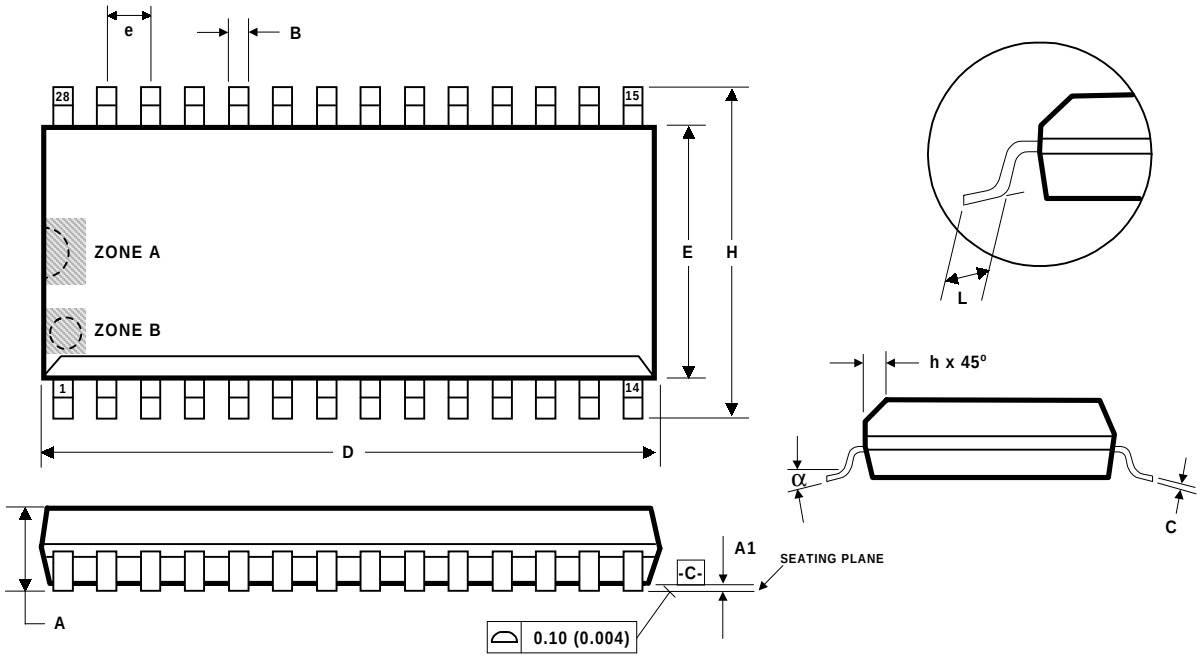
Figure 17 External Components Diagram

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1	100nF	De-coupling for DVDD1.
C2	10µF	Reservoir capacitor for DVDD1.
C3	100nF	De-coupling for DVDD2.
C4	10µF	Reservoir capacitor for DVDD2
C5	100nF	De-coupling for AVDD.
C6	10µF	Reservoir capacitor for AVDD
C7	100nF	De-coupling for VRB..
C8	10µF	Reservoir capacitor for VRB.
C9	100nF	De-coupling for VMID
C10	22µF	Reservoir capacitor for VMID.
C11	100nF	De-coupling for VRT
C12	10µF	Reservoir capacitor for VRT
C13	100nF	De-coupling capacitor for VRLC
C14	10µF	Reservoir capacitor VRLC

Table 4 External Components Descriptions

PACKAGE DIMENSIONS

D: 28 PIN SOICW 7.5mm (0.3") Wide Body, 1.27mm Lead Pitch **DM016.B**



Symbols	Dimensions (mm)		Dimensions (Inches)	
	MIN	MAX	MIN	MAX
A	2.35	2.65	0.0926	0.1043
A_1	0.10	0.30	0.0040	0.0118
B	0.33	0.51	0.0130	0.0200
C	0.23	0.32	0.0091	0.0125
D	17.70	18.10	0.6969	0.7125
e	1.27 BSC		0.0500 BSC	
E	7.40	7.60	0.2914	0.2992
h	0.25	0.75	0.0100	0.0290
H	10.00	10.65	0.3940	0.4190
L	0.40	1.27	0.0160	0.0500
α	0^o	8^o	0^o	8^o
REF:	JEDEC.95, MS-013			

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).
D. MEETS JEDEC.95 MS-013, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.
E. PIN ONE INDICATORS WILL BE LOCATED IN EITHER ZONE A OR ZONE B.