

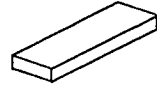
1/4 DUTY LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6437 is a 1/4 duty LCD driver for segment type LCD panel.

The LCD driver consists of 4-common and 32-segment drives up to 128 segments.

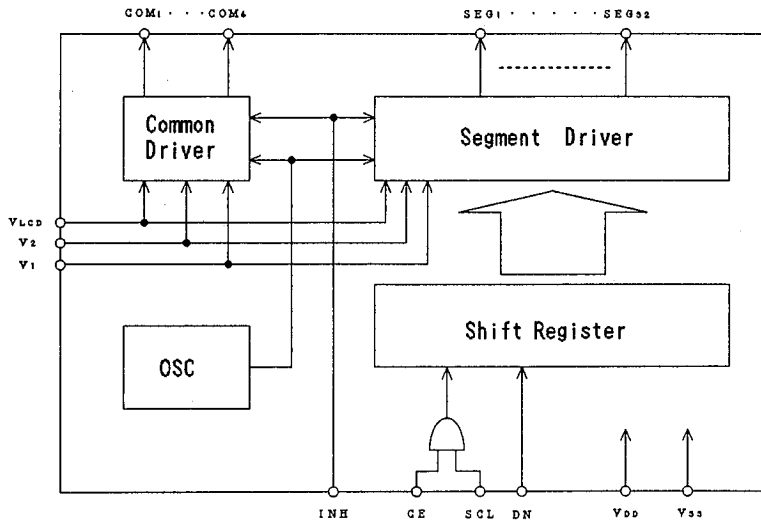
The rectangle outline is useful the COG applications.

■ PACKAGE OUTLINE

■ FEATURES

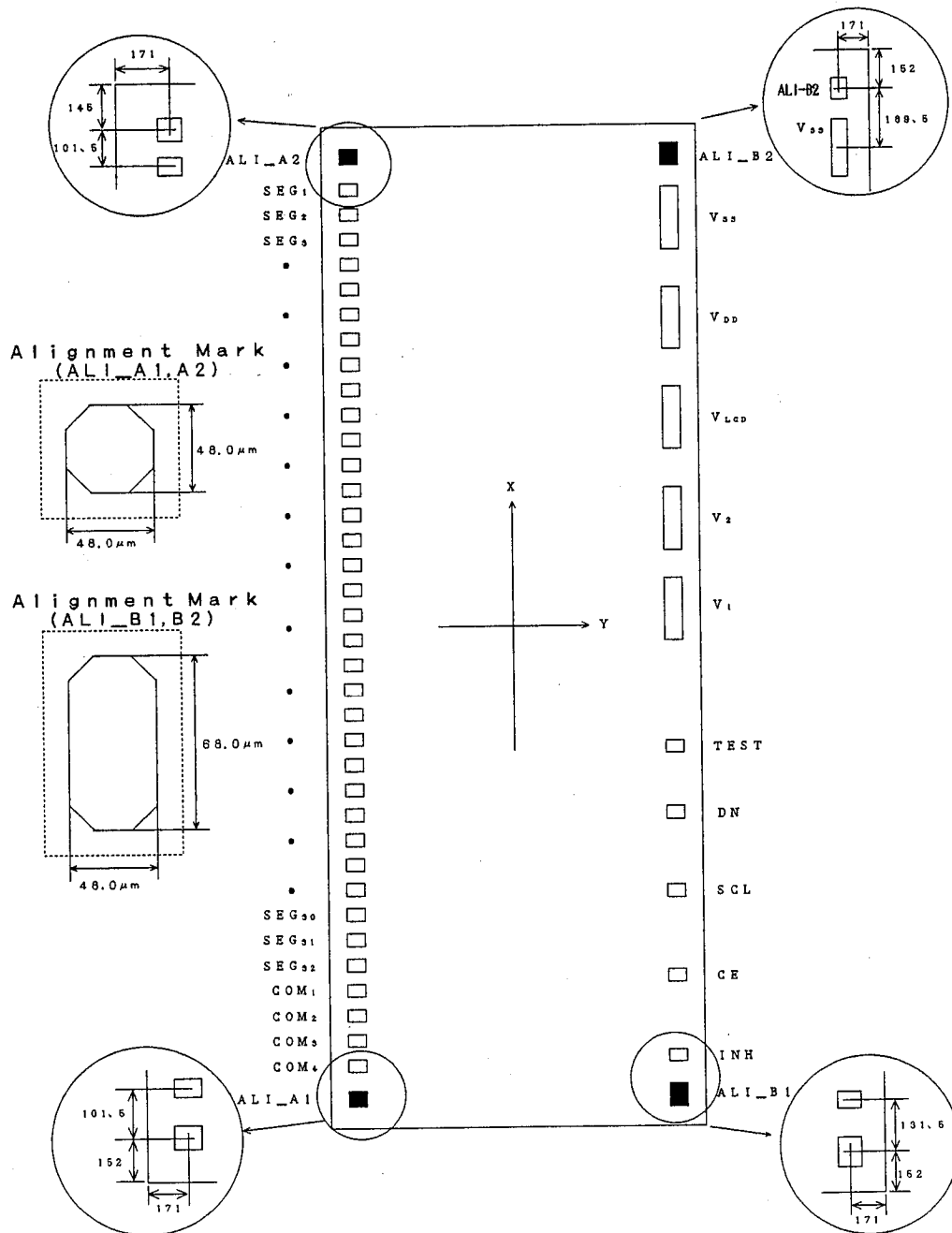
- 32 Segment Drivers
- Duty and Bias Ratio : 1/4Duty, 1/3Bias(up to 128 segments)
- Serial Data Transmission (Shift Clock 2MHz max.)
- Oscillation Circuit On-chip
- Display Off Function (INH Terminal)
- Operating Voltage --- 2.4~3.6V
- LCD Driving Voltage --- 6.0V Max.
- Package Outline --- Chip / Bumped Chip
- C-MOS Technology

NJU6437C

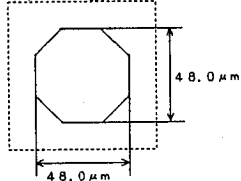
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■ BLOCK DIAGRAM


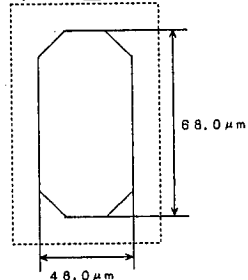
■ PAD LOCATION



Alignment Mark (ALI_A1,A2)



Alignment Mark (ALI_B1,B2)



- Chip size : 4.0mm x 1.5mm
- Chip center : X=0 μm, Y=0 μm
- Chip thickness : 400±30 μm
- Pad size : 50 μm x 70 μm
- V₁, V₂, V_{LCD}, V_{DD}, V_{SS} Terminal is 250 μm x 70 μm
- Bump height : 25 μm TYP.
- Bump material : Au

■ : 4th Mark is the Alignment Mark.
The Alignment Mark is useful the COG Assembly.

■ PAD COORDINATES

 Chip Size 4.0x1.5mm(Chip Center X=0 μ m, Y=0 μ m)

No	PAD NAME	X=(μ m)	Y=(μ m)	No	PAD NAME	X=(μ m)	Y=(μ m)
1	INH	-1716.5	-575.0	26	SEG _{1,6}	253.5	579.0
2	CE	-1406.5	-575.0	27	SEG _{1,7}	153.5	579.0
3	SCL	-1076.5	-575.0	28	SEG _{1,8}	53.5	579.0
4	DN	-766.5	-575.0	29	SEG _{1,9}	-46.5	579.0
5	TEST	-485.0	-575.0	30	SEG _{2,0}	-146.5	579.0
6	V ₁	100.0	-575.0	31	SEG _{2,1}	-246.5	579.0
7	V ₂	458.5	-575.0	32	SEG _{2,2}	-346.5	579.0
8	V _{LCD}	858.5	-575.0	33	SEG _{2,3}	-446.5	579.0
9	V _{DD}	1258.5	-575.0	34	SEG _{2,4}	-546.5	579.0
10	V _{SS}	1658.5	-575.0	35	SEG _{2,5}	-646.5	579.0
11	SEG ₁	1753.5	579.0	36	SEG _{2,6}	-746.5	579.0
12	SEG ₂	1653.5	579.0	37	SEG _{2,7}	-846.5	579.0
13	SEG ₃	1553.5	579.0	38	SEG _{2,8}	-946.5	579.0
14	SEG ₄	1453.5	579.0	39	SEG _{2,9}	-1046.5	579.0
15	SEG ₅	1353.5	579.0	40	SEG _{3,0}	-1146.5	579.0
16	SEG ₆	1253.5	579.0	41	SEG _{3,1}	-1246.5	579.0
17	SEG ₇	1153.5	579.0	42	SEG _{3,2}	-1346.5	579.0
18	SEG ₈	1053.5	579.0	43	COM ₁	-1446.5	579.0
19	SEG ₉	953.5	579.0	44	COM ₂	-1546.5	579.0
20	SEG _{1,0}	853.5	579.0	45	COM ₃	-1646.5	579.0
21	SEG _{1,1}	753.5	579.0	46	COM ₄	-1746.5	579.0
22	SEG _{1,2}	653.5	579.0	ALIGNMENT	ALI_A1	-1848.0	579.0
23	SEG _{1,3}	553.5	579.0	ALIGNMENT	ALI_A2	1855.0	579.0
24	SEG _{1,4}	453.5	579.0	ALIGNMENT	ALI_B1	-1848.0	-579.0
25	SEG _{1,5}	353.5	579.0	ALIGNMENT	ALI_B2	1848.0	-579.0

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■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N
1	INH	Display-Off Control Terminal : When display goes to off, the before display Off data in the shift-register is retained. "H" : Display-Off "L" : Display-On
2	CE	Chip Enable Signal Input Terminal : "H" : LCD display data "L" : Disable
3	SCL	Serial Data Transmission Clock Input Terminal : LCD display data are input synchronized SCL clock signal rise edge.
4	DN	Serial Data Input Terminal Data input timing : SCL clock rise edge
6	V ₁	LCD Driving Voltage Adjust Terminal
7	V ₂	LCD Driving Voltage Adjust Terminal
8	V _{LCD}	Power Supply for LCD Driving
9	V _{DD}	Power Supply (+3V)
10	V _{SS}	Power Supply (0V)
11~42	SEG ₁ ~ SEG ₃₂	LCD Segment Output Terminals
43~46	COM ₁ ~ COM ₄	LCD Common Output Terminals

■ FUNCTIONAL DESCRIPTION

(1) Operation of each block

(1-1) Oscillation Circuit :

This circuits supply the basical clock signal to other circuits like as common driver and segment driver.

(1-2) Shift-Register

When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.

(1-3) Common Divider Circuit

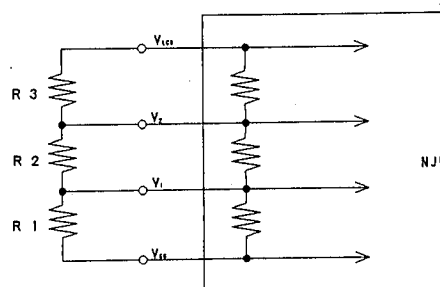
This circuit divides the oscillating signal to generate the common timing.

(1-4) Segment Divider Circuit

This circuit divides the oscillating signal to generate the segment timing.

(1-5) The LCD Driving Voltage Adjust circuit

The incorporated Bleeder Resistance sets 1/3 bias, and LCD Driver ability can be increased by connecting external resistance.



(2) Display Data input timing, correspond to segment and common terminal

When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.

When the power is turned on, whole data in the shift-register are "L".

- ※ Whole 128bits data transfer to the shift register. When the input data is less than 128 bits, parts which bit data is inputted corresponded to display, and segment which correspond to the rest part in "off".

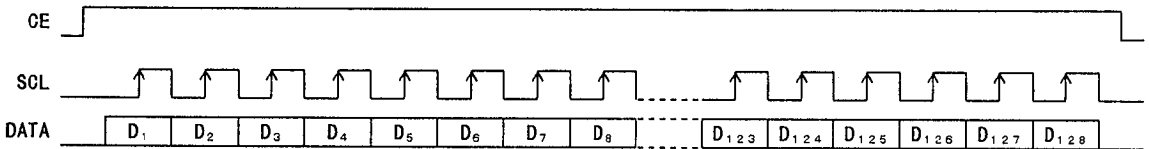
In case of over then 128bits, front 128bits from fall edge of "CE" signal is valid.

- Input data correspond to Segment Status

The "H" input data correspond to segment "ON" and "L" correspond to "OFF".

Data (D1...D128)	Segment Status
"H"	ON
"L"	OFF

- Display Data Correspond to Segment Status



(2-3) Display Data Correspond to Segment and Common Terminals

Segment	Data	COM ₁	COM ₂	COM ₃	COM ₄
SEG ₁	D ₁ D ₂ D ₃ D ₄	○	○	○	○
SEG ₂	D ₅ D ₆ D ₇ D ₈	○	○	○	○
⋮	⋮	⋮	⋮	⋮	⋮
SEG ₃₁	D ₁₂₁ D ₁₂₂ D ₁₂₃ D ₁₂₄	○	○	○	○
SEG ₃₂	D ₁₂₅ D ₁₂₆ D ₁₂₇ D ₁₂₈	○	○	○	○

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Operating Voltage (1)	V _{DD}	-0.3 ~ +7.0	V
Operating Voltage (2)	V _{LCD}	-0.3 ~ +7.0	V
Operating Voltage (3)	V ₁ , V ₂	-0.3 ~ +7.0	V
Input Voltage	V _{IN}	-0.3 ~ VDD	V
Operating Temperature	T _{OPR}	-20 ~ +75	°C
Storage Temperature	T _{STG}	-55 ~ +125	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0 V

Note 3) The relation: V_{LCD} ≥ V₂ ≥ V₁ ≥ V_{SS} must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation.

■ ELECTRICAL CHARACTERISTICS

- DC Characteristics

 (Ta=25°C, V_{DD}=3.0~5.0V, V_{SS}=0V, V_{LCD}=6.0V)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Operating Voltage (1)	Recommend	V _{DD}	V _{DD} Terminal	2.4	3.0	3.6	V	
	Available	V _{DD}	V _{DD} Terminal	2.4	3.0	5.5	V	
Operating Voltage (2)		V _{LCD}	V _{LCD} Terminal	2.0		6.0	V	
Operating Voltage (3)		V ₂	V ₂ Terminal	2.0	2/3V _{LCD}	V _{LCD}	V	
Operating Voltage (4)		V ₁	V ₁ Terminal	0.7	1/3V _{LCD}	V ₂	V	
"H" Input Voltage		V _{IH}	CE, SCL, DN, INH Terminals	0.7V _{DD}		V _{DD}	V	
"L" Input Voltage		V _{IL}	CE, SCL, DN, INH Terminals	V _{SS}		0.3V _{DD}	V	
"H" Input Current		I _{IH}	CE, SCL, DN, INH Term., V _{IN} =V _{DD}			5	μA	
"L" Input Current		I _{IL}	CE, SCL, DN, INH Term., V _{IN} =V _{SS}			5	μA	
"H" Output Voltage (1)		V _{OH(1)}	SEG ₁ ~SEG ₃₂ Term., I _O =-1μA	V _{LCD} -0.6			V	5
"L" Output Voltage (1)		V _{OL(1)}	SEG ₁ ~SEG ₃₂ Term., I _O =1μA			V _{DD} +0.6	V	5
Middle Level Voltage 1/3 (1)		V _{MS1/3}	SEG ₁ ~SEG ₃₂ Term., I _O =±1μA	1/3V _{LCD} -0.6	1/3V _{LCD}	1/3V _{LCD} +0.6	V	5
Middle Level Voltage 2/3 (1)		V _{MS2/3}	SEG ₁ ~SEG ₃₂ Term., I _O =±1μA	2/3V _{LCD} -0.6	2/3V _{LCD}	2/3V _{LCD} +0.6	V	5
"H" Output Voltage (2)		V _{OH(2)}	COM ₁ ~COM ₄ Term., I _O =-30μA	V _{LCD} -0.6			V	6
"L" Output Voltage (2)		V _{OL(2)}	COM ₁ ~COM ₄ Term., I _O =30μA			V _{SS} +0.6	V	6
Middle Level Voltage 1/3 (2)		V _{MC1/3}	COM ₁ ~COM ₄ Term., I _O =±1μA	1/3V _{LCD} -0.6	1/3V _{LCD}	1/3V _{LCD} +0.6	V	6
Middle Level Voltage 2/3 (2)		V _{MC2/3}	COM ₁ ~COM ₄ Term., I _O =±1μA	2/3V _{LCD} -0.6	2/3V _{LCD}	2/3V _{LCD} +0.6	V	6
Operating Current (1)		I _{SS}	V _{DD} Terminal	V _{DD} =5.0V V _{LCD} OPEN	16	30	μA	
				V _{DD} =3.0V V _{LCD} OPEN	7.5	10		
Operating Current (2)		I _{LCD}	V _{LCD} Terminal	V _{DD} =3.0V V _{LCD} =6.0V		12	μA	
Hysteresis Voltage		V _H	CE, SCL, DN, INH Terminal	V _{DD} =5.0V	0.3	0.6	V	
				V _{DD} =3.0V	0.3	1.0		

(Note 5) Segment terminals are open.

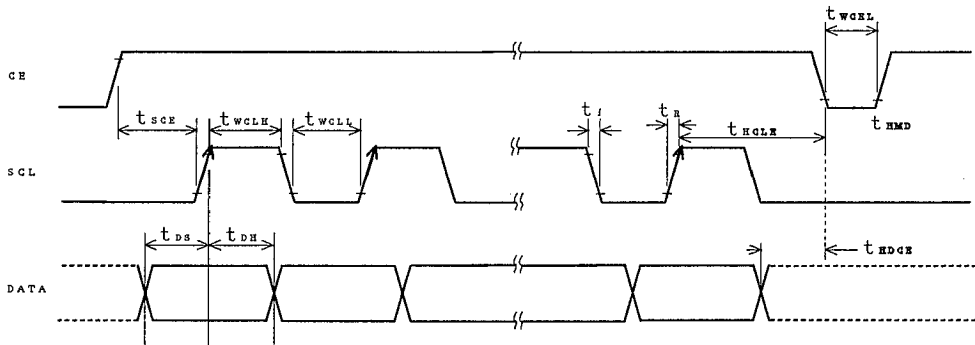
(Note 6) Common terminals are open.

• AC Characteristics

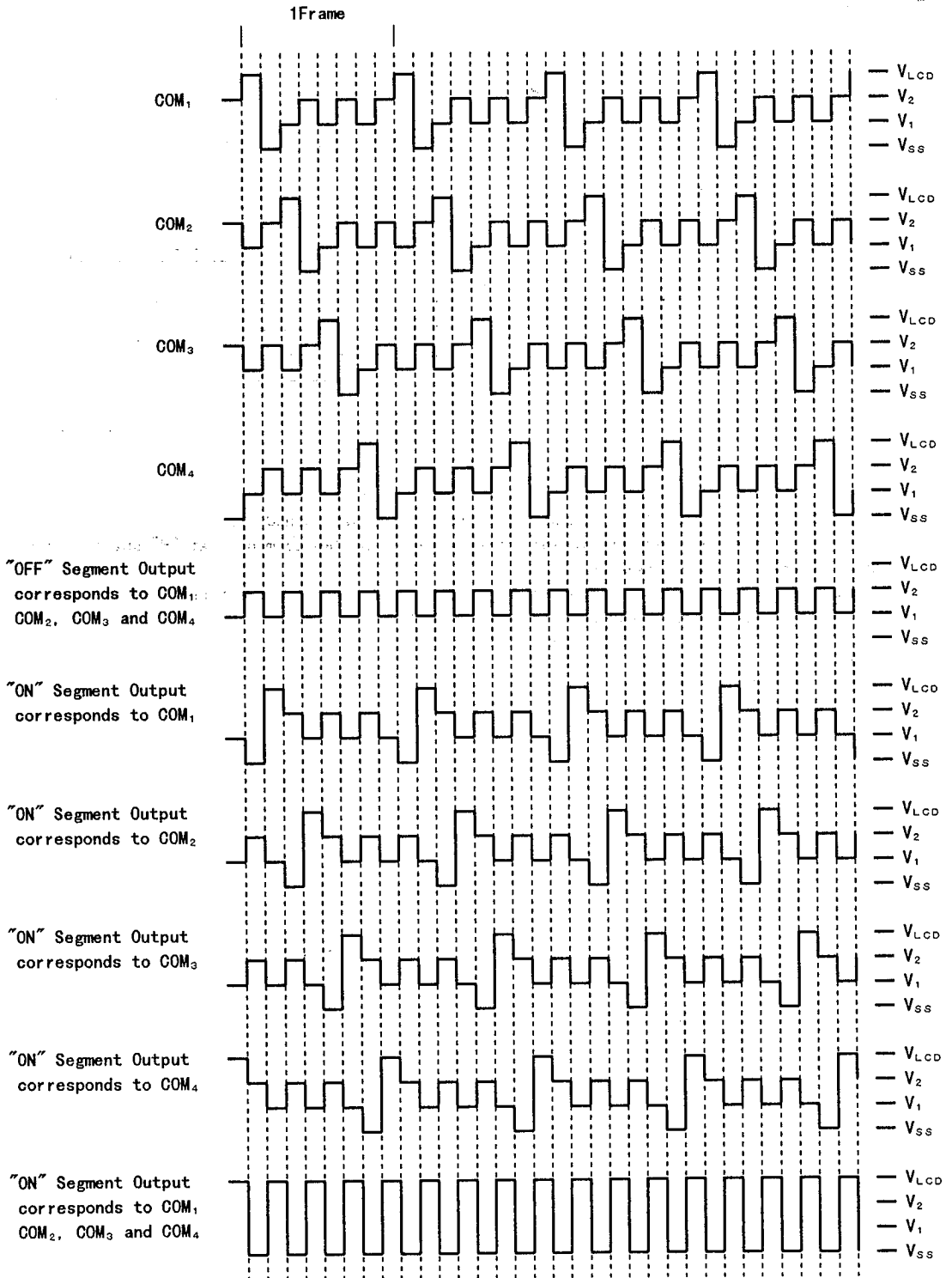
 (Ta=25°C, V_{DD}=3.0V, V_{SS}=0V, V_{LCD}=6.0V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
"L" Clock Pulse Width	t _{WCLL}	SCL	0.25	—	—	μs	
"H" Clock Pulse Width	t _{WCLH}	SCL	0.25	—	—	μs	
SCL Rise time, Fall time	t _r , t _f	SCL	—	—	50	ns	
Data Set-up Time	t _{DS}	DN, SCL	0.25	—	—	μs	
Data Hold Time	t _{DH}	SCL	0.25	—	—	μs	
CE Set-up Time	t _{SCE}	CE, DN	1.25	—	—	μs	
CE Hold Time	t _{HOLE}	SCL, CE	1.00	—	—	μs	
"L" CE Pulse Width	t _{WCEL}	CE	4.00	—	—	μs	
Frame Frequency	f _O	COM ₁ ~ COM ₄ ,	V _{DD} =5.0V	45	75	—	Hz
		SEG ₁ ~ SEG ₃₂	V _{DD} =3.0V	45	70	—	

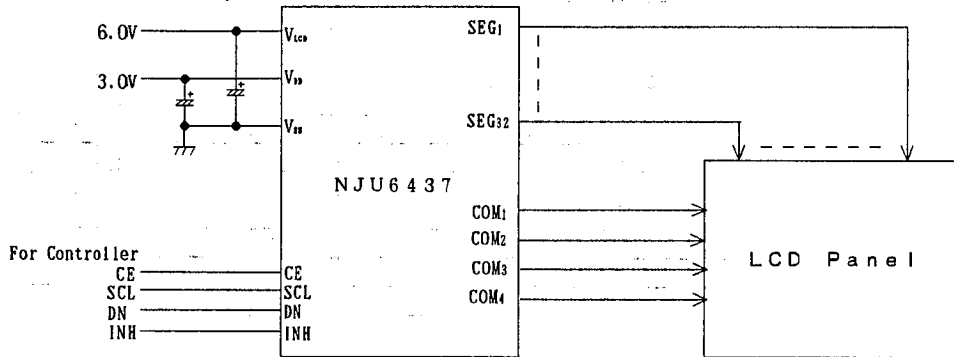
• Input Timing Characteristics



■ LCD Driving Waveform(1/4DUTY · 1/3BIAS)



■ APPLICATION CIRCUIT



(Note) The internal display data is undefined when V_{DD} is just turned on.

To avoid the meaningless display, please keep the INH terminal at "H" until proper display data has been transferred.

In order to set the initial condition, 128-bit blank data or the first 128-bit data to be displayed should be transferred.

MEMO

[CAUTION]

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