TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC74VHC20F, TC74VHC20FN, TC74VHC20FT

## DUAL 4-INPUT NAND GATE

(Note) The JEDEC SOP (FN) is not available in Japan.

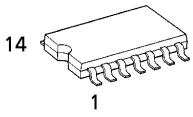
The TC74VHC20 is an advanced high speed CMOS 4-INPUT NAND GATE fabricated with silicon gate $C^2MOS$ technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including a buffer output, which provide high noise immunity and stable output.

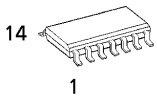
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

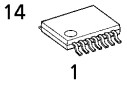
- High Speed····· $t_{pd}$ = 3.3ns(typ.) at $V_{CC}$ = 5V
- Low Power Dissipation····· $I_{CC}$ = 2$\mu$A(Max.) at Ta = 25°C
- High Noise Immunity····· $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$ (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range···· $V_{CC}$ (opr) = 2V~5.5V
- Pin and Function Compatible with 74ALS20




F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)

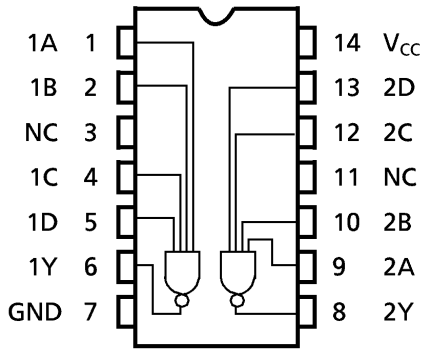



FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)



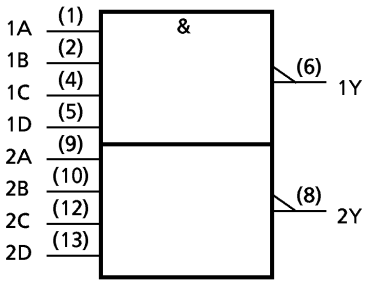

FT (TSSOP14-P-0044-0.65)
Weight : 0.06g (Typ.)

### PIN ASSIGNMENT




(TOP VIEW)

### IEC LOGIC SYMBOL




### TRUTH TABLE

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| A | B | C | D | Y |
| L | X | X | X | H |
| X | L | X | X | H |
| X | X | L | X | H |
| X | X | X | L | H |
| H | H | H | H | L |

X : Don't Care

961001EBA2

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Supply Voltage Range | $V_{CC}$ | −0.5~7.0 | V |
| DC Input Voltage | $V_{IN}$ | −0.5~7.0 | V |
| DC Output Voltage | $V_{OUT}$ | −0.5~$V_{CC}$ + 0.5 | V |
| Input Diode Current | $I_{IK}$ | −20 | mA |
| Output Diode Current | $I_{OK}$ | ±20 | mA |
| DC Output Current | $I_{OUT}$ | ±25 | mA |
| DC $V_{CC}$/Ground Current | $I_{CC}$ | ±50 | mA |
| Power Dissipation | $P_D$ | 180 | mW |
| Storage Temperature | $T_{stg}$ | −65~150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 2.0~5.5 | V |
| Input Voltage | $V_{IN}$ | 0~5.5 | V |
| Output Voltage | $V_{OUT}$ | 0~$V_{CC}$ | V |
| Operating Temperature | $T_{opr}$ | −40~85 | °C |
| Input Rise and Fall Time | dt / dv | 0~100 ($V_{CC}$ = 3.3 ± 0.3V)<br>0~20 ($V_{CC}$ = 5 ± 0.5V) | ns / V |

## DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | | $V_{CC}$ (V) | Ta = 25°C MIN. | Ta = 25°C TYP. | Ta = 25°C MAX. | Ta = −40~85°C MIN. | Ta = −40~85°C MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| High - Level Input Voltage | $V_{IH}$ | | | 2.0 | 1.50 | — | — | 1.50 | — | V |
| | | | | 3.0~5.5 | $V_{CC}$ × 0.7 | — | — | $V_{CC}$ × 0.7 | — | |
| Low - Level Input Voltage | $V_{IL}$ | | | 2.0 | — | — | 0.50 | — | 0.50 | V |
| | | | | 3.0~5.5 | — | — | $V_{CC}$ × 0.3 | — | $V_{CC}$ × 0.3 | |
| High - Level Output Voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −50μA | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | 3.0 | 2.9 | 3.0 | — | 2.9 | — | |
| | | | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | |
| | | | $I_{OH}$ = −4mA | 3.0 | 2.58 | — | — | 2.48 | — | |
| | | | $I_{OH}$ = −8mA | 4.5 | 3.94 | — | — | 3.80 | — | |
| Low - Level Output Voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ | $I_{OL}$ = 50μA | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | 3.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | $I_{OL}$ = 4mA | 3.0 | — | — | 0.36 | — | 0.44 | |
| | | | $I_{OL}$ = 8mA | 4.5 | — | — | 0.36 | — | 0.44 | |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$ = 5.5V or GND | | 0~5.5 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent Supply Current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | 2.0 | — | 20.0 | |

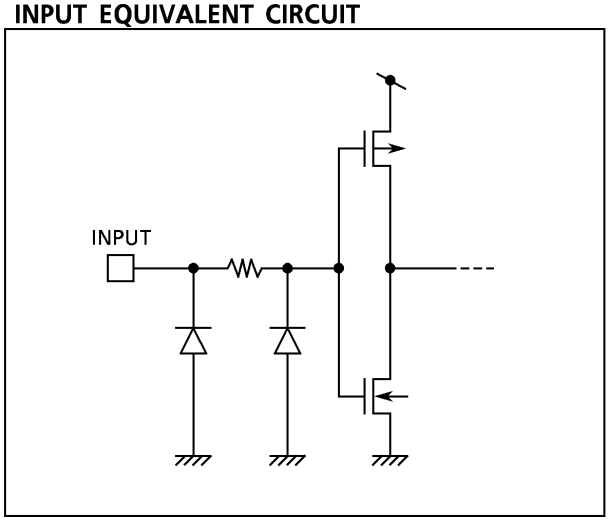
**AC ELECTRICAL CHARACTERISTICS ( Input $t_r = t_f = 3ns$ )**

| PARAMETER | SYMBOL | TEST CONDITION | | | Ta = 25°C | | | Ta = −40~85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | CL (pF) | MIN. | TYP. | MAX. | MIN. | MAX. | |
| Propagation Delay Time | $t_{pLH}$ $t_{pHL}$ | | 3.3 ± 0.3 | 15 | − | 4.6 | 6.6 | 1.0 | 8.0 | ns |
| | | | | 50 | − | 7.1 | 10.1 | 1.0 | 11.5 | |
| | | | 5.0 ± 0.5 | 15 | − | 3.3 | 5.0 | 1.0 | 6.0 | |
| | | | | 50 | − | 4.8 | 7.0 | 1.0 | 8.0 | |
| Input Capacitance | $C_{IN}$ | | | | − | 4 | 10 | − | 10 | pF |
| Power Dissipation Capacitance | $C_{PD}$ | (Note 1) | | | − | 19 | − | − | − | |

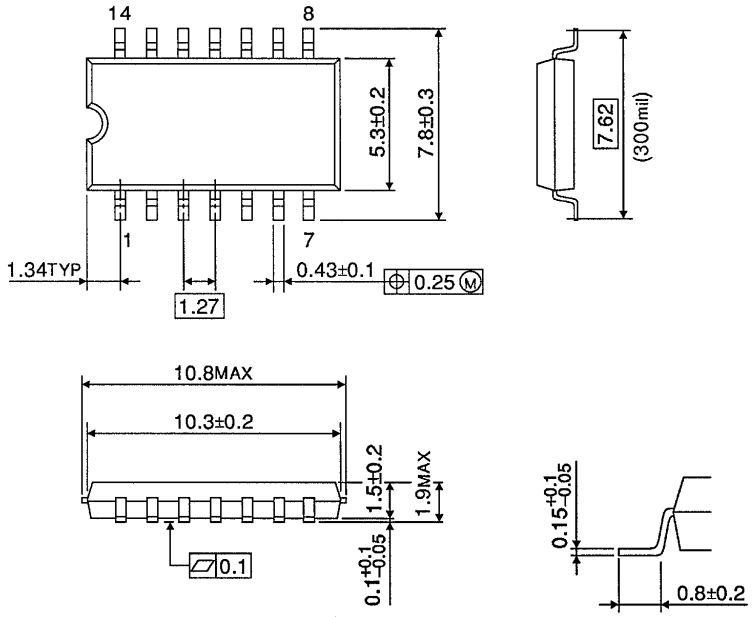
Note (1) $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

$$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ ( per Gate )}$$

**INPUT EQUIVALENT CIRCUIT**



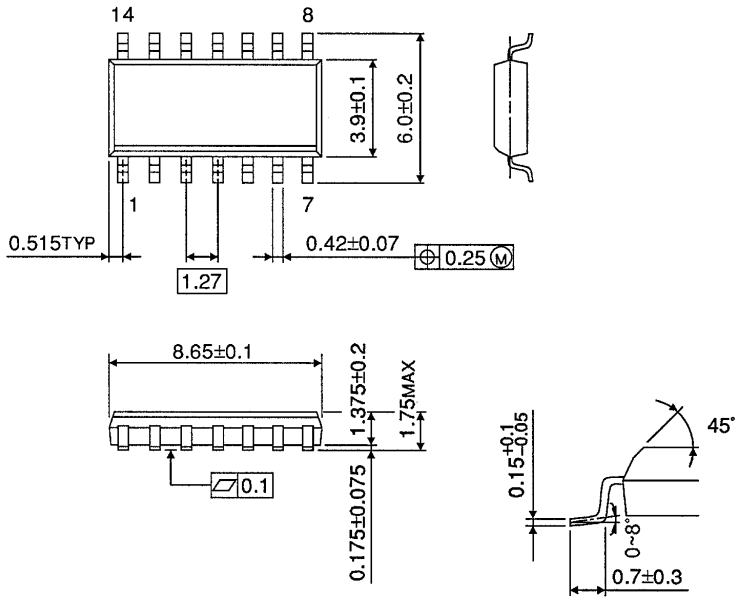
**SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27)** Unit in mm




Weight : 0.18g (Typ.)

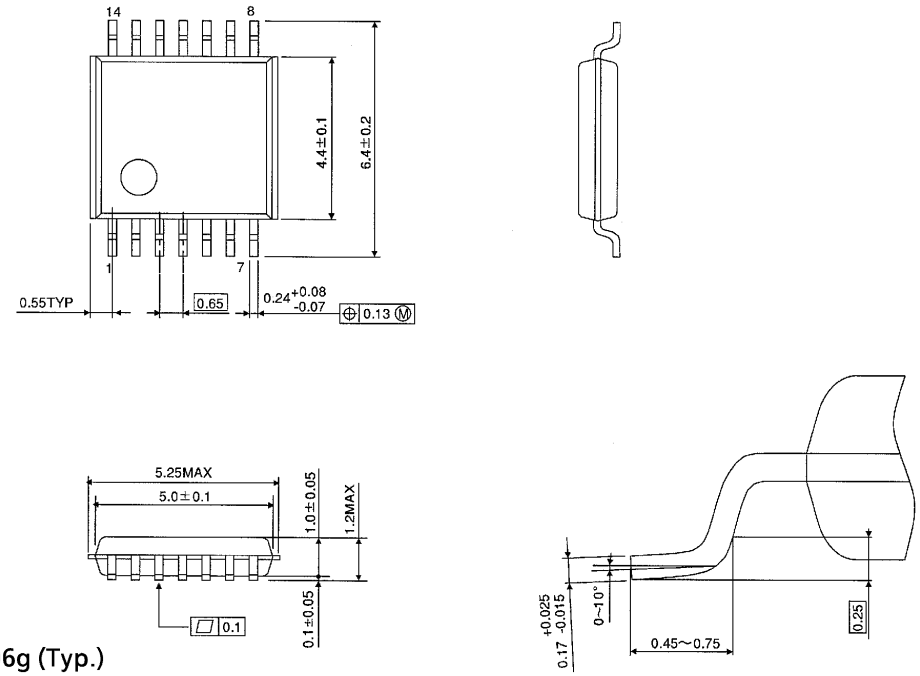
**SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150-1.27)** Unit in mm

(Note) This package is not available in Japan.




Weight : 0.12g (Typ.)

**TSSOP 14PIN OUTLINE DRAWING (TSSOP14-P-0044-0.65)** Unit in mm




Weight : 0.06g (Typ.)