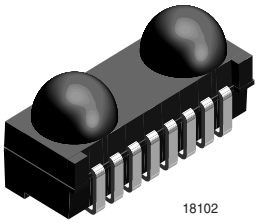
# Fast Infrared Transceiver Module (FIR, 4 Mbit/s) for 2.7 V to 5.5 V Operation

## Description

The TFDU6102 is a low-power infrared transceiver module compliant to the latest IrDA physical layer standard for fast infrared data communication, supporting IrDA speeds up to 4.0 Mbit/s (FIR), and carrier based remote control modes up to 2 MHz. Integrated within the transceiver module are a PIN photodiode, an infrared emitter (IRED), and a low-power CMOS control IC to provide a total front-end solution in a single package.




Vishay FIR transceivers are available in different package options, including this BabyFace package (TFDU6102). This wide selection provides flexibility for a variety of applications and space constraints. The transceivers are capable of directly interfacing with a wide variety of I/O devices which perform the modulation/ demodulation function, including National Semiconductor's PC87338, PC87108 and PC87109, SMC's FDC37C669, FDC37N769 and CAM35C44, and Hitachi's SH3. TFDU6102 has a tri-state output and is floating in shut-down mode with a weak pull-up.

## Features

- Supply voltage 2.7 V to 5.5 V, Operating idle current (receive mode) < 3 mA, Shutdown current < 5 µA over full temperature range
- Surface Mount Package, top and side view, 9.7 mm x 4.7 mm x 4.0 mm
- Operating Temperature - 25 °C to 85 °C
- Storage Temperature - 40 °C to 100 °C
- Transmitter Wavelength typ. 886 nm, supporting IrDA® and Remote Control
- IrDA® compliant, link distance > 1 m, ± 15 °, window losses are allowed to still be inside the IrDA® spec.
- Remote Control Range > 8 m, typ. 22 m
- ESD > 4000 V (HBM), Latchup > 200 mA
- EMI immunity > 550 V/m for GSM frequency and other mobile telephone bands / (700 MHz to 2000 MHz, no external shield)
- Split power supply, LED can be driven by a separate power supply not loading the regulated supply. U.S. Pat. No. 6,157,476
- Tri-state-Receiver Output, floating in shut down with a weak pull-up
- Eye safety class 1 (IEC60825-1, ed. 2001), limited LED on-time, LED current is controlled, no single fault to be considered

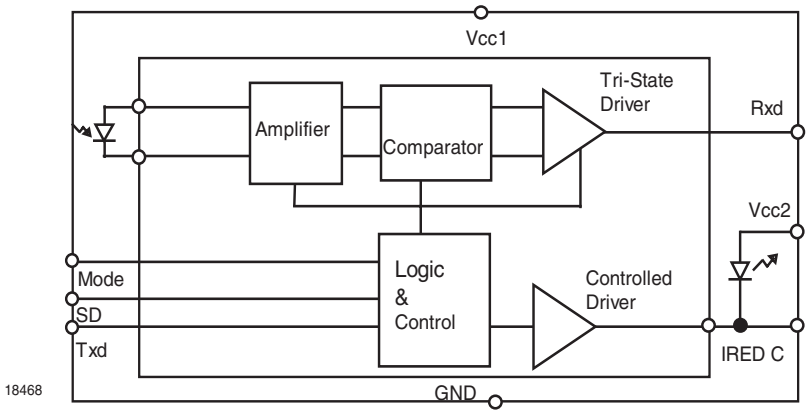
## Applications

- Notebook Computers, Desktop PCs, Palmtop Computers (Win CE, Palm PC), PDAs
- Digital Still and Video Cameras
- Printers, Fax Machines, Photocopiers, Screen Projectors
- Telecommunication Products (Cellular Phones, Pagers)
- Internet TV Boxes, Video Conferencing Systems
- External Infrared Adapters (Dongles)
- Medical and Industrial Data Collection

## Parts Table

| Part | Description | Qty / Reel |
|---|---|---|
| TFDU6102-TR3 | Oriented in carrier tape for side view surface mounting | 1000 pcs |
| TFDU6102-TT3 | Oriented in carrier tape for top view surface mounting | 1000 pcs |

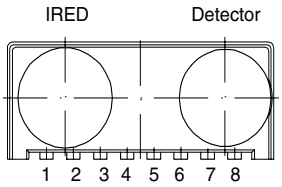
## Functional Block Diagram




## Pinout

TFDU6102
weight 200 mg

**"U" Option BabyFace (Universal)**




### Definitions:

In the Vishay transceiver data sheets the following nomenclature is used for defining the IrDA operating modes:

SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhy 1.0

MIR: 576 kbit/s to 1152 kbit/s
FIR: 4 Mbit/s
VFIR: 16 Mbit/s

MIR and FIR were implemented with IrPhy 1.1, followed by IrPhy 1.2, adding the SIR Low Power Standard. IrPhy 1.3 extended the Low Power Option to MIR and FIR and VFIR was added with IrPhy 1.4.A new version of the standard in any case obsoletes the former version.

## Pin Description

| Pin Number "U" | Function | Description | I/O | Active |
|---|---|---|---|---|
| 1 | $V_{CC2}$ IRED Anode | Connect IRED anode directly to $V_{CC2}$. For voltages higher than 3.6 V an external resistor might be necessary for reducing the internal power dissipation. An unregulated separate power supply can be used at this pin. | | |
| 2 | IRED Cathode | IRED cathode, internally connected to driver transistor | | |
| 3 | Txd | This input is used to transmit serial data when SD is low. An on-chip protection circuit disables the LED driver if the Txd pin is asserted for longer than 80 µs. When used in conjunction with the SD pin, this pin is also used to receiver speed mode. | I | HIGH |
| 4 | Rxd | Received Data Output, push-pull CMOS driver output capable of driving a standard CMOS or TTL load. No external pull-up or pull-down resistor is required. **Floating with a weak pull-up of 500 kΩ (typ.) in shutdown mode.** | O | LOW |
| 5 | SD | Shutdown, also used for dynamic mode switching. Setting this pin active places the module into shutdown mode. On the falling edge of this signal, the state of the Txd pin is sampled and used to set receiver low bandwidth (Txd = Low, SIR) or high bandwidth (Txd = High, MIR and FIR) mode. Will be overwritten by the mode pin input, which must float, when dynamic programming is used. | I | HIGH |
| 6 | $V_{CC1}$ | Supply Voltage | | |
| 7 | Mode | HIGH: High speed mode, MIR and FIR; LOW: Low speed mode, SIR only (see chapter "Mode Switching"). Must float, when dynamic programming is used. | I | |
| | Mode | The mode pin can also be used to indicate the dynamically programmed mode. The maximum load is limited to 50 pF. High indicates FIR/MIR-, low indicates SIR-mode | O | |
| 8 | GND | Ground | | |

## Absolute Maximum Ratings

Reference point Ground Pin 8, unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

| Parameter | Test Conditions | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage range, transceiver | 0 V < $V_{CC2}$ < 6 V | $V_{CC1}$ | - 0.5 | | + 6 | V |
| Supply voltage range, transmitter | 0 V < $V_{CC1}$ < 6 V | $V_{CC2}$ | - 0.5 | | + 6.5 | V |
| Input currents | for all pins, except IRED anode pin | | | | 10 | mA |
| Output sinking current | | | | | 25 | mA |
| Power dissipation | see derating curve, figure 5 | $P_D$ | | | 500 | mW |
| Junction temperature | | $T_J$ | | | 125 | °C |
| Ambient temperature range (operating) | | $T_{amb}$ | - 25 | | + 85 | °C |
| Storage temperature range | | $T_{stg}$ | - 25 | | + 85 | °C |
| Soldering temperature | see recommended solder profile (see figure 4) | | | | 240 | °C |
| Average output current | | $I_{IRED}$ (DC) | | | 125 | mA |
| Repetitive pulse output current | < 90 µs, $t_{on}$ < 20 % | $I_{IRED}$ (RP) | | | 600 | mA |
| IRED anode voltage | | $V_{IREDA}$ | - 0.5 | | + 6.5 | V |
| Voltage at all inputs and outputs | $V_{in}$ > $V_{CC1}$ is allowed | $V_{IN}$ | | | 5.5 | V |
| Load at mode pin when used as mode indicator | | | | | 50 | pF |

## Eye safety information

Reference point Pin: GND unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

| Parameter | Test Conditions | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Virtual source size | Method: (1 - 1/e) encircled energy | d | 2.5 | 2.8 | | mm |
| Maximum Intensity for Class 1 | IEC60825-1 or EN60825-1, edition Jan. 2001 | $I_e$ | | | *) (500)**) | mW/sr |

*)Due to the internal limitation measures the device is a "class1" device

**)IrDA specifies the max. intensity with 500 mW/sr

## Electrical Characteristics

### Transceiver

$T_{amb}$ = 25 °C, $V_{CC}$ = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

| Parameter | Test Conditions | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 2.7 | | 5.5 | V |
| Supply current (Idle) [1] | SD = Low, $E_e$ = 0 klx | $I_{CC}$ | | 2 | 3 | mA |
| Supply current (Idle)[1] | SD = Low, $E_e$ = 1 klx[2] | $I_{CC}$ | | 2 | 3 | mA |
| Shutdown supply current | SD = High, Mode = Floating $E_e$ = 0 klx | $I_{SD}$ | | | 2.0 | µA |
| | SD = High, Mode = Floating $E_e$ = 1 klx[2] | $I_{SD}$ | | | 2.5 | µA |
| | SD = High, T = 85 °C, Mode = Floating, not ambient light sensitive | $I_{SD}$ | | | 5 | µA |
| Operating temperature range | | $T_A$ | - 25 | | + 85 | °C |
| Output voltage low | $I_{OL}$ = 1 mA, $C_{load}$ = 15 pF | $V_{OL}$ | | | 0.4 | V |
| Output voltage high | $I_{OH}$ = 500 µA, $C_{load}$ = 15 pF | $V_{OH}$ | 0.8 x $V_{CC}$ | | | V |
| | $I_{OH}$ = 250 µA, $C_{load}$ = 15 pF | $V_{OH}$ | 0.9 x $V_{CC}$ | | | V |
| Output Rxd current limitation high state | Short to Ground | | | | 20 | mA |
| Output Rxd current limitation low state | Short to $V_{CC1}$ | | | | 20 | mA |
| Rxd to $V_{CC1}$ impedance | SD = High | $R_{Rxd}$ | 400 | 500 | 600 | kΩ |
| Input voltage low (Txd, SD, Mode) | | $V_{IL}$ | - 0.5 | | 0.5 | V |
| Input voltage high (Txd, SD, Mode) | CMOS level [3] | $V_{IH}$ | $V_{CC}$ - 0.5 | | $V_{CC}$ + 0.5 | V |
| | TTL level, $V_{CC1}$ = 4.5 V | $V_{IH}$ | 2.4 | | | V |
| Input leakage current (Txd, SD) | | $I_L$ | - 10 | | + 10 | µA |
| Input leakage current Mode | | $I_{ICH}$ | - 2 | | + 2 | µA |
| Input capacitance (Txd, SD, Mode) | | $C_{IN}$ | | | 5 | pF |

[1] Receive mode only.
In transmit mode, add additional 85 mA (typ) for IRED current. Add Rxd output current depending on Rxd load.

[2] Standard Illuminant A

[3] The typical threshold level is between 0.5 x $V_{CC2}$ ($V_{CC}$ = 3 V) and 0.4 x $V_{CC}$ ($V_{CC}$ = 5.5 V) . It is recommended to use the specified min/ max values to avoid increased operating current.

## Optoelectronic Characteristics

### Receiver

$T_{amb}$ = 25 °C, $V_{CC}$ = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

| Parameter | Test Conditions | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Minimum detection threshold irradiance, SIR mode | 9.6 kbit/s to 115.2 kbit/s<br>λ = 850 nm to 900 nm | $E_e$ | | 25<br>(2.5) | 35<br>(3.5) | mW/m² (µW/cm²) |
| Minimum detection threshold irradiance, MIR mode | 1.152 Mbit/s<br>λ = 850 nm to 900 nm | $E_e$ | | 65<br>(6.5) | | mW/m² (µW/cm²) |
| Minimum detection threshold irradiance, FIR mode | 4.0 Mbit/s<br>λ = 850 nm to 900 nm | $E_e$ | | 80<br>(8.0) | 90<br>(9.0) | mW/m² (µW/cm²) |
| Maximum detection threshold irradiance | λ = 850 nm to 900 nm | $E_e$ | | 5<br>(500) | | kW/m² (mW/cm²) |
| No detection receiver input irradiance | *) | $E_e$ | 4<br>(0.4) | | | mW/m² (µW/cm²) |
| Rise time of output signal | 10 % to 90 %, 15 pF | $t_{r\ (Rxd)}$ | 10 | | 40 | ns |
| Fall time of output signal | 90 % to 10 %, 15 pF | $t_{f\ (Rxd)}$ | 10 | | 40 | ns |
| Rxd pulse width of output signal, 50 %, SIR mode | input pulse length<br>1.4 µs < $P_{Wopt}$ < 25 µs | $t_{PW}$ | | 2.1 | | µs |
| | input pulse length<br>1.4 µs < $P_{Wopt}$ < 25 µs,<br>- 25 °C < T < 85 °C **) | $t_{PW}$ | 1.5 | 1.8 | 2.6 | µs |
| Rxd pulse width of output signal, 50 %, MIR mode | input pulse length<br>$P_{Wopt}$ = 217 ns,<br>1.152 Mbit/s | $t_{PW}$ | 110 | 250 | 270 | ns |
| Rxd pulse width of output signal, 50 %, FIR mode | input pulse length<br>$P_{Wopt}$ = 125 ns,<br>4.0 Mbit/s | $t_{PW}$ | 100 | | 140 | ns |
| | input pulse length<br>$P_{Wopt}$ = 250 ns,<br>4.0 Mbit/s | $t_{PW}$ | 225 | | 275 | ns |
| Stochastic jitter, leading edge | input irradiance = 100 mW/m², 4.0 Mbit/s | | | | 20 | ns |
| | input irradiance = 100 mW/m², 1.152 Mbit/s | | | | 40 | ns |
| | input irradiance = 100 mW/m², 576 kbit/s | | | | 80 | ns |
| | input irradiance = 100 mW/m², ≤ 115.2 kbit/s | | | | 350 | ns |
| Receiver start up time | after completion of shutdown programming sequence<br>Power on delay | | | | 500 | µs |
| Latency | | $t_L$ | | 170 | 300 | µs |

Note: All timing data measured with 4 Mbit/s are measured using the IrDA® FIR transmission header.
The data given here are valid 5 µs after starting the preamble.

*) This parameter reflects the backlight test of the IrDA physical layer specification to guarantee immunity against light from fluorescent lamps

**) Retriggering once during applied optical pulse may occur

## Transmitter

$T_{amb}$ = 25 °C, $V_{CC}$ = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

| Parameter | Test Conditions | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| IRED operating current, switched current limiter | See derating curve (fig. 5). For 3.3 V operations no external resistor needed. For 5 V application that might be necessary depending on operating temperature range. | $I_D$ | 500 | 550 | 600 | mA |
| Output leakage IRED current | | $I_{IRED}$ | - 1 | | 1 | µA |
| Output radiant intensity recommended application circuit | $\alpha$ = 0 °, 15 °<br>Txd = High, SD = Low,<br>$V_{CC1} = V_{CC2}$ = 3.3 V<br>Internally current-controlled, no external resistor | $I_e$ | 120 | 170 | 350 | mW/sr |
| Output radiant intensity | $V_{CC1}$ = 5.0 V, $\alpha$ = 0 °, 15 °<br>Txd = Low or SD = High,<br>(Receiver is inactive as long as SD = High) | $I_e$ | | | 0.04 | mW/sr |
| Output radiant intensity, angle of half intensity | | $\alpha$ | | ± 24 | | ° |
| Peak - emission wavelength | | $\lambda_p$ | 880 | | 900 | nm |
| Spectral bandwidth | | $\Delta\lambda$ | | 40 | | nm |
| Optical rise time, fall time | | $t_{ropt}$, $t_{fopt}$ | 10 | | 40 | ns |
| Optical output pulse duration | input pulse width 217 ns, 1.152 Mbit/s | $t_{opt}$ | 207 | 217 | 227 | ns |
| | input pulse width 125 ns, 4.0 Mbit/s | $t_{opt}$ | 117 | 125 | 133 | ns |
| | input pulse width 250 ns, 4.0 Mbit/s | $t_{opt}$ | 242 | 250 | 258 | ns |
| | input pulse width<br>0.1 µs < $t_{Txd}$ < 100 µs *) | $t_{opt}$ | | $t_{Txd}$ | | µs |
| | input pulse width $t_{Txd} \geq$ 100 µs *) | $t_{opt}$ | 23 | | 100 | µs |
| Optical overshoot | | | | | 25 | % |

*) Typically the output pulse duration will follow the input pulse duration t and will be identical in length t.
However, at pulse duration larger than 100 µs the optical output pulse duration is limited to 100 µs. This pulse duration limitation can already start at 23 µs

## Recommended Circuit Diagram

Vishay Semiconductors transceivers integrate a sensitive receiver and a built-in power driver. The combination of both needs a careful circuit board layout. The use of thin, long, resistive and inductive wiring should be avoided. The inputs (Txd, SD, Mode) and the output Rxd should be directly (DC) coupled to the I/O circuit.

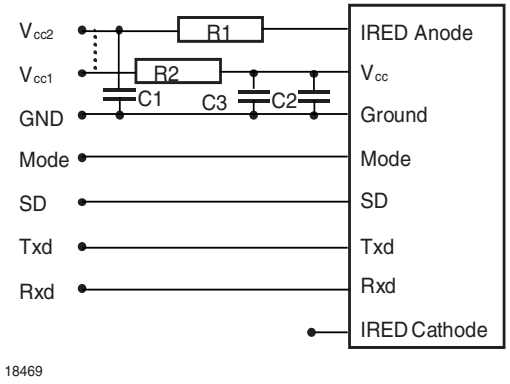



Figure 1. Recommended Application Circuit

The capacitor C1 is buffering the supply voltage and reduces the influence of the inductance of the power supply line. This one should be a Tantalum or other fast capacitor to guarantee the fast rise time of the IRED current. The resistor R1 is only necessary for higher operating voltages and elevated temperatures, see derating curve in figure 5, to avoid too high internal power dissipation.

The capacitors C2 and C3 combined with the resistor R2 (as the low pass filter) is smoothing the supply voltage $V_{CC1}$. R2, C1, C2, and C3 are optional and dependent on the quality of the supply voltages $V_{CC1}$ and $V_{CC2}$ and injected noise. An unstable power supply with dropping voltage during transmission may reduce sensitivity (and transmission range) of the transceiver. The placement of these parts is critical. It is strongly recommended to position C2 and C3 as close as possible to the transceiver power supply pins. An Tantalum capacitor should be used for C1 and C3 while a ceramic capacitor is used for C2.

In addition, when connecting the described circuit to the power supply, low impedance wiring should be used.

When extended wiring is used the inductance of the power supply can cause dynamically a voltage drop at $V_{CC2}$. Often some power supplies are not apply to follow the fast current is rise time. In that case another 4.7 µF (type, see table under C1) at $V_{CC2}$ will be helpful.

Keep in mind that basic RF-design rules for circuit design should be taken into account. Especially longer signal lines should not be used without termination. See e.g. "The Art of Electronics" Paul Horowitz, Wienfield Hill, 1989, Cambridge University Press, ISBN: 0521370957.

### Table 1.
### Recommended Application Circuit Components

| Component | Recommended Value | Vishay Part Number |
|---|---|---|
| C1, C3 | 4.7 µF, 16 V | 293D 475X9 016B |
| C2 | 0.1 µF, Ceramic | VJ 1206 Y 104 J XXMT |
| R1 | **5 V supply voltage:** 2 Ω , 0.25 W ( recommended using two 1 Ω, 0.125 W resistor in series)<br>**3.3 V supply voltage:** no resistors necessary, the internal controller is able to control the current | e.g. 2 x CRCW-1206-1R0-F-RT1 |
| R2 | 47 Ω, 0.125 W | CRCW-1206-47R0-F-RT1 |

## I/O and Software

In the description, already different I/Os are mentioned. Different combinations are tested and the function verified with the special drivers available from the I/O suppliers. In special cases refer to the I/O manual, the Vishay application notes, or contact directly Vishay Sales, Marketing or Application.

## Mode Switching

The TFDU6102 is in the SIR mode after power on as a default mode, therefore the FIR data transfer rate has to be set by a programming sequence using the Txd and SD inputs as described below or selected by setting the Mode Pin. The Mode Pin can be used to statically set the mode (Mode Pin: LOW: SIR, HIGH: 0.576 Mbit/s to 4.0 Mbit/s). If not used or in standby mode, the mode input should float or should not be loaded with more than 50 pF. The low frequency mode covers speeds up to 115.2 kbit/s. Signals with higher data rates should be detected in the high frequency mode. Lower frequency data can also be received in the high frequency mode but with reduced sensitivity.
To switch the transceivers from low frequency mode to the high frequency mode and vice versa, the programming sequences described below are required.

## Setting to the High Bandwidth Mode (0.576 Mbit/s to 4.0 Mbit/s)

1. Set SD input to logic "HIGH".
2. Set Txd input to logic "HIGH". Wait $t_s \geq 200$ ns.
3. Set SD to logic "LOW" (this negative edge latches state of Txd, which determines speed setting).
4. After waiting $t_h \geq 200$ ns Txd can be set to logic "LOW". The hold time of Txd is limited by the maximum allowed pulse length.

After that Txd is enabled as normal Txd input and the transceiver is set for the high bandwidth (576 kbit/s to 4 Mbit/s) mode.

## Setting to the Lower Bandwidth Mode (2.4 kbit/s to 115.2 kbit/s)

1. Set SD input to logic "HIGH".
2. Set Txd input to logic "LOW". Wait $t_s \geq 200$ ns.
3. Set SD to logic "LOW" (this negative edge latches state of Txd, which determines speed setting).
4. Txd must be held for $t_h \geq 200$ ns.

After that Txd is enabled as normal Txd input and the transceiver is set for the lower bandwidth (9.6 kbit/s to 115.2 kbit/s) mode.

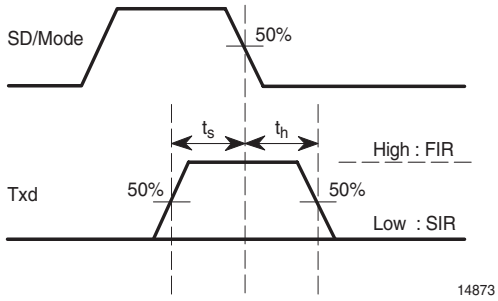



Figure 2. Mode Switching Timing Diagram

## Table 2. Truth table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| SD | Txd | Optical input Irradiance mW/m$^2$ | Rxd | Transmitter |
| high | x | x | weakly pulled (500 kΩ) to $V_{CC1}$ | 0 |
| low | high | x | low (active) | $I_e$ |
| | high > 80 µs | x | high | 0 |
| | low | < 4 | high | 0 |
| | low | > Min. Detection Threshold Irradiance<br>< Max. Detection Threshold Irradiance | low (active) | 0 |
| | low | > Max. Detection Threshold Irradiance | x | 0 |

## Recommended Solder Profile

Solder Profile for Sn/Pb soldering

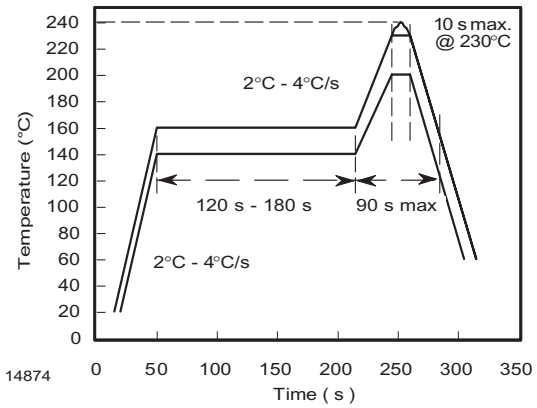



Figure 3. Recommended Solder Profile

## Lead-Free, Recommended Solder Profile

The TFDU6102 is a lead-free transceiver and qualified for lead-free processing. For lead-free solder paste like $Sn_{(3.0\ -\ 4.0)}Ag_{(0.5\ -\ 0.9)}Cu$, there are two standard reflow profiles: Ramp-Soak-Spike (RSS) and Ramp-To-Spike (RTS). The Ramp-Soak-Spike profile was developed primarily for reflow ovens heated by infrared radiation. Shown below in figure 4 is Vishay's recommended profile for use with the TFDU6102 transceivers. For more details please refer to Application note: SMD Assembly Instruction.

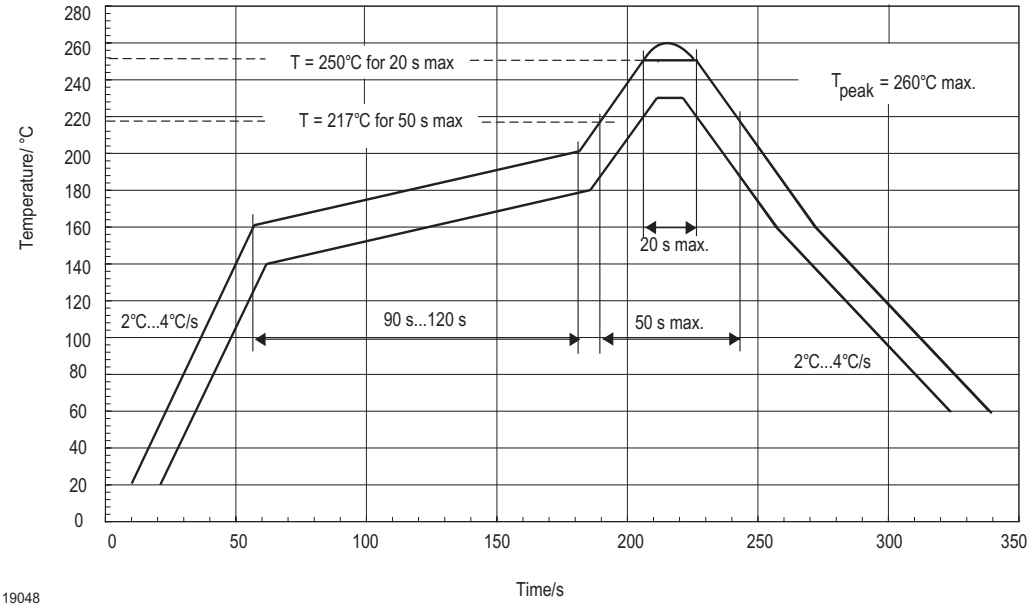



Figure 4. Solder Profile, RSS Recommendation

## Current Derating Diagram

Figure 5 shows the maximum operating temperature when the device is operated without external current limiting resistor. A power dissipating resistor of 2 Ω is recommended from the cathode of the IRED to Ground for supply voltages above 4 V. In that case the device can be operated up to 85 °C, too.

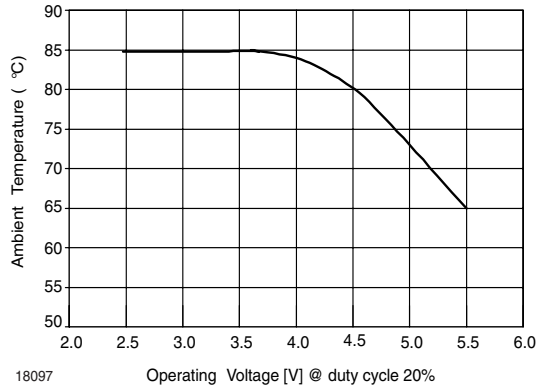
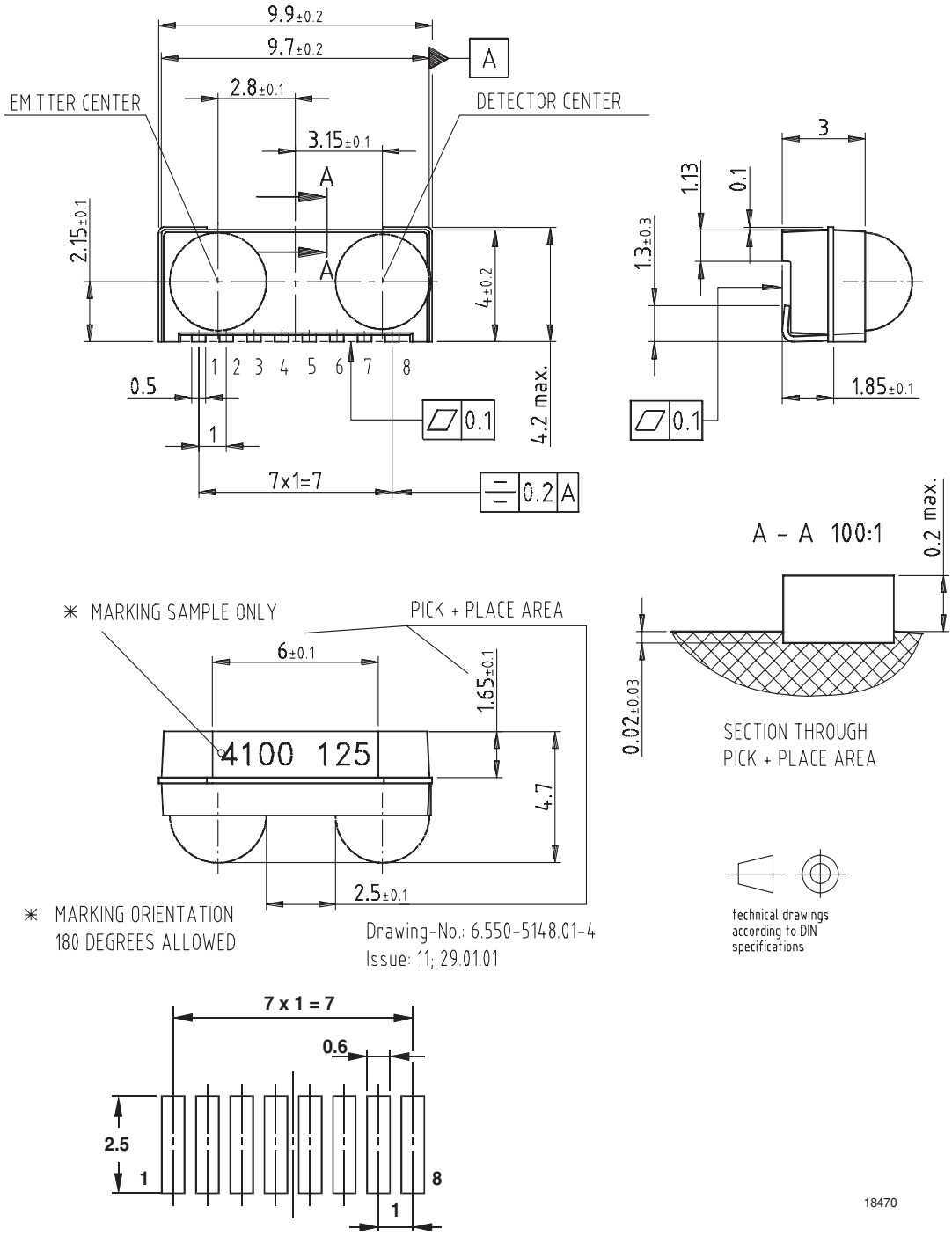
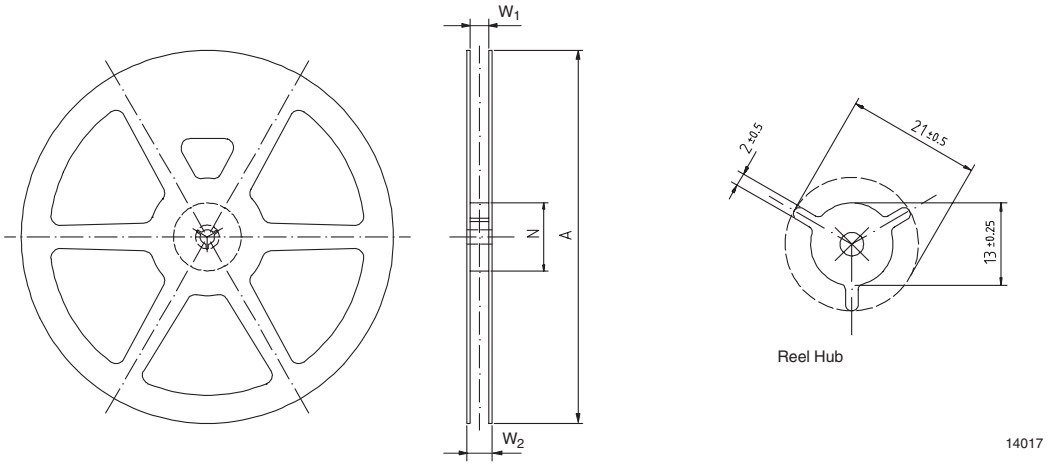



Figure 5. Temperature Derating Diagram

## Package Dimensions in mm

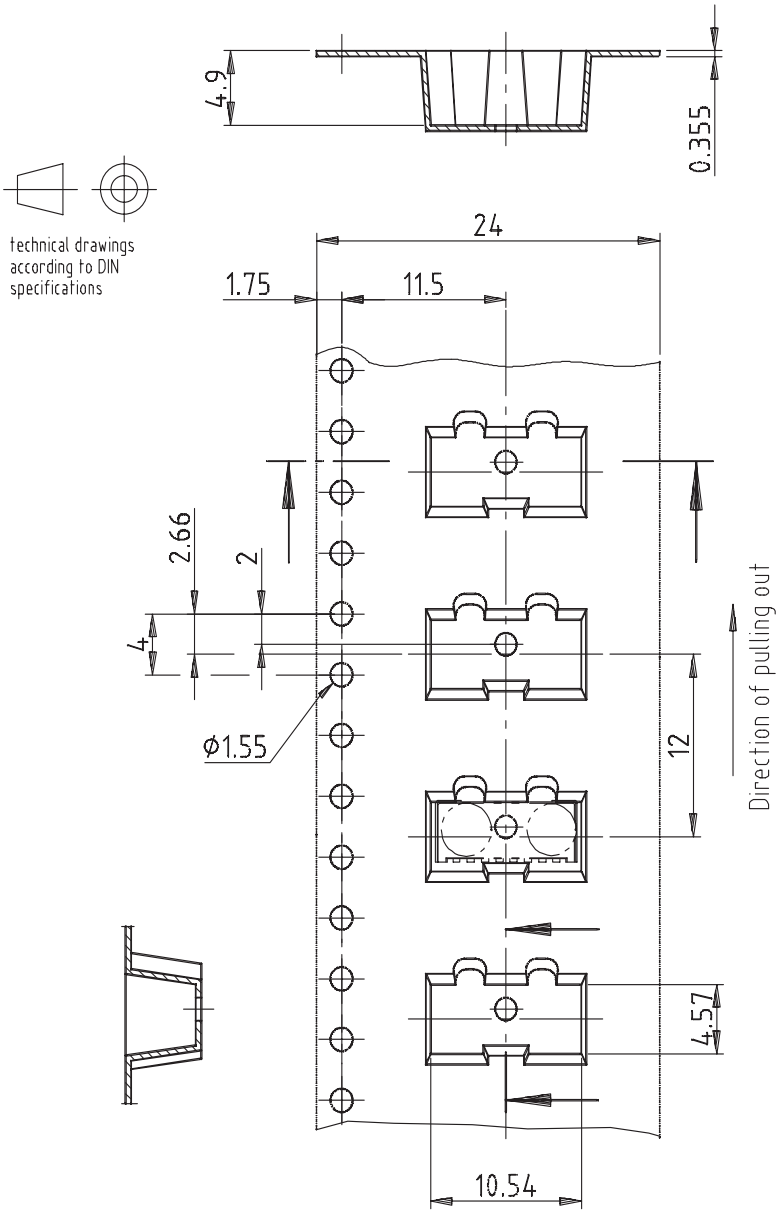


## Reel Dimensions




| Tape Width | A max. | N | $W_1$ min. | $W_2$ max. | $W_3$ min. | $W_3$ max. |
|---|---|---|---|---|---|---|
| mm | mm | mm | mm | mm | mm | mm |
| 24 | 330 | 60 | 24.4 | 30.4 | 23.9 | 27.4 |

## Tape Dimensions in mm

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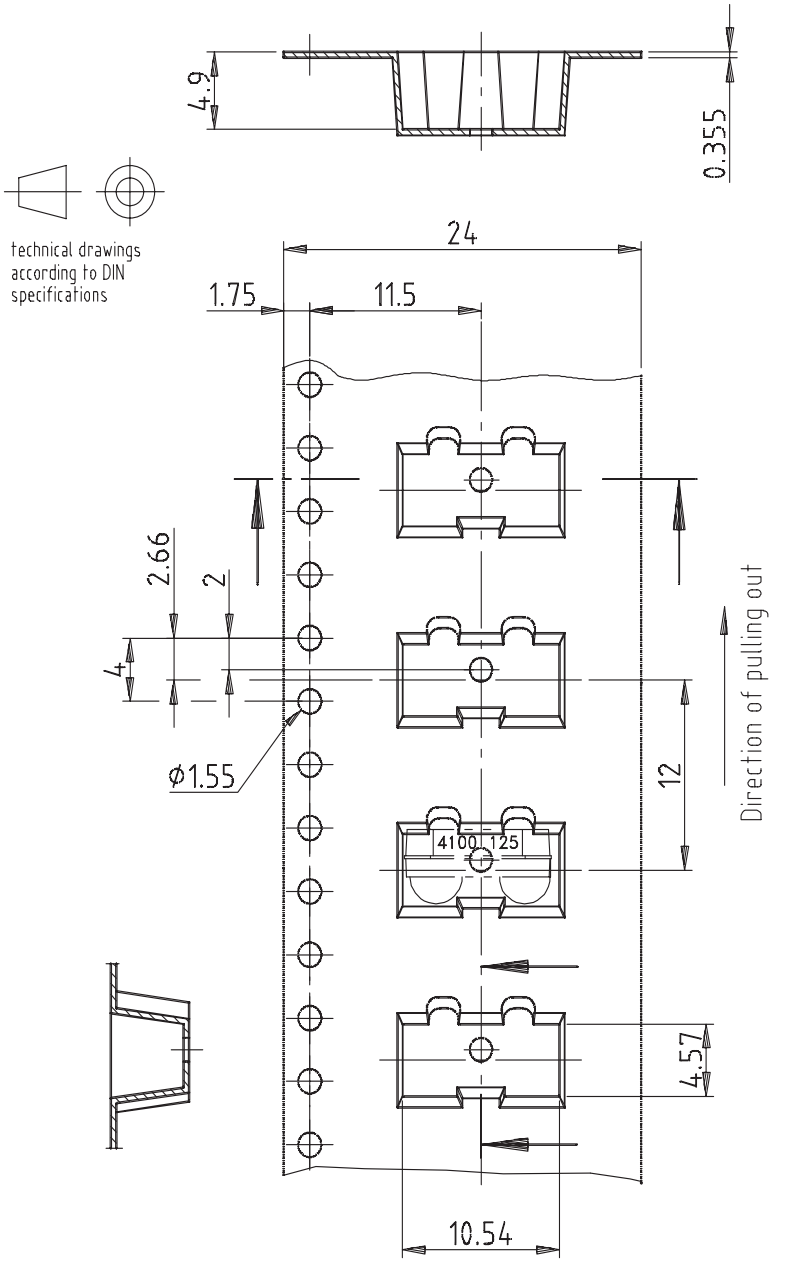


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## Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operatingsystems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

**Vishay Semiconductor GmbH** has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

**Vishay Semiconductor GmbH** can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.



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