APU428

4-Bit Micro-controller With LCD Driver

Features

- Low power dissipation
- Powerful instruction set (148 instructions)
  - Binary addition, subtraction, BCD adjustment, logical operation in direct addressing mode and index
  - addressing mode
  - Single-bit manipulation (set, reset, decision for branch)
  - Various conditional branches
  - 16 working registers and manipulation
  - LCD driver data transfer
  - Look-up table
  - Programmable option
  - System clock selection
- Memory capacity
  - Instruction ROM capacity 2048 x 16 bits
  - Index ROM capacity 256 x 8 bits
  - Internal RAM capacity 256 x 4 bits (low-address 128 nibbles can be accessed by direct addressing, full-range 256 nibbles can be accessed by index addressing)
- Input/output ports
  - Port IOA 4 pins (with internal pull-low, chattering clock, MUX with CX, RR, RT, RH/ SEG 37~40 by mask option)
  - Port IOB 4 pins (MUX with ELC, ELP, BZB, BZ/SEG41, 42 by mask option)
  - Port IOC 4 pins (with internal pull-low, low-level hold, chattering clock, MUX option with AN1~4 by mask option)
  - Port IOD 4 pins (MUX with PWM1, 2/SEG33~36 by mask option)
- 8-level subroutine nesting
- Interrupt function
  - External factor 2 (INT pin & port IOA, IOC input)
  - Internal factor 4 (predivider, 2 timers & RFC)
- Built-in EL-light driver, alarm, frequency or melody generator (MUX with IOB/ SEG41, 42)
- Built-in R to F converter circuit (MUX with IOA/SEG37~40)
- Built-in comparator, 6/8-bit PWM output, 4-bit D/A converter, low-battery detector; this structure can be used as a 4/6/8-bit full range ADC
  - Port PWM 2 pins (MUX with SEG35, 36)
  - Port ADC 4 pins (MUX with IOC)
- 2 6-bit programmable timers with programmable clock source
- Watchdog timer
- LCD/LED driver output
  - 42 LCD/LED driver outputs (up to 168 LCD segments are drivable)
  - Mask option is used to select static, 1/2 bias 1/2 duty, 1/2 bias 1/3 duty, 1/2 bias 1/4 duty, 1/3 bias 1/3 duty and 1/3 bias 1/4 duty drive modes of the LCD panel
  - Mask option is used to select DC output, and static, 1/2 duty, 1/3 duty and 1/4 duty drive modes of the LED panel
  - Mask option is used to select SEG28~32 as P open-drain DC outputs
  - Single instruction stops all segments that are either in LCD or LED
- Built-in voltage doubler, halver, tripler charge pump circuit
- Dual clock operation
- HALT function
- Stop function

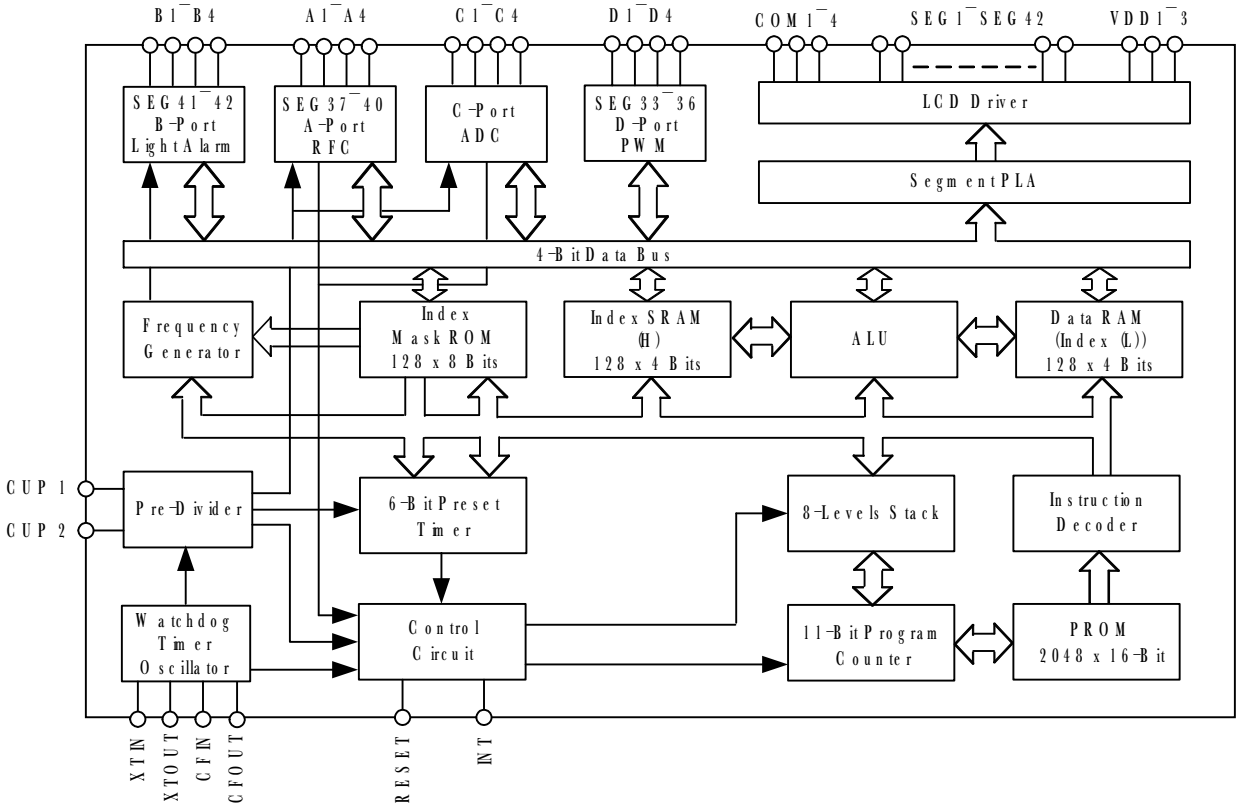
General Description

APU428 is an embedded high-performance 4-bit microcomputer with an LCD/LED driver. It contains all the necessary functions in a single chip: 4-bit parallel processing ALU, ROM, RAM, I/O ports, timer, clock generator, dual clock, ADC, RFC, alarm, EL-light, LCD driver, look-up table and watchdog timer. The instruction set consists of 148 instructions which include nibble operation, manipulation, various conditional branch instructions and LCD data transfer instructions which are powerful and easy to follow.

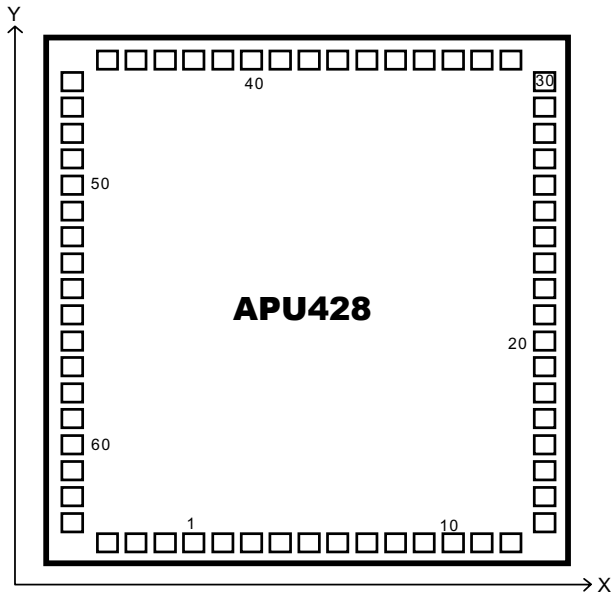
The HALT function stops any internal operations other than the oscillator, divider and LCD driver in order to minimize the power dissipation.

The stop function stops all clocks in the chip.

Block Diagram



Pad Assignment



Pad Coordinates

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	SEG1	560	70	34	SEG34	1480	2265
2	SEG2	675	70	35	SEG35	1365	2265
3	SEG3	790	70	36	SEG36	1250	2265
4	SEG4	905	70	37	SEG37	1135	2265
5	SEG5	1020	70	38	SEG38	1020	2265
6	SEG6	1135	70	39	SEG39	905	2265
7	SEG7	1250	70	40	SEG40	790	2265
8	SEG8	1365	70	41	SEG41	675	2265
9	SEG9	1480	70	42	SEG42	560	2265
10	SEG10	1595	70	43	IOB3	445	2265
11	SEG11	1710	70	44	IOB4	330	2265
12	SEG12	1840	70	45	GND	200	2265
13	SEG13	1970	160	46	VDD	70	2175
14	SEG14	1970	290	47	CFIN	70	2045
15	SEG15	1970	420	48	CFOUT	70	1915
16	SEG16	1970	535	49	XTIN	70	1800
17	SEG17	1970	650	50	XTOUT	70	1685
18	SEG18	1970	765	51	TESTA	70	1570
19	SEG19	1970	880	52	RESET	70	1455

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
20	SEG20	1970	995	53	INT	70	1340
21	SEG21	1970	1110	54	IOM1	70	1225
22	SEG22	1970	1225	55	IOM2	70	1110
23	SEG23	1970	1340	56	IOM3	70	995
24	SEG24	1970	1455	57	IOM4	70	880
25	SEG25	1970	1570	58	VDD1	70	765
26	SEG26	1970	1685	59	VDD2	70	650
27	SEG27	1970	1800	60	VDD3	70	535
28	SEG28	1970	1915	61	CUP1	70	420
29	SEG29	1970	2045	62	CUP2	70	290
30	SEG30	1970	2175	63	COM1	70	160
31	SEG31	1840	2265	64	COM2	200	70
32	SEG32	1710	2265	65	COM3	330	70
33	SEG33	1595	2265	66	COM4	445	70
Chip size: 84.65 x 96.45 mil^2							

Pad Descriptions

Pad Name	I/O	Description
BAK		Positive back-up voltage. In Li mode, connects a 0.1u capacitance to GND.
VDD1 VDD2 VDD3		LCD drives the voltage and positive supply voltage. While in Ag mode, connects +1.5V to V_{DD1}. While in Li/ExtV mode, connects +3.0V to $_{VDD2}$.
RESET	I	Input pin from LSI reset request signal. Internal pull-down resistor.
INT	I	Input pin for external INT request signal. Falling or rising edge triggered by mask option. Internal pull-down or pull-up resistor or none is selected by mask option.
TESTA	I	Test signal input pin.
CUP1 CUP2	O	Switching pins for supplying the LCD driving voltage to the VDD1, 2, 3 pins. Connects the CUP1 and CUP2 pins with nonpolarized electrolytic capacitor if 1/2 or 1/3 bias mode has been selected. In the static mode, these pins should be open.
XIN XOUT	I O	Time-based counter frequency (clock-specified, LCD alternating frequency, alarm signal frequency) or system clock oscillation. 32kHz crystal oscillator. Oscillation stops at the execution of STOP instruction.
CFIN CFOUT	I O	System clock oscillation. Connected with ceramic resonator. Connected with RC oscillation circuit. Oscillation stops at the execution of STOP or SLOW instruction.
COM1~4	O	Output pins for supplying voltage to drive the common pins of the LCD or LED panel.
SEG1~42	O	Output pins for LCD or LED panel segment.
IOA1~4	I/O	Input/Output port A can use software to define the internal pull-low resistor and chattering clock in order to reduce input bounce and generate interrupt. This port shares pins with SEG37~40 and is set by mask option. This port also shares pins with CC, RR, RT and RH, and is set by mask option.

Pad Name	I/O	Description
IOB1~4	I/O	I/O Input/Output port B. IOB1, 2 shares pins with SEG41, 42, or ELC, ELP and is set by mask option. IOB3, 4 shares pins with BZ, BZB and is set by mask option.
IOC1~4	I/O	I/O Input/Output port C can use software to define the internal pull-low/ low-level hold resistor and chattering clock in order to reduce input bounce and generate interrupt. This port shares pins with AN1-4 and is set by mask option.
IOD1~4	I/O	Input / Output port D. This port shares pins with SEG33~36 and is set by mask option. IOD3,4 shares pins with PWM1,2 and is set by mask option.
RFC CC RR RT RH	I O O O	1 input pin and 3 output pins for RFC application. This port shares pins with SEG37~40 and is set by mask option. This port shares pins with IOA1~4 and is set by mask option.
EL ELC ELP	O O	Output port for the EL-light. These ports share pins with SEG41, 42 and are set by mask option. These ports share pins with IOB1, 2 and are set by mask option.
ALM BZB Z	O O	Output port for alarm, frequency or melody generator. This port shares pins with IOB3,4 and is set by mask option.
GND		Negative supply voltage.

Absolute Maximum Rating

Ta = 0 to 70℃ GND=0V

Name	Symbol	Rating	Unit
Maximum Supply Voltage	V_{DD1}	-0.3 ~ +5.5	V
	V_{DD2}	-0.3 ~ +5.5	V
	V_{DD3}	-0.3 ~ +8.5	V
Maximum Input Voltage	V_{IN}	-0.3 to $V_{DD1/2}$+0.3	V
Maximum Output Voltage	V_{OUT1}	-0.3 to $V_{DD1/2}$+0.3	V
	V_{OUT2}	-0.3 to V_{DD3}+0.3	V
Maximum Operating Temperature	t_{OPG}	0 to +70	℃
Maximum Storage Temperature	t_{STG}	-25 to +125	℃

Allowable operating conditions

Ta = 0 to 70℃ GND=0V

Name	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	V_{DD1}		1.2	5.25	V
	V_{DD2}		2.4	5.25	V
	V_{DD3}		2.4	8.0	V
Oscillator Start-up Voltage	V_{DDB}	Crystal Mode	1.3		V
Oscillator Sustain Voltage	V_{DDB}	Crystal Mode	1.2		V
Supply Voltage	V_{DD1}	Ag Mode	1.2	1.65	V
Supply Voltage	V_{DD2}	EXT-V, Li Mode	2.4	5.25	V
Input ″H″ Voltage	V_{IH1}	Ag Battery Mode	$V_{DD1-0.7}$	$V_{DD1+0.7}$	V
Input ″L″ Voltage	V_{IL1}		-0.7	0.7	V
Input ″H″ Voltage	V_{IH2}	Li Battery Mode	$V_{DD2-0.7}$	$V_{DD2+0.7}$	V
Input ″L″ Voltage	V_{IL2}		-0.7	0.7	V
Input ″H″ Voltage	V_{IH3}	OSCIN at Ag Battery Mode	$0.8V_{DD1}$	V_{DD1}	V
Input ″L″ Voltage	V_{IL3}		0	$0.2V_{DD1}$	V
Input ″H″ Voltage	V_{IH4}	OSCIN at Li Battery Mode	$0.8V_{DD2}$	V_{DD2}	V
Input ″L″ Voltage	V_{IL4}		0	$0.2V_{DD2}$	V
Input ″H″ Voltage	V_{IH5}	CFIN at Li Battery or EXT-V Mode	$0.8V_{DD2}$	V_{DD2}	V
Input ″L″ Voltage	V_{IL5}		0	$0.2V_{DD2}$	V
Input ″H″ Voltage	V_{IH6}	RC Mode	$0.8V_{DDO}$	V_{DDO}	V
Input ″L″ Voltage	V_{IL6}		0	$0.2V_{DDO}$	V
Operating Freq.	f_{OPG1}	Crystal Mode	32	3580	kHz
	f_{OPG2}	External RC Mode	32	1000	kHz
	f_{OPG3}	CF Mode	1000	3580	kHz

Electrical Characteristics

Ta=0 to 70℃

Input resistance

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
″L″-Level Hold t_R (IOC)	R_{IIH1}	V_I=0.2V_{DD1}, #1	10	40	100	kΩ
	R_{IIH2}	V_I=0.2V_{DD2}, #2	10	40	100	kΩ
	R_{IIH3}	V_I=0.2V_{DD2}, #3	5	20	50	kΩ
IOC/IOA Pull-Down t_R	R_{MSD1}	V_I=V_{DD1}, #1	200	500	1000	kΩ
	R_{MSD2}	V_I=V_{DD2}, #2	200	500	1000	kΩ
	R_{MSD3}	V_I=V_{DD3}, #3	100	250	500	kΩ
INT Pull-Up t_R	R_{INTU1}	V_I=V_{DD1}, #1	200	500	1000	kΩ
	R_{INTU2}	V_I=V_{DD2}, #2	200	500	1000	kΩ
	R_{INTU3}	V_I=V_{DD3}, #3	100	250	500	kΩ
INT Pull-Down t_R	R_{INTD1}	V_I=GND, #1	200	500	1000	kΩ
	R_{INTD2}	V_I=GND, #2	200	500	1000	kΩ
	R_{INTD3}	V_I=GND, #3	100	250	500	kΩ
RES Pull-Down t_R	R_{RES1}	V_I=GND or V_{DD1}, #1	5	20	50	kΩ
	R_{RES2}	V_I=GND or V_{DD2}, #2	5	20	50	kΩ
	R_{RES3}	V_I=GND or V_{DD2}, #3	5	20	50	kΩ

Note: #1: V_{DD1}= 1.2V (Ag), #2: V_{DD2}= 2.4V (Li), #3: V_{DD2}= 4V (Ext-V).

DC output characteristics

Name	Symbol	Condition	For	Min.	Typ.	Max.	Unit
Output ″H″ Voltage	V_{OH1a}	I_{OH}=-10μA, #1	SEG1~ SEG32	0.8	0.9	1.0	V
	V_{OH2a}	I_{OH}=-50μA, #2		1.5	1.8	2.1	V
	V_{OH3a}	I_{OH}=-200μA, #3		2.5	3	3.5	V
Output ″L″ Voltage	V_{OL1a}	I_{OL}=20μA, #1		0.2	0.3	0.4	V
	V_{OL2a}	I_{OL}=100μA, #2		0.3	0.6	0.9	V
	V_{OL3a}	I_{OL}=400μA, #3		0.5	1.0	1.5	V
Output ″H″ Voltage	V_{OH1c}	I_{OH}=-200μA, #1	SEG33~ SEG42, IOB3~4, IOC-n	0.8	0.9	1.0	V
	V_{OH2c}	I_{OH}=-1mA, #2		1.5	1.8	2.1	V
	V_{OH3c}	I_{OH}=-3mA, #3		2.5	3	3.5	V
Output ″L″ Voltage	V_{OL1c}	I_{OL}=400μA, #1		0.2	0.3	0.4	V
	V_{OL2c}	I_{OL}=2mA, #2		0.3	0.6	0.9	V
	V_{OL3c}	I_{OL}=6mA, #3		0.5	1.0	1.5	V

Note: #1: V_{DD1}= 1.2V (Ag), #2: V_{DD2}= 2.4V (Li), #3: V_{DD2}= 4V (Ext-V).

Segment driver output characteristics

Name	Symbol	Condition	For	Min.	Typ.	Max.	Unit
Static display mode							
Output ″H″ Voltage	V_{OH1d}	I_{OH}=-1μA, #1	SEG-n	1.0			V
	V_{OH2d}	I_{OH}=-1μA, #2		2.2			V
	V_{OH3d}	I_{OH}=-1μA, #3		3.8			V
Output ″L″ Voltage	V_{OL1d}	I_{OL}=1μA, #1				0.2	V
	V_{OL2d}	I_{OL}=1μA, #2				0.2	V
	V_{OL3d}	I_{OL}=1μA, #3				0.2	V
Output ″H″ Voltage	V_{OH1e}	I_{OH}=-10μA, #1	COM-n	1.0			V
	V_{OH2e}	I_{OH}=-10μA, #2		2.2			V
	V_{OH3e}	I_{OH}=-10μA, #3		3.8			V
Output ″L″ Voltage	V_{OL1e}	I_{OL}=10μA, #1				0.2	V
	V_{OL2e}	I_{OL}=10μA, #2				0.2	V
	V_{OL3e}	I_{OL}=10μA, #3				0.2	V
1/2 bias display mode							
Output ″H″ Voltage	V_{OH12f}	I_{OH}=-1μA, #1, #2	SEG-n	2.2			V
	V_{OH3f}	I_{OH}=-1μA, #3		3.8			V
Output ″L″ Voltage	V_{OL12f}	I_{OL}=1μA, #1, #2				0.2	V
	V_{OL3f}	I_{OL}=1μA, #3				0.2	V
Output ″H″ Voltage	V_{OH12g}	I_{OH}=-10μA, #1, #2	COM-n	2.2			V
	V_{OH3g}	I_{OH}=-10μA, #3		3.8			V
Output ″M″ Voltage	V_{OM12g}	$I_{OI/H}$=±10μA, #1, #2		1.0		1.4	V
	V_{OM3g}	$I_{OI/H}$=±10μA, #3		1.8		2.2	V
Output ″L″ Voltage	V_{OL12g}	I_{OL}=10μA, #1, #2				0.2	V
	V_{OL3g}	I_{OL}=10μA, #3				0.2	V
1/3 bias display mode							
Output ″H″ Voltage	V_{OH12i}	I_{OH}=-1μA, #1, #2	SEG-n	3.4			V
	V_{OH3i}	I_{OH}=-1μA, #3		5.8			V
Output ″M1″ Voltage	V_{OM12i}	$I_{OI/H}$=±10μA, #1, #2		1.0		1.4	V
	V_{OM13i}	$I_{OI/H}$=±10μA, #3		1.8		2.2	V
Output ″M2″ Voltage	V_{OM22i}	$I_{OI/H}$=±10μA, #1, #2		2.2		2.6	V
	V_{OM23i}	$I_{OI/H}$=±10μA, #3		3.8		4.2	V
Output ″L″ Voltage	V_{OL12i}	I_{OL}=1μA, #1, #2				0.2	V
	V_{OL3i}	I_{OL}=1μA, #3				0.2	V
Output ″H″ Voltage	V_{OH12j}	I_{OH}=-10μA, #1, #2	COM-n	3.4			V
	V_{OH3j}	I_{OH}=-10μA, #3		5.8			V
Output ″M1″ Voltage	V_{OM12j}	$I_{OI/H}$=±10μA, #1, #2		1.0		1.4	V
	V_{OM13j}	$I_{OI/H}$=±10μA, #3		1.8		2.2	V
Output ″M2″ Voltage	V_{OM22j}	$I_{OI/H}$=±10μA, #1, #2		2.2		2.6	V
	V_{OM23j}	$I_{OI/H}$=±10μA, #3		3.8		4.2	V
Output ″L″ Voltage	V_{OL12j}	I_{OL}=10μA, #1, #2				0.2	V
	V_{OL3j}	I_{OL}=10μA, #3				0.2	V

Note: #1: V_{DD1}= 1.2V (Ag), #2: V_{DD2}= 2.4V (Li), #3: V_{DD2}= 4V (Ext-V).

Functional Description

Index SRAM

The 256 X 4 bits index SRAM is used for applications that need more SRAM or need to load addresses by operation, and data SRAM is included at a lower-half address in the index SRAM.

Index ROM

The 256 X 8 bits index ROM can be used in the 4-bit or 8-bit mode.

I/O ports

The IOA port can be selected by software separately as input or output. It can also be selected with/without internal pull-low and different chattering clocks for a HALT release / interrupt trigger in order to reduce the input bounce for the key scan:

PH6: 512Hz, PH8: 128Hz, PH10: 32Hz.

The pull-low of IOA will be masked off for those pins defined as output pins:

The IOA port can be used as a pseudo serial output port.

The IOB port can be selected by software separately as input or output.

Th e IOC port can be selected by software separately as input or output, and with/without internal pull-low and different chattering clocks for a HALT release /interrupt trigger in order to reduce the bounce of the key scan.

The pull-low of the IOC will be masked off for those pins defined as output pins.

The IOD port can be selected by software separately as input or output.

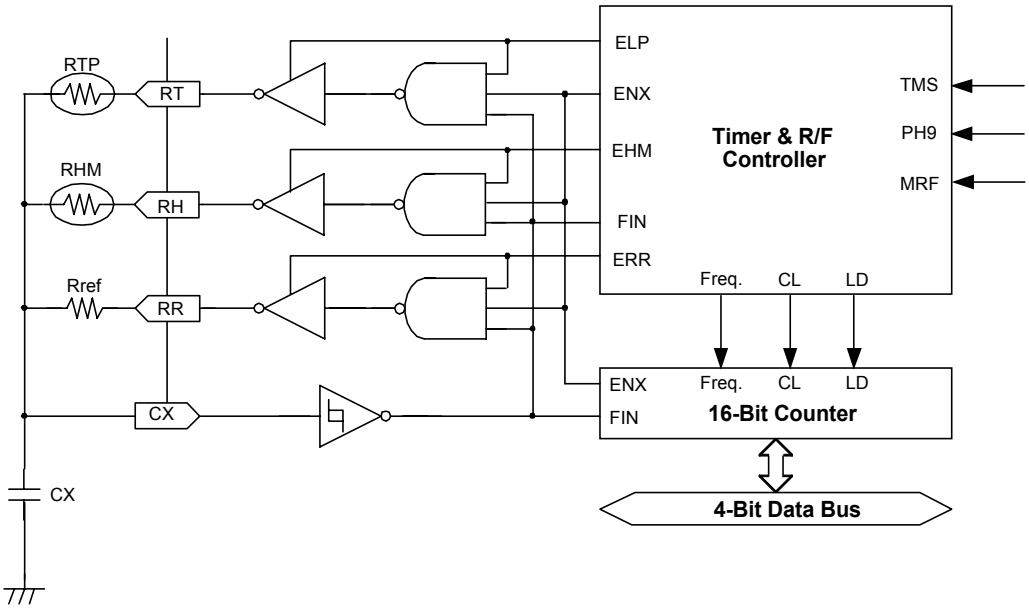
The IOD port can be used as a pseudo serial output port.

The initial state of all I/O ports is the standard input state, and IOA and C have pull-low.

Before setting the I/O ports from input to output, execute the output function first to ensure the output state.

Resistor to frequency converter

We use an RC oscillation circuit and a 16-bit counter to calculate the relative resistance of temperature and humidity sensor. The diagram is shown below:



There are 2 methods for measuring the input frequency. First, set FIN (i.e. CX) as the clock input and use timer 2 or the software directly as interval control. Second, if the FIN (CX) frequency is too low (either because of a poor resolution for a fixed interval or a longer interval for better resolution but a longer read-out rate, ex.10 seconds per read-out), you can switch the measure mode to set FIN (CX) as the interval control. It will

enable the counter from the first FIN rising edge to the next rising edge, then will generate an interrupt. It may also use FREQ (internal frequency generator output) as clock input, hence counting the CX interval. For measuring the resistor value of the temperature and humidity sensor, we must first measure the frequency of Rref, then the frequency of Sensor:

Fref= K / Rref CX and

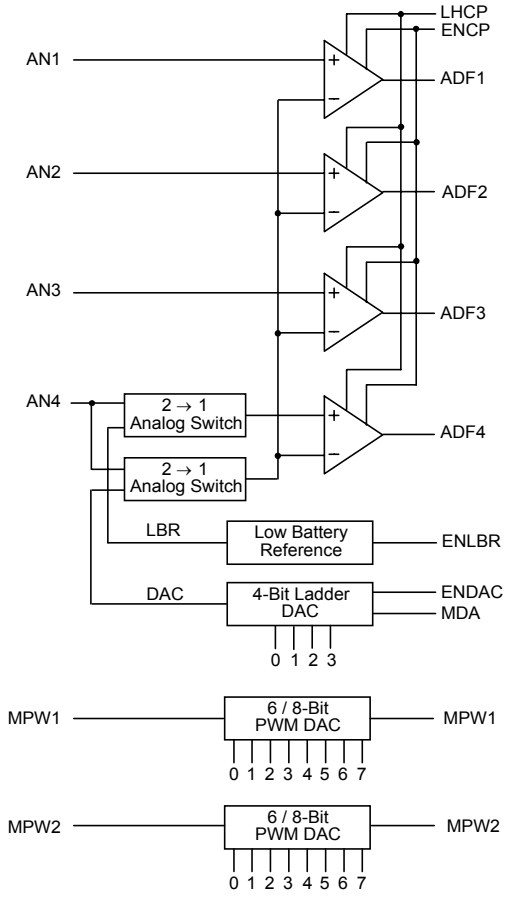
Fsensor= K / Rsensor CX, hence

Rsensor = Rref * Freq / Fsensor.

The CX input can be used as a clock counter.

Analog-to-Digital converter

The diagram is shown below:

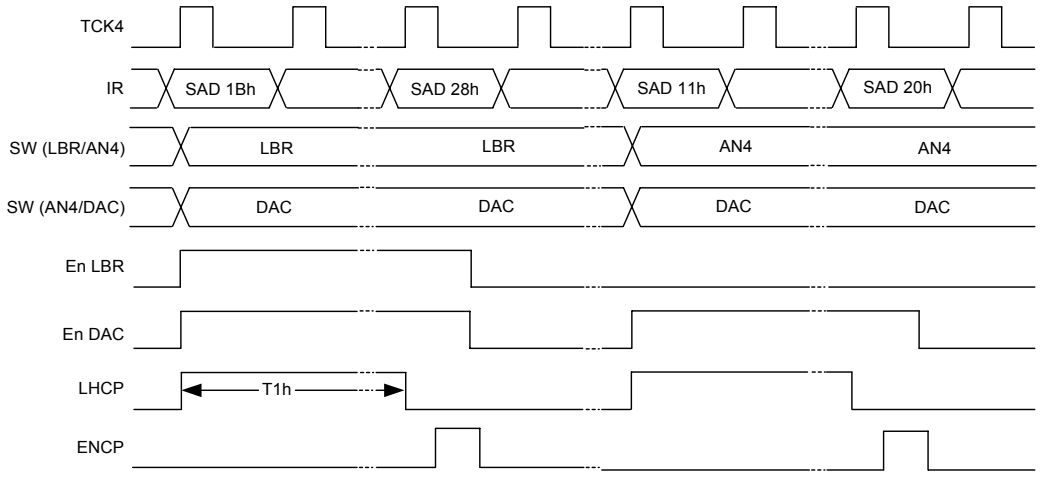


The use of these blocks is illustrated below:

- Comparator: Sets negative input as AN4, compare with AN1, 2, 3.
- 4-bit ADC: Sets negative input as internal 4-bit DAC, positive input as AN4, software control for AN1, 2, 3, 4 analog value archive.
- Low battery detector: Sets negative input as internal 4-bit DAC, positive input as LBR (low battery reference). If the DAC level is lower than LBR, it means there is a low-battery condition.
- PWM DAC output: With an external RC network, 6-bit or 8-bit PWM DAC can be used.
- 6-bit/ 8-bit ADC: Sets negative input as AN4, connects from PWM with an external RC network. You can get analog value from AN1, 2, 3.
- Supply voltage measurement: Sets negative input as AN4, connects from PWM with an external RC network, positive input is LBR. If comparative data is N, the supply voltage is LBR (about 1.26V) * 255 / N.

Note: The internal 4-bit DAC level is 1/32 V_{DD} for 0, 3/32 for 1, 29/32 for E and 31/32 for F. The level of 6-bit PWM is 0/63, 1/63, 62/63 and 63/63, and the level of 8-bit PWM is 0/255, 1/255, 254/255 and 255/255.

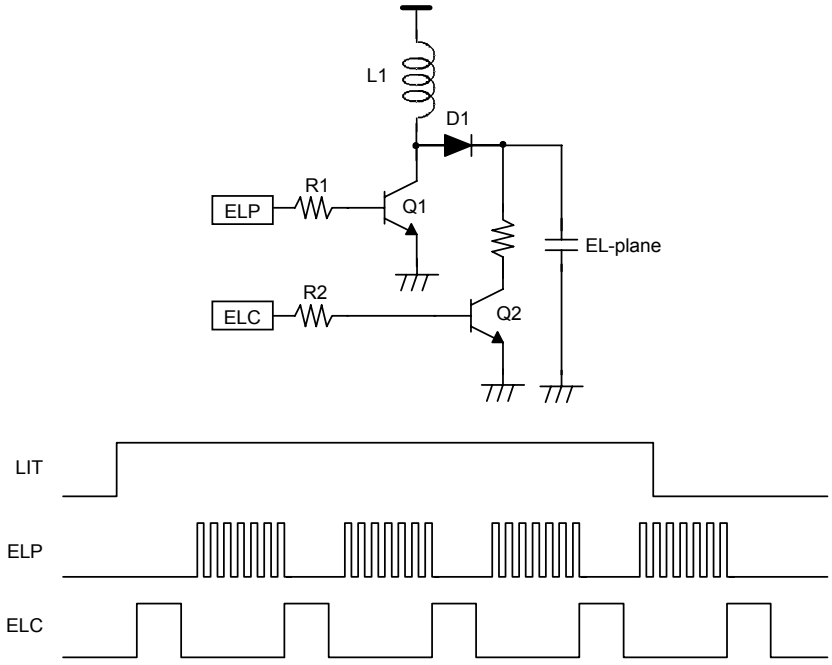
An example of ADC timing is shown below:



Note: Power Supply = 1.2V ⇒ T1h needs 5ms
Power Supply = 2.4V ⇒ T1h needs 10μs

EL-light

Sets ELC and ELP clock and duty cycle using ELC X instruction, then turn on and off ELC and ELP output by SF X and RF X instruction. With external transistor, diode, inductor and resistor, we can pump the EL panel to AC 100~250V.



When the EL-light is turned on, the ELC will turn on before ELP, but when the EL-light is off, the ELP and ELC will turn off after the next falling edge of ELC in order to make sure no voltage is left on the EL plane.

Timer

The 6-bit programmable timer can select PH3/PH9/PH15/FREQ (Timer 2 can also select PH5/PH7/PH11/PH13 by TM2X instruction) as the clock source. When it underflows, HALT release signals are generated.

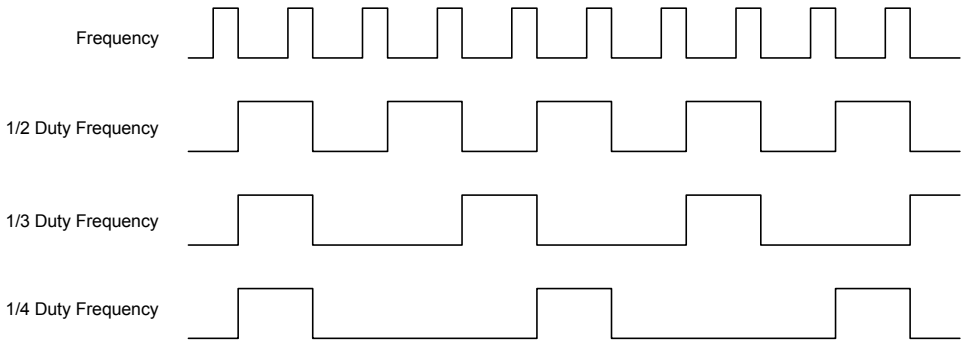
Predivider

The predivider is a 15-sage counter that uses PH0 as clock source. The output of T-FF is changed when the input signal is changed from H to L. PH11~15 are reset to L when PLC 100H instruction is executed, power-on reset or external reset is used. When PH14 is changed from H to L, the HALT release signal is generated.

Alarm/frequency/melody

There is an 8-bit programmable counter and an 8-bit envelope control for alarm, frequency or melody output from BZ/BZB.

The frequency counter can use software to select 1/2 duty, 1/3 duty,1/4 duty drive modes.



INT function

The INT pin can be selected by mask option as pull-high/pull-low or none, and as a rising edge/falling edge trigger.

Watchdog Timer

The watchdog timer automatically generates a device reset when it overflows. The interval of overflow is 8/64/512 x PH10 (set by mask option). You can use software to enable and disable this function. The watchdog enable flag will be disabled by power on reset or reset pin reset condition, but cannot be disabled by watchdog reset itself.

HALT function

The HALT instruction disables all clocks except the predivider, timer, frequency counter, PWM, EL-light generator and chattering clock in order to minimize the operating current.

STOP function

The STOP instruction disables all clocks to minimize the standby current, so only two external factors (INT, IOA/IOC) can release the stop condition.

Instruction Table

Instruction	Machine Code	Function	Flag/Remark
NOP	0000 0000 0000 0000	No Operation	
LCT Lz, Ry	0000 001Z ZZZZ YYYY	Lz ← { 7SEG ← Ry}	
LCB Lz, Ry	0000 010Z ZZZZ YYYY	Lz ← { 7SEG ← Ry}	
LCP Lz, Ry	0000 011Z ZZZZ YYYY	Lz ← Ry , AC	
LCD Lz, @HL	0000 100Z ZZZZ 0000	Lz ← T@HL	
OPA Rx	0000 1010 0XXX XXXX	Port(A) ← Rx	
OPAS Rx, D	0000 1011 DXXX XXXX	A1, 2, 3, 4 ← Rx0, Rx1, D, Pulse	
OPB Rx	0000 1100 0XXX XXXX	Port(B) ← Rx	

Instruction	Machine Code	Function	Flag/Remark
OPC Rx	0000 1101 0XXX XXXX	Port(C) ← Rx	
OPD Rx	0000 1110 0XXX XXXX	Port(D) ← Rx	
OPDS Rx	0000 1111 DXXX XXXX	D1, 2, 3, 4 ← Rx0, Rx1, D, Pulse	
FRQ Rx, D	0001 00DD 0XXX XXXX	FREQ ← Rx, AC DD=00: 1/4 Duty DD=01: 1/3 Duty DD=10: 1/2 Duty	
FRQ D,@HL	0001 01DD 0000 0000	FREQ ← T@HL	
FRQX D,X	0001 10DD XXXX XXXX	FREQ ← X	
MVL Rx	0001 1100 0XXX XXXX	L ← Rx	
MVH Rx	0001 1101 0XXX XXXX	H ← Rx	
MPW1 Rx	0001 1110 0XXX XXXX	PWM1 ← Rx , AC	
MPW2 Rx	0001 1111 0XXX XXXX	PWM2 ← Rx , AC	
ADC Rx	0010 0000 0XXX XXXX	AC ← Rx+AC+CF	CF
ADC @HL	0010 0000 1000 0000	AC ← @HL+AC+CF	CF
ADC* Rx	0010 0001 0XXX XXXX	AC, Rx ← Rx+AC+CF	CF
ADC* @HL	0010 0001 1000 0000	AC, @HL ← @HL+AC+CF	CF
SBC Rx	0010 0010 0XXX XXXX	AC ← Rx+ACB+CF	CF
SBC @HL	0010 0010 1000 0000	AC ← @HL+ACB+CF	CF
SBC* Rx	0010 0011 0XXX XXXX	AC, Rx ← Rx+ACB+CF	CF
SBC* @HL	0010 0011 1000 0000	AC, @HL ← @HL+ACB+CF	CF
ADD Rx	0010 0100 0XXX XXXX	AC ← Rx+AC	CF
ADD @HL	0010 0100 1000 0000	AC ← @HL+AC	CF
ADD* Rx	0010 0101 0XXX XXXX	AC,Rx ← Rx+AC	CF
ADD* @HL	0010 0101 1000 0000	AC, @HL ← @HL+AC	CF
SUB Rx	0010 0110 0XXX XXXX	AC ← Rx+ACB+1	CF
SUB @HL	0010 0110 1000 0000	AC ← @HL+ACB+1	CF
SUB* Rx	0010 0111 0XXX XXXX	AC, Rx ← Rx+ACB+1	CF
SUB* @HL	0010 0111 1000 0000	AC,@HL ← @HL+ACB+1	CF
ADN Rx	0010 1000 0XXX XXXX	AC ← Rx+AC	
ADN @HL	0010 1000 1000 0000	AC ← @HL+AC	
ADN* Rx	0010 1001 0XXX XXXX	AC, Rx ← Rx+AC	
ADN* @HL	0010 1001 1000 0000	AC,@HL ← @HL+AC	
AND Rx	0010 1010 0XXX XXXX	AC ← Rx AND AC	
AND @HL	0010 1010 1000 0000	AC ← @HL AND AC	
AND* Rx	0010 1011 0XXX XXXX	AC, Rx ← Rx AND AC	
AND* @HL	0010 1011 1000 0000	AC,@HL ← @HL AND AC	
EOR Rx	0010 1100 0XXX XXXX	AC ← Rx EXOR AC	
EOR @HL	0010 1100 1000 0000	AC ← @HL EXOR AC	
EOR* Rx	0010 1101 0XXX XXXX	AC, Rx ← Rx EXOR AC	
EOR* @HL	0010 1101 1000 0000	AC,@HL ← @HL EXOR AC	

Instruction	Machine Code	Function	Flag/Remark
OR Rx	0010 1110 0XXX XXXX	AC ← Rx OR AC	
OR @HL	0010 1110 1000 0000	AC ← @HL OR AC	
OR* Rx	0010 1111 0XXX XXXX	AC, Rx ← Rx OR AC	
OR* @HL	0010 1111 1000 0000	AC,@HL ← @HL OR AC	
ADCI Ry,D	0011 0000 DDDD YYYY	AC ← Ry+D+CF CF	
ADCI* Ry,D	0011 0001 DDDD YYYY	AC, Ry ← Ry+D+CF	CF
SBCI Ry,D	0011 0010 DDDD YYYY	AC ← Ry+DB+CF	CF
SBCI* Ry,D	0011 0011 DDDD YYYY	AC, Ry ← Ry+DB+CF	CF
ADDI Ry,D	0011 0100 DDDD YYYY	AC ← Ry+D	CF
ADDI* Ry,D	0011 0101 DDDD YYYY	AC, Ry ← Ry+D	CF
SUBI Ry,D	0011 0110 DDDD YYYY	AC ← Ry+DB+1	CF
SUBI* Ry,D	0011 0111 DDDD YYYY	AC, Ry ← Ry+DB+1	CF
ADNI Ry,D	0011 1000 DDDD YYYY	AC ← Ry+D	
ADNI* Ry,D	0011 1001 DDDD YYYY	AC, Ry ← Ry+D	
ANDI Ry,D	0011 1010 DDDD YYYY	AC ← Ry AND D	
ANDI* Ry,D	0011 1011 DDDD YYYY	AC, Ry ← Ry AND D	
EORI Ry,D	0011 1100 DDDD YYYY	AC ← Ry EXOR D	
EORI* Ry,D	0011 1101 DDDD YYYY	AC, Ry ← Ry EXOR D	
ORI Ry,D	0011 1110 DDDD YYYY	AC ← Ry OR D	
ORI* Ry,D	0011 1111 DDDD YYYY	AC, Ry ← Ry OR D	
INC* Rx	0100 0000 0XXX XXXX	AC, Rx ← Rx+1	
INC* @HL	0100 0000 1000 0000	AC, @HL ← @HL+1	
DEC* Rx	0100 0001 0XXX XXXX	AC, Rx ← Rx-1	
DEC* @HL	0100 0001 1000 0000	AC, @HL ← @HL-1	
IPA Rx	0100 0010 0XXX XXXX	AC, Rx ← Port(A)	
IPB Rx	0100 0100 0XXX XXXX	AC, Rx ← Port(B)	
IPC Rx	0100 0111 0XXX XXXX	AC, Rx ← Port(C)	
IPD Rx	0100 1000 0XXX XXXX	AC, Rx ← Port(D)	
MAF Rx	0100 1010 0XXX XXXX	AC,Rx ← STS1	B3: CF B2: AC=0 B1: (No use) B0: (No use)
MSB Rx	0100 1011 0XXX XXXX	AC,Rx ← STS2	B3: (No use) B2: SCF2(HRx) B1: SCF1(CPT) B0: BCF
MSC Rx	0100 1100 0XXX XXXX	AC,Rx ← STS3	B3: SCF7(PDV) B2: PH15 B1: SCF5(TMR1) B0: SCF4(INT)
MCX Rx	0100 1101 0XXX XXXX	AC,Rx ← STS3X	B3: SCF9(RFC) B2: SCF0(APT) B1: SCF6(TMR2) B0: (No use)

Instruction	Machine Code	Function	Flag/Remark
MSD Rx	0100 1110 0XXX XXXX	AC,Rx ← STS4	B3: (No use) B2: RFOVF B1: WDF B0: CSF
MDX Rx	0100 1111 0XXX XXXX	AC,Rx ← STS4X	B3: ADF4 B2: ADF3 B1: ADF2 B0: ADF1
SR0 Rx	0101 0000 0XXX XXXX	ACn, Rxn ← Rx(n+1) AC3, Rx3 ← 0	
SR1 Rx	0101 0001 0XXX XXXX	ACn, Rxn ← Rx(n+1) AC3, Rx3 ← 1	
SL0 Rx	0101 0010 0XXX XXXX	ACn, Rxn ← Rx(n-1) AC0, Rx0 ← 0	
SL1 Rx	0101 0011 0XXX XXXX	Can, Rxn ← Rx(n-1) AC0, Rx0 ← 1	
DAA	0101 0100 0000 0000	AC ← BCD(AC)	
DAA* Rx	0101 0101 0XXX XXXX	AC, Rx ← BCD(AC)	
DAA* @HL	0101 0101 1000 0000	AC, @HL ← BCD(AC)	
DAS	0101 0110 0000 0000	AC ← BCD(AC)	
DAS* Rx	0101 0111 0XXX XXXX	AC, Rx ← BCD(AC)	
DAS* @HL	0101 0111 1000 0000	AC, @HL ← BCD(AC)	
LDS Rx,D	0101 1DDD DXXX XXXX	AC, Rx ← D	
LDH Rx,@HL	0110 0000 0XXX XXXX	AC, Rx ← H(T@HL)	
LDH* Rx,@HL	0110 0001 0XXX XXXX	AC, Rx ← H(T@HL) HL ← HL + 1	
LDL Rx,@HL	0110 0010 0XXX XXXX	AC, Rx ← L(T@HL)	
LDL* Rx,@HL	0110 0011 0XXX XXXX	AC, Rx ← L(T@HL) HL ← @HL + 1	
MRF1 Rx	0110 0100 0XXX XXXX	AC,Rx ← RFC3-0	
MRF2 Rx	0110 0101 0XXX XXXX	AC,Rx ← RFC7-4	
MRF3 Rx	0110 0110 0XXX XXXX	AC,Rx ← RFC11-8	
MRF4 Rx	0110 0111 0XXX XXXX	AC,Rx ← RFC15-12	
STA Rx	0110 1000 0XXX XXXX	Rx ← AC	
STA @HL	0110 1000 1000 0000	@HL ← AC	
LDA Rx	0110 1100 0XXX XXXX	AC ← Rx	
LDA @HL	0100 1100 1000 0000	AC ← @HL	
MRA Rx	0110 1101 0XXX XXXX	CF ← Rx3	CF
MRW @HL,Rx	0110 1110 0XXX XXXX	AC,@HL ← Rx	
MWR Rx,@HL	0110 1111 0XXX XXXX	AC,Rx ← @HL	
MRW Ry,Rx	0111 0YYY YXXX XXXX	AC,Ry ← Rx	
MWR Rx,Ry	0111 1YYY YXXX XXXX	AC,Rx←Ry	
JB0 X	1000 0XXX XXXX XXXX	PC ← X	if AC0 = 1

Instruction	Machine Code	Function	Flag/Remark
JB1 X	1000 1XXX XXXX XXXX	PC ← X	if AC1 = 1
JB2 X	1001 0XXX XXXX XXXX	PC ← X	if AC2 = 1
JB3 X	1001 1XXX XXXX XXXX	PC ← X	if AC3 = 1
JNZ X	1010 0XXX XXXX XXXX	PC ← X	if AC ≠ 0
JNC X	1010 1XXX XXXX XXXX	PC ← X	if CF = 0
JZ X	1011 0XXX XXXX XXXX	PC ← X	if AC = 0
JC X	1011 1XXX XXXX XXXX	PC ← X	if CF = 1
CALL X	1100 0XXX XXXX XXXX	STACK ← PC+1 PC ← X	
JMP X	1101 0XXX XXXX XXXX	PC ← X	
RTS	1101 1000 0000 0000	PC ← STACK	CALL Return
SCC X	1101 1001 0X0X 0XXX	X6 = 1: Cfq = BCLK X6 = 0: Cfq = PH0 X5 = 1: Cpw = BCLK X5 = 0: Cpw = PH0 X,4 = 1: Set P(A) X,4 = 0: Set P(C) X2,1,0=001: Cch = PH10 X2,1,0=010: Cch = PH8 X2,1,0=100: Cch = PH6	
SCA X	1101 1010 00XX 0000	X5: A1-4 Enable (SEF5) X4: C1-4 Enable (SEF4)	
SAD X	1101 1011 00XX XXXX	X5: Enable Cmp. output X4: Latch Data to Cmp. X3=1: CP4(+) = LBR X3=0: CP4(+) = AN4 X2=1: CP1~4(-) = AN4 X2=0: CP1~4(-) = DAC X1: Enable LBR X0: Enable DAC	
SPA X	1101 1100 000X XXXX	X4: Set A4~1 Pull-Low X3~0: Set A4~1 I/O	
SPB X	1101 1101 0000 XXXX	X3~0: Set B4~1 I/O	
SPC X	1101 1110 000X XXXX	X4: Set C4-1 Pull-Low /Low-Level-Hold X3~0: Set C4-1 I/O	
SPD X	1101 1111 0000 XXXX	X3-0: Set D4~1 I/O	
TMS Rx	1110 0000 0XXX XXXX	Timer1 ← Rx, AC	
TMS @HL	1110 0001 0000 0000	Timer1 ← T@HL	
TMSX	X 1110 0010 XXXX XXXX	X7,6=11: Ctm=FREQ X7,6=10: Ctm=PH15 X7,6=01: Ctm=PH3 X7,6=00: Ctm=PH9 X5~0: Set Timer1 Value	
MDA Rx	1110 0011 0XXX XXXX	DAC ← Rx	
TM2 Rx	1110 0100 0XXX XXXX	Timer2 ← Rx, AC	
TM2 @HL	1110 0101 0000 0000	Timer2 ← T@HL	

Instruction	Machine Code	Function	Flag/Remark
TM2X X	1110 011X XXXX XXXX	X8,7,6=111 : Ctm=PH13 X8,7,6=110 : Ctm=PH11 X8,7,6=101 : Ctm=PH7 X8,7,6=000 : Ctm=PH5 X8,7,6=011 : Ctm=FREQ X8,7,6=010 : Ctm=PH15 X8,7,6=001 : Ctm=PH3 X8,7,6=000 : Ctm=PH9 X5~0: Set Timer2 Value	
SHE X	1110 1000 0XXX XXX0	X6: Enable HEF6(RFC) X4: Enable HEF4(TMR2) X3: Enable HEF3(PDV) X2: Enable HEF2(INT) X1: Enable HEF1(TMR1)	
SIE* X	1110 1001 0XXX XXXX	X6: Enable IEF6(RFC) X4: Enable IEF4(TMR2) X3: Enable IEF3(PDV) X2: Enable IEF2(INT) X1: Enable IEF1(TMR1) X0: Enable IEF0(A,CPT)	
PLC X	1110 101X 0XXX XXXX	X8: Reset PH15~11 X6, 4~0: Reset HRF6, 4~0	
SRF X	1110 1100 00XX XXXX	X5: Enable Cx Control X4: Enable Timer2 Control X3: Enable Counter X2: Enable RH Output X1: Enable RT Output X0: Enable RR Output	 ENX EHM ETP ERR
SRE X	1110 1101 X0XX 0000	X6~4: Enable SRF6~4	SRF6 (A Port) SRF5 (HRF2) SRF4 (M Port)
FAST	1110 1110 0000 0000	SCLK: High Speed Clock	
SLOW	1110 1111 0000 0000	SCLK: Low Speed Clock	
SF X	1111 0000 X00X XXXX	X7: Reload Set X4: WDT Enable X3: HALT after EL LIGHT X2: EL LIGHT On X1: BCF Set X0: CF Set	RL1 WDF BCF CF
RF X	1111 0100 X00X 0XXX	X7: Reload Reset X4: WDT Reset X2: EL LIGHT Off X1: BCF Reset X0: CF Reset	RL1 WDF BCF CF
SF2 X	1111 1000 0000 0XXX	X0: Reload Set X1: Dis-ENX Set X2: Close all segments	RL2 DED RSOFF
RF2 X	1111 1001 0000 0XXX	X0: Reload Reset X1: Dis-ENX Reset X2: Release all Segments	RL2 DED RSOFF

Instruction	Machine Code	Function	Flag/Remark
ALM X	1111 101X XXXX XXXX	X8,7,6=111: FREQ X8,7,6=100: DC1 X8,7,6=011: PH3 X8,7,6=010: PH4 X8,7,6=001: PH5 X8,7,6=000: DC0 X5~0←PH15~10	
ELC X	1111 110X XXXX XXXX	X8=1 BCLKX X8=0 PH0 X7,6=11 BCLK/8 X7,6=10 BCLK/4 X7,6=01 BCLK/2 X7,6=00 BCLK X5,4=11 1/1 X5,4=10 1/2 X5,4=01 1/3 X5,4=00 1/4 X3,2=11 PH5 X3,2=10 PH6 X3,2=01 PH7 X3,2=00 PH8 X1,0=11 1/1 X1,0=10 1/2 X1,0=01 1/3 X1,0=00 1/4	ELP – CLK BCLKX ELP – DUTY ELC – CLK ELC – DUTY
HALT	1111 1110 0000 0000	HALT operation	
STOP	1111 1111 0000 0000	STOP operation	

Symbol description

AC:	Accumulator	D:	Immediate data
ACn:	Accumulator bit-n	PC:	Program counter
X:	Address	CF:	Carry flag
Rx:	Memory of address X	Rxn:	Memory bit-n of address X
WDF:	Watchdog timer enable flag	Ry:	Memory of working register Y
HL:	Index register	BCF:	Back-up flag
BCLK:	System clock address	@HL:	Memory of index RAM
IEFn:	Interrupt enable flag	HRFn:	HALT release flag
SRFn:	Stop release enable flag	HEFn:	HALT release enable flag
SCFn:	Start condition flag	Cfq:	Clock source of frequency generator
Cch:	Clock source of chartering detector	Ctm:	Clock source of timer
TMR:	Timer overflow release flag	PDV:	Predivider
SEFn:	Switch enable flag	Lz:	LCD latch
FREQ:	Frequency generator setting value	T@HL:	Memory of index ROM
ADF:	ADC flag	CSF:	Clock source flag
DAC:	Digital-to-analog converter output signal		
LBR:	Low-battery voltage reference	L:	Low address of index
H:	High address of index	RFOVF:	RFC overflow flag
HT@HL:	High nibble of index ROM	LT@HL:	Low nibble of index ROM