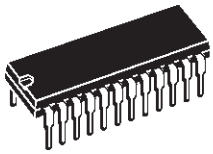
SGS-THOMSON MICROELECTRONICS

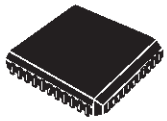
STLC5444

QUAD FEEDER POWER SUPPLY

- SUPPLIES POWER FOR UP TO FOUR DIGITAL TELEPHONE LINES
- CONFORMS TO THE CCITT RECOMMENDATIONS FOR POWER FEED AT THE S OR T REFERENCE POINTS
- SUPPORTS POINT-TO-POINT AND POINT TO MULTIPOINT CONFIGURATIONS
- EACH OF THE FOUR LINES IS INDIVIDUALLY CONTROLLED
- HIGH-VOLTAGE BCD TECHNOLOGY SUPPORTING UP TO -130V
- AUTOMATIC THERMAL SHUTDOWN
- STATUS CONDITION DETECTION (BY MICROPROCESSOR) FOR EACH LINE:
  - Low output voltage
  - Openloop
  - Current overload
  - Thermal overload
  - Normal line condition
- PROGRAMMABLE CURRENT LIMITING
- OUTPUT CURRENT UP TO 120mA



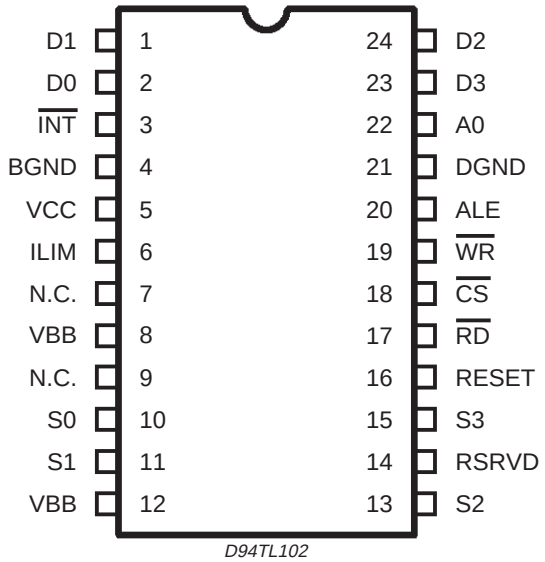
DIP24



PLCC44

ORDERING NUMBERS: STLC5444B1 (DIP24)
STLC5444FN (PLCC44)

DIP24 PIN CONNECTION (Top view)



DESCRIPTION

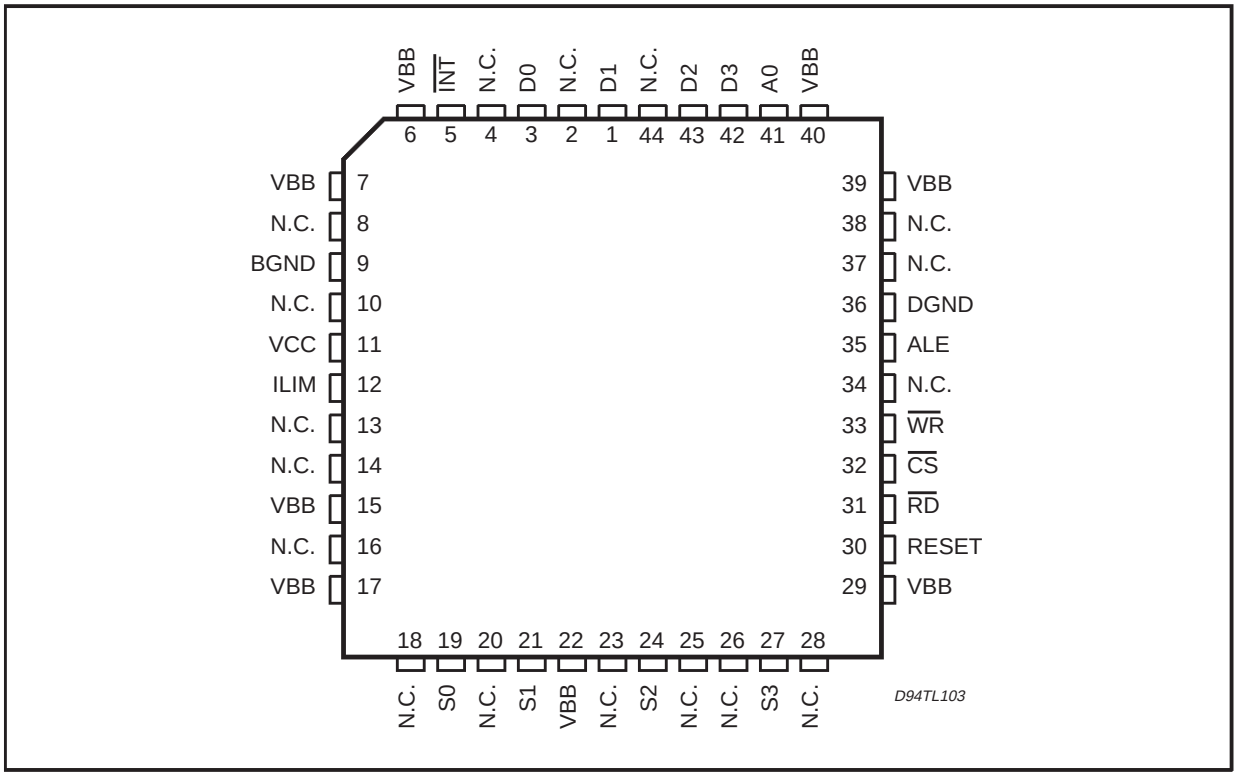
The ISDN Quad Feeder Power Supply (IQFPS) provides a power source for up to four line interfaces. The power source to the device is a local battery or a centralized regulated power supply.
It can operate in point-to-point and point-to-multipoint configurations as far as S interface is concerned.
By the device microprocessor interface, each powered line is individually controlled and monitored.
Therefore, overloads and faults are easy to detect and localize even in a large system.

The status conditions detected by the device on each line that may be read by the microprocessor are :

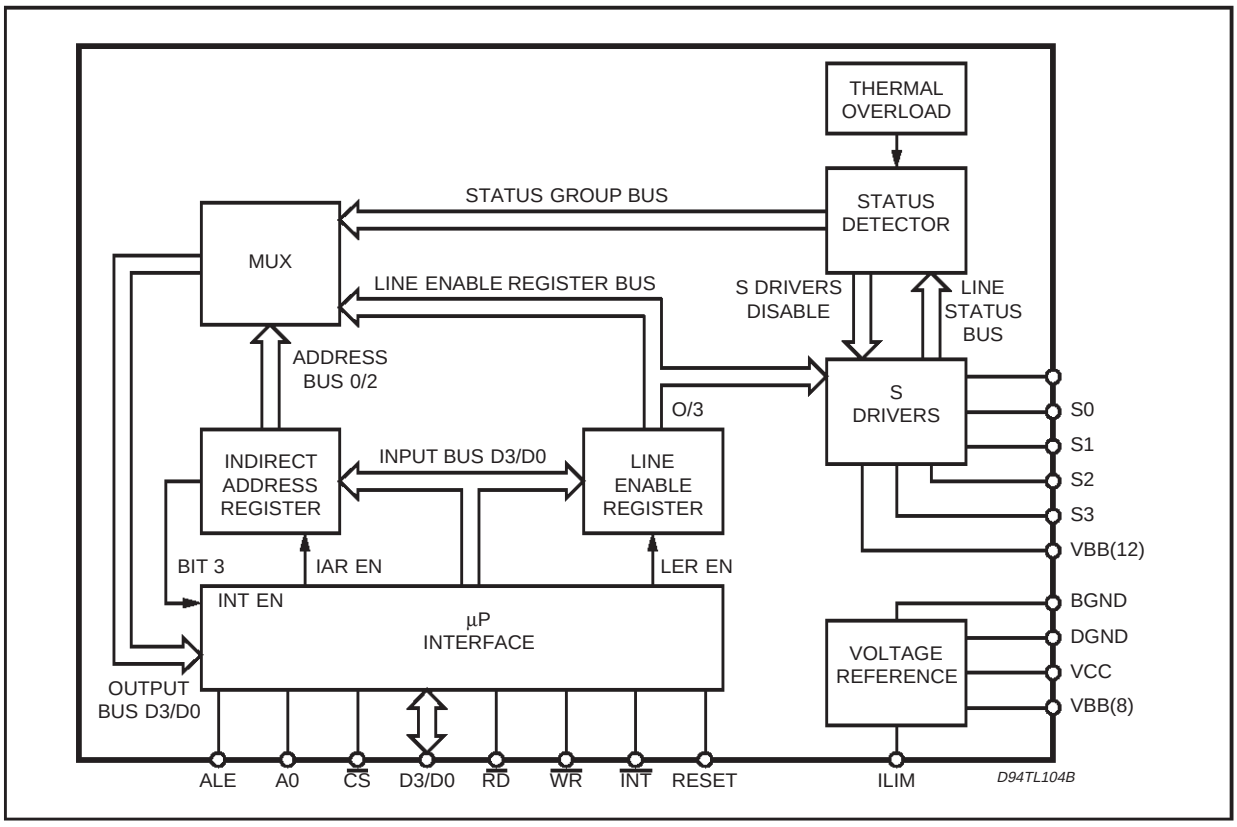
- low output voltage
- openloop
- current overload
- thermal overload
- normal line conditions

A hardware current limiting programmable feature is available.

PLCC44 PIN CONNECTION (Top view)



BLOCK DIAGRAM



PIN DESCRIPTION

Name	N° PLCC	N° DIP	Function
D1	1	1	Bit 1 of the tri state I/O data bus
NC	2,4,8,10, 13,14, 16,18, 20,23, 25,26, 28,34, 37,38,44	7,9	No connection
D0	3	2	Bit 0 of the tri state I/O data bus
$\overline{INT}$	5	3	Active low interrupt output for the µP (open drain)
VBB	6,7 15,17 22,29, 39,40	8,12	Battery supply line (negative battery's terminal)
BGND	9	4	Battery ground line
VCC	11	5	+5V supply line
ILIM	12	6	Current limit programming
S0	19	10	Output of the power switch controller 0
S1	21	11	Output of the power switch controller 1
S2	24	13	Output of the power switch controller 2
RSRVD	–	14	Reserved pin: it must be left floating
S3	27	15	Output of the power switch controller 3
RESET	30	16	Active high reset input
$\overline{RD}$	31	17	Active low read input
$\overline{CS}$	32	18	Active low chip select input
$\overline{WR}$	33	19	Active low write input
ALE	35	20	Active high address latch enable
DGND	36	21	Digital ground
A0	41	22	Address bit for R/W operations on the data bus
D3	42	23	Bit 3 of the I/O tri state data bus
D2	43	24	Bit 2 of the I/O tri state data bus

FUNCTIONAL DESCRIPTION

ADDRESS LINE (Input)

A0 selects source and destination locations for read and write operations on the data bus. A0 must be valid on the falling edge of ALE or during RD and WR if ALE is tied High.

ALE - Address Latch Enable (Input; Active High)

ALE is an input control pulse used to strobe the address on the A0 line into the address latch. This signal is active High to admit the input address. The address is latched on the High-Low transition of ALE. While ALE is High, the address latch is transparent. For an unmultiplexed microprocessor bus, ALE must be tied High.

BGND - Ground Battery

CS - Chip Select (Input; Active Low)

CS must be Low to enable the read or write operations of the device. Data transfer occurs over the D3-D0 lines.

D3-D0 - DATA BUS (Input/Output; Three-State)

The four bidirectional data bus lines are to exchange information with a microprocessor. D0 is the least significant bit and D3 is the most significant bit. A High on the data bus corresponds to a logical 1. These lines act as input when WR and CS are active and as output when RD and CS are active. When CS is inactive, the D3-D0 pins are placed in a high-impedance state.

FUNCTIONAL DESCRIPTION (continued)

DGND - Ground Digital

ILIM - Current Limit Programming (Input)

ILIM programs the current limit of the Output drivers using an external resistor connected between ILIM and VBB. The ILIM pin is 1.25V more positive than VBB. The current limit is 5mA plus 1000 times the current in the external resistor. The programmed current limit applies to each driver.

INT - Interrupt (Output; Open-Collector, Active Low)

INT augments the Microprocessor Interface by generating an interrupt when a Current Overload Detector (COD) occurs. INT is active whenever any bits in the COD register are active. INT is not latched; when the COD register is zero, INT goes inactive (High). INT will also go inactive if the IQFPS automatically disables the S-output driver that caused the interrupt (due to Thermal Overload), or if the microprocessor disables that line via the Line Enable Register (LER). COD interrupts can be masked via the Indirect Address Register (IAR); RESET always disables the INT pin.

RD - Read (Input; Active Low)

The active Low read signal is conditioned by CS and transfers internal information to the data bus. If A0 is a logical 0, logic levels of the Indirect Address Register (IAR) and Thermal Shutdown Status bit will be transferred to D3-D0. If A0 is a logical 1, the data addressed by the IAR will be transferred to D3-D0.

RESET - Reset (Input; Active High)

RESET initialize the registers in the device, leaving the drivers switched off.

S3-S0 - Drivers (Output)

S3-S0 each supply power to one line. The outputs can sink up to 120 mA each. The voltage at the line is connected to VBB through a DMOS switch.

VBB - Battery Voltage (input)

VBB is the internal negative supply voltage. VBB must always be connected to the most negative supply voltage. The MPI Registers will not function properly when the battery power is disconnected, that is, when VBB is floating or grounded. The IQFPS should also be reset if a drastic transient is applied to VBB.

VCC - +5V Power Supply (Input)

WR - Write (Input; Active Low)

The active Low write signal is conditioned by CS and transfers information from the data bus to an internal register selected by A0. If A0 is a logical 1, D3-D0 is written into the Line Enable Register (LER). If A0 is a logical 0, D3-D0 is written into the IAR. LER and IAR are the only two writable registers in the device.

DC CHARACTERISTICS (V_{BB} = -54V; V_{CC} = 5V; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input Voltage High Level		2			V
V_{IL}	Input Voltage Low Level				0.8	V
I_{OH}	High Level Output Current	V_{OH} = 2.4V	400			µA
I_{OL}	Low Level Output Current	V_{OL} = 0.4V	2			mA
I_{IH}	High Level Input Current	V_{IH} = 2V			10	µA
I_{IL}	Low Level Input Current	V_{IL} = 0.8V			60	µA
I_{OZH}	Output Hi-Z Current High	2.4V < V_{OZ} < V_{CC}			10	µA
I_{OZL}	Output Hi-Z Current Low	0V < V_{OZ} < 0.4V			10	µA
I_{CC}	V_{CC} supply Current			1.4	5	mA
C_L	Logic I/O Capacitance			10		pF
V_{SAT}	Saturation Voltage	I_S = 80mA			2	V
R_{on}	Output DMOS Saturation Resistivity	I_S = 80mA			25	Ω
I_{BB}	V_{BB} Supply Current	V_{BB} = -54V, R_{LIM} = 26.6KΩ, Output Disabled		3.2	6	mA
ΔI_{SLIM}	Delta Limit Current vs. Theoretical Programmed Value I_{SLIM}	R_{LIM} = 26.6KΩ, V_{BB} = -96V R_{LIM} = 10.9KΩ, V_{BB} = -54V			±10%	
V_{LVD}	Low Voltage Detector Threshold (relative to V_{BB})	S3 - S0 output active	2.7	3	3.3	V
I_{SOL}	Current Overload Detector Threshold (as % of I_{SLIM})		75		90	%
I_{SOC}	Open Loop Detector Threshold		1.5	3	4	mA
I_{SZ}	Si Leakage Current to ground @ Si disabled	V_{BB} = -110V			100	µA
H_{LVD}	Low Voltage Detector Hysteresis			18	200	mV
H_{OLD}	Open Loop Detector Hysteresis			0.6	1.6	mA
H_{COD}	Current Overload Detector Hysteresis			2.4	4.0	mA
H1	130°C Thermal Detector Hysteresis			10		°C
H2	160°C Thermal Detector Hysteresis			10		°C
T_{H1}	Thermal Overload Recovery Time H1			80		µs

SWITCHING CHARACTERISTICS (V_{BB} = -54V; V_{CC} = 5V; unless otherwise specified)

MICROPROCESSOR READ/WRITE TIMING NON MULTIPLEXED MODE (for references see figure 1a and 2b).

Symbol	Parameter	Min.	Max.	Unit
t_{RLRH}	RD, CS pulse width	260		ns
t_{RHRL}	RD, recovery time T_{amb}: 0 to 70°C	200		ns
	T_{amb}: -40 to 0°C and +70°C to +85°C	220		ns
t_{RLDA}	RD, CS low to data available		260	ns
t_{RHDZ}	RD or CS high to data Z T_{amb}: 0 to 70°C		130	ns
	T_{amb}: -40 to 0°C and +70°C to +85°C		160	ns
t_{ASRL}	Address setup time to READ active	0		ns
t_{AHRH}	Address hold time to READ inactive	0		ns
t_{ASWL}	Address setup time to WRITE active	30		ns
t_{AHWH}	Addess hold time to WRITE inactive	50		ns
t_{ADDA}	Address stable to data available T_{amb}: 0 to 70°C	360		ns
	T_{amb}: -40 to 0°C and +70°C to +85°C	390		ns
t_{WLWH}	WR or CS pulse width	200		ns
t_{WHWL}	Write recovery time	200		ns
t_{DAWH}	Data setup time	100		ns
t_{WHDZ}	Data hold time T_{amb}: 0 to 70°C	20		ns
	T_{amb}: -40 to 0°C and +70°C to +85°C	40		ns
t_{RES}	Reset Pulse with	200		ns

Note: AC timings are tested at 0.8V and 2V with input levels of 0.4V and 2.4V.

SWITCHING CHARACTERISTICS (V_{BB} = -54V; V_{CC} = 5V; unless otherwise specified)

MICROPROCESSOR READ/WRITE TIMING MULTIPLEXED MODE (for references see figure 1 and 2).

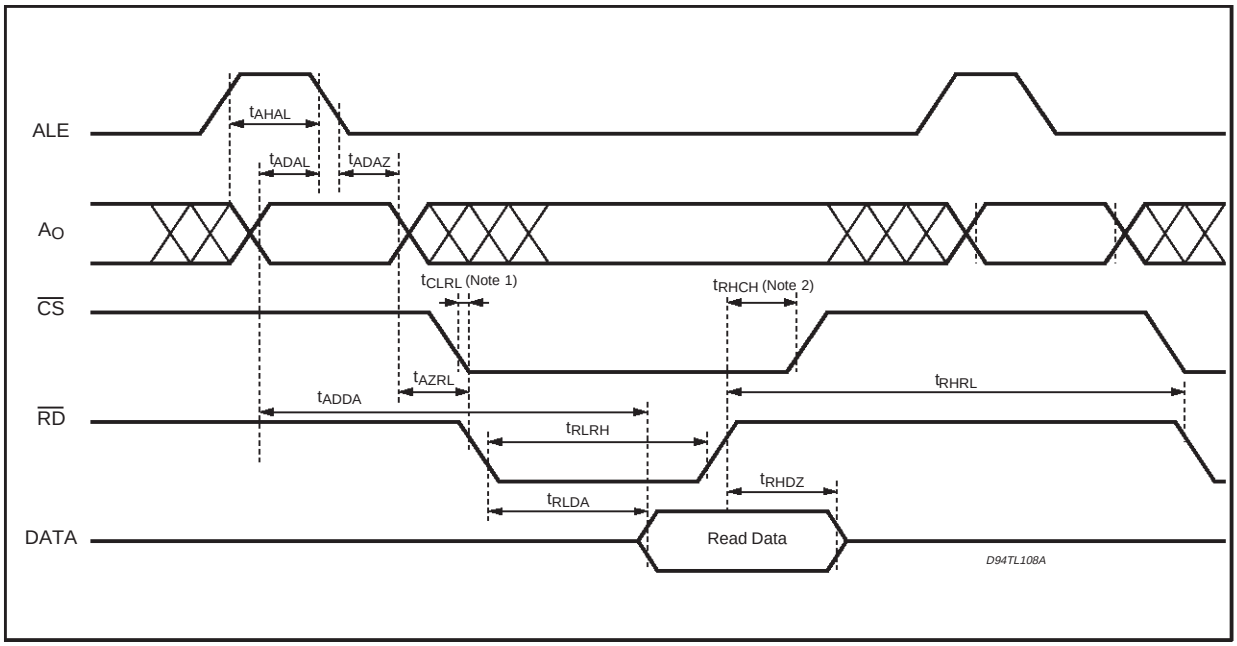
Symbol	Parameter	Min.	Max.	Unit
t_{RLRH}	RD, CS pulse width	260		ns
t_{RHRL}	RD, recovery time T_{amb}: 0 to 70°C	200		ns
	T_{amb}: -40 to 0°C and +70°C to +85°C	220		ns
t_{RLDA}	RD, CS low to data available		260	ns
t_{RHDZ}	RD or CS high to data Z T_{amb}: 0 to 70°C		130	ns
	T_{amb}: -40 to 0°C and +70°C to +85°C		160	ns
t_{AHAL}	ALE pulse width	100		ns
t_{ADAL}	Address setup time	60		ns
t_{ADAZ}	Address hold time	50		ns
t_{AZRL}	Address Z to $\overline{RD}$ low	0		ns
t_{AZWL}	Address Z to $\overline{WR}$ Low	0		ns
t_{ADDA}	Address stable to data available T_{amb}: 0 to 70°C	360		ns
	T_{amb}: -40 to 0°C and +70°C to +85°C	390		ns
t_{WLWH}	WR or CS pulse width	200		ns
t_{WHWL}	Write recovery time	200		ns
t_{DAWH}	Data setup time	100		ns
t_{WHDZ}	Data hold time T_{amb}: 0 to 70°C	20		ns
	T_{amb}: -40 to 0°C and +70°C to +85°C	40		ns
t_{RES}	Reset Pulse with	200		ns

Note: AC timings are tested at 0.8V and 2V with input levels of 0.4V and 2.4V.

Si Timing (at 10% of final value)

Symbol	Parameter	Test condition	Typ.	Max.	Unit
t_{EN}	Si output enable time (from LER)	R_{LOAD} = 3kΩ	2	5	µs
t_{DIS}	Si output disable time (from LER or RESET)		3	6	µs

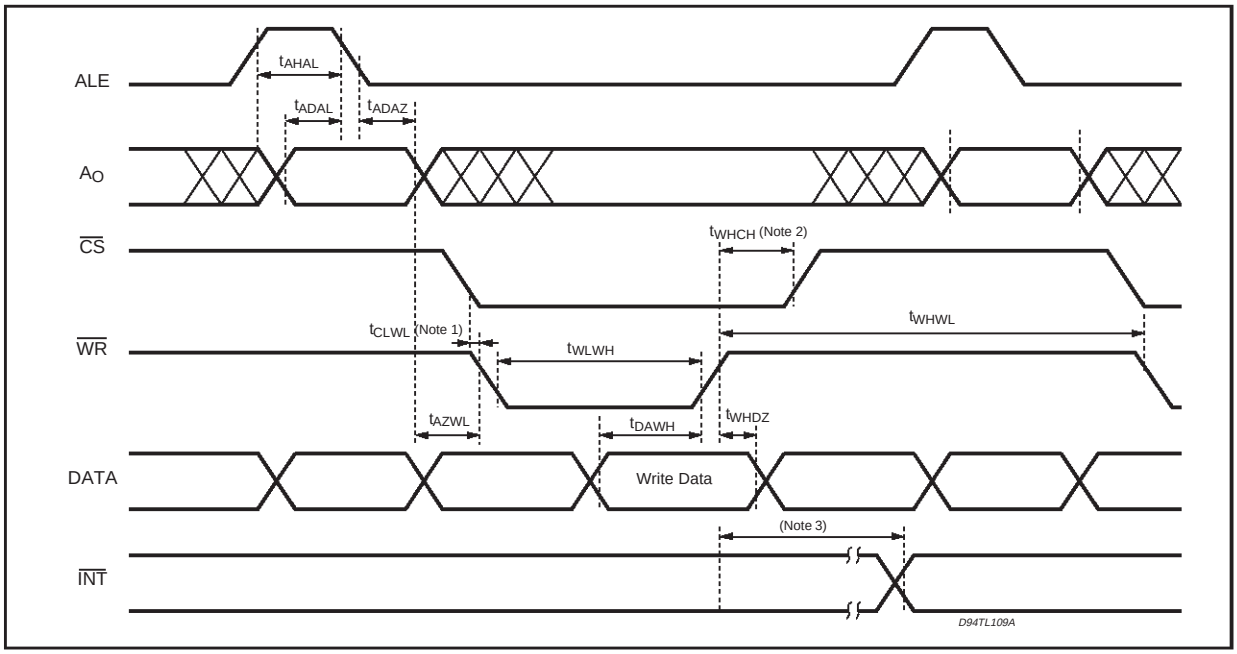
Figure 1: Microprocessor Read Timing.



Notes:
1 - If t_{CLRL} is negative, t_{RHRL}, t_{RLRH}, t_{AZRL}, and t_{RLDA} are measured from $\overline{CS}$ rather than $\overline{RD}$.
2 - If t_{RHCH} is negative, t_{RHRL}, t_{RLRH} and t_{RHDZ} are measured from $\overline{CS}$ rather than $\overline{RD}$.

When a read from the LER immediately follows a write to the LER a minimum of 1 µs is required between these operations.

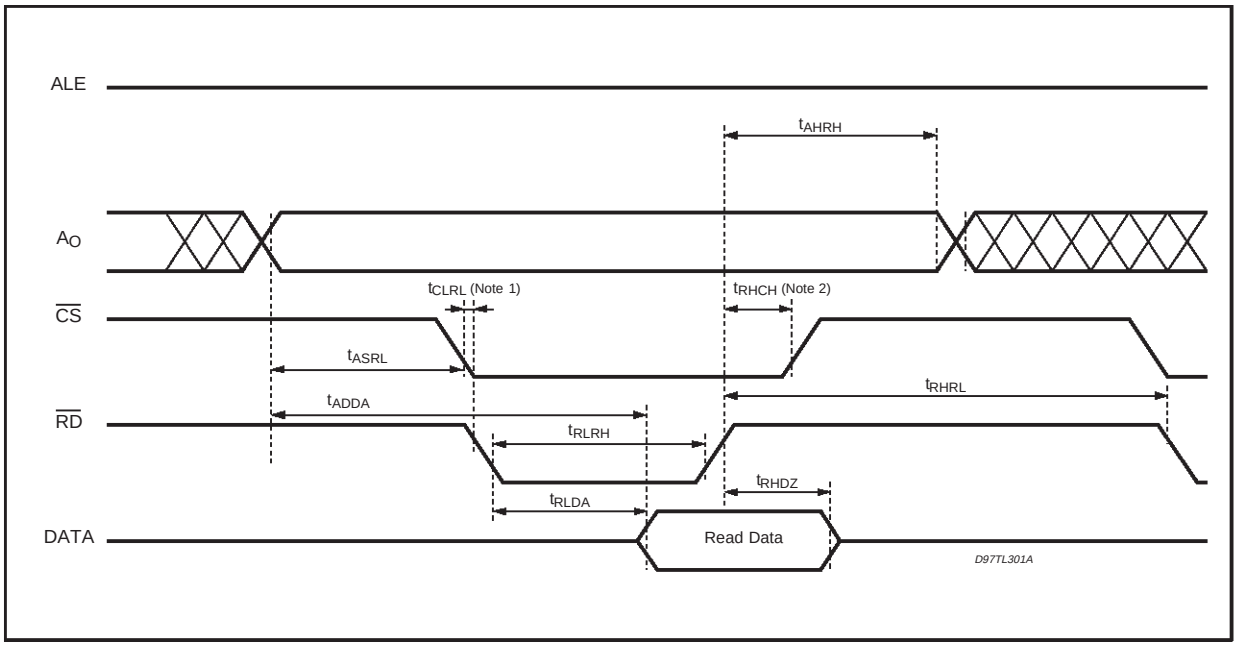
Figure 2: Microprocessor Write Timing.



Notes:
1 - If t_{CLWL} is negative t_{WHWL} and t_{WLWH} are measured from $\overline{CS}$ rather than $\overline{WR}$.
2 - If t_{WHCH} is negative, t_{WHWL}, t_{WLWH}, t_{DAWH} and t_{WHDZ} are measured from $\overline{CS}$ rather than $\overline{WR}$.

The propagation delay from the writing of the T/I bit to the effect on the $\overline{INT}$ pin is approximately 1µs for both mask and enable operations.

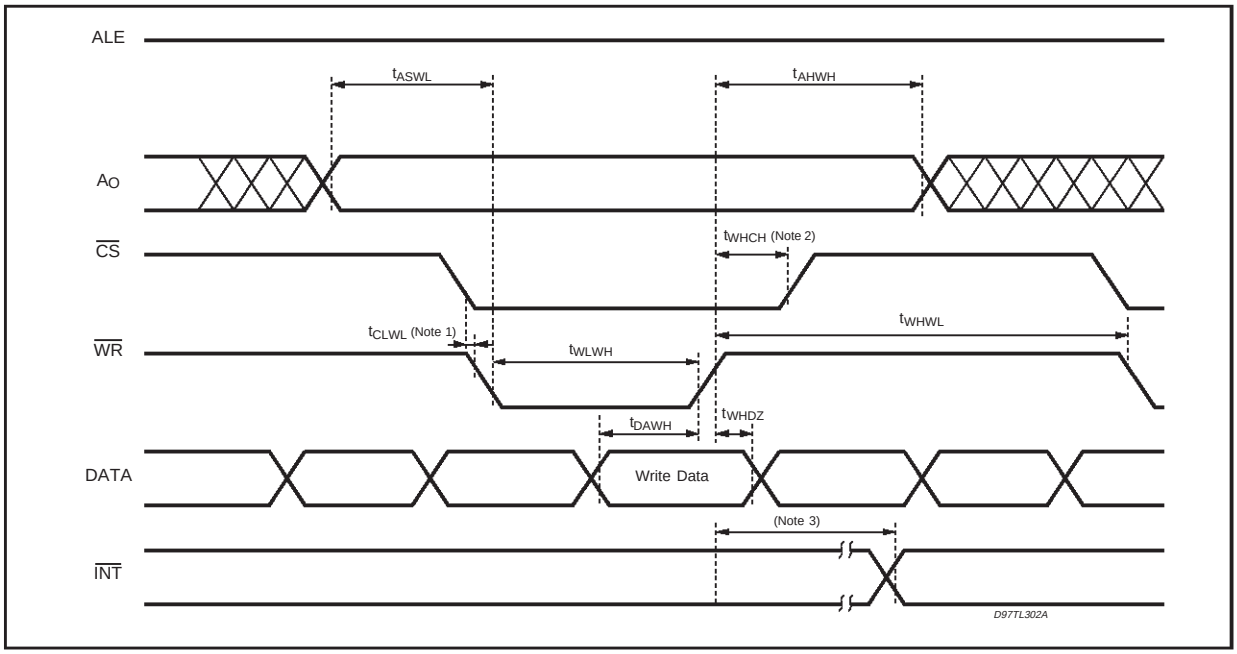
Figure 1a: Microprocessor Read Timing non multiplexed mode.



Notes:
1 - If t_{CLRL} is negative, t_{RHRL}, t_{RLRH}, t_{AZRL}, and t_{RLDA} are measured from $\overline{CS}$ rather than $\overline{RD}$.
2 - If t_{RHCH} is negative, t_{RHRL}, t_{RLRH} and t_{RHDZ} are measured from $\overline{CS}$ rather than $\overline{RD}$.

When a read from the LER immediately follows a write to the LER a minimum of 1 µs is required between these operations.

Figure 2a: Microprocessor Write Timing non multiplexed mode.



Notes:
1 - If t_{CLWL} is negative t_{WHWL} and t_{WLWH} are measured from $\overline{CS}$ rather than $\overline{WR}$.
2 - If t_{WHCH} is negative, t_{WHWL}, t_{WLWH}, t_{DAWH} and t_{WHDZ} are measured from $\overline{CS}$ rather than $\overline{WR}$.

The propagation delay from the writing of the T/I bit to the effect on the $\overline{INT}$ pin is approximately 1µs for both mask and enable operations.

OPERATIVE DESCRIPTION.

Initialization

The device is initialized by the RESET pin. In this state the analog drivers are switched off, the Indirect Address Register (IAR) is cleared, and the internally latched address A0 is cleared.

Power at Output drivers

The voltage at the Output drivers is approximately V_{BB} (more precisely: V_{BB} - V_{SAT}).

Analog Section

The analog section consists of four line drivers, which are DMOS transistor switches capable of sinking up to 120 mA each. The power to the drivers is derived from the negative supply voltage (V_{BB}). The output voltage to each line is slaved to V_{BB}, and the voltage drop in each driver is approximately 1.5V.

Line driver protection is provided through the integration of current limit and over-temperature shut-off. The current limit is hardware-programmable via an external resistor (RLIM) connected between ILIM and V_{BB}.

The output limit is : 5mA + 1000 x 1.25V/RLIM.

This 1000 x gain makes the ILIM pin susceptible to external noise, care should be taken to connect RLIM as close as possible to the component.

The thermal shut-off is internally set at approximately 160°C.

At this temperature all the drivers are unconditionally switched off. However, at approximately 130°C, only the drivers that are in the current-overload condition will be turned off.

Status detectors, associated with each of the line drivers, monitor the load conditions on each line by comparing an electrical parameter (e.g., current and voltage at the line) with reference level. The output of each detector can be read by the microprocessor. In addition to these status detectors, the temperature of the device is monitored via integrated temperature detectors. The detectors respond at approximately 130°C and 160°C, as defined above, and the 160°C detector can be monitored by the microprocessor via the MPI. The status detectors provide the following information from each of the lines (all detectors have built-in hysteresis) :

***) Low Output Voltage Detection**
The low-output-voltage status bit becomes active when the voltage across the output DMOS transistor exceeds the proper voltage threshold (V_{LVD}).

***) Open Loop Detection**
The open-loop status bit becomes active when the current on the line drops below a minimum value.

***) Current Overload Detection**
The current-overload status bits become active when the current on the line nears the current limit. These bits active the INT output if COD interrupts are enabled via the IAR Register.

***) Thermal Overload Detection**
If the device temperature reaches 130°C, then all the line drivers in the current-overload condition will be switched off and the corresponding bits in the Thermal Overload Register will be activated. If the device temperature increases to 160°C, all the line drivers will be turned off, and all the bits in the Thermal Overload Register will be activated.

The T-bit will also be set, and it can be read along with the Indirect Address Register (IAR) to indicate that all the drivers have been turned off. To initialize any of the bits in the Thermal Overload Register, the microprocessor must first turn off the line drivers that must not be reactivated until the T-bit in the address register is cleared by the temperature detector in the device.

MPI Section

The MPI allows the user to access the detectors defined in the analog section. The line driver's status bits are grouped by function. Bits 3-0 of the detectors correspond to lines 3-0, respectively.

The status group are :

- Low Voltage Detector (LVD)
- Open Loop Detector (OLD)
- Current Overload Detector (COD)
- Thermal Overload Register (TOR)

The data is not latched in these status groups except in the TOR.

Thus, the user should filter (multiple samples) the received data to ensure its integrity. There are two other registers in the MPI: the Indirect Address Register (IAR), and Line Enable Register (LER).

The IAR contains 3 bits that address the desired status group or the LER. The IAR is read along with the T-bit defined in the analog section. The microprocessor can read the IAR to check the validity of the address. A 1us delay is required between a write to the LER register, followed by a Read of the same register. Subsequent reads of the LER do not have this constraint.

The LER is used to enable or disable the individual line drivers. The line drivers will only become active if the corresponding bit in the TOR is inactive. The LER is a read/write register.

The MPI is the interface containing the following pins :

D3-D0	Bidirectional	Data Bus
A0	Input	Address Line
ALE	Input	Address Latch Enable
$\overline{RD}$	Input	Read Enable
$\overline{WR}$	Input	Write Enable
$\overline{CS}$	Input	Chip Select
$\overline{INT}$	Output	COD Interrupt
RESET	Input	Reset pin

The 4-bit bidirectional data bus (D3-D0) is used to communicate with the registers. Access to the registers is controlled by CS, RD, WR, ALE, and A0 as shown below. A read or write cycle must be preceded by a valid A0. A0 is latched internally in a transparent latch by ALE. The selection of the status group or the LER is determined by the content of the IAR.

The truth table for the MPI control is shown below :

CS	RD	WR	A0	
0	1	0	0	Write IAR (T bit is read only)
0	0	1	0	Read IAR and T bit
0	1	0	1	Write LER
0	0	1	1	Read status groups or LER
1	X	X	X	No access

Indirect Address Register (IAR) and T/I Bit

The IAR is 3 bits wide and accessible through the data port, D2-D0. The content of the Indirect Address Register (IAR2-IARO) determines the selection of the status groups or the LER. The thermal overload bit T/I is read and written at the same time as IAR and occupies D3.

This register has the following format :

Bit	Symbol	
0	IARO	Bit 0 of the IAR
1	IAR1	Bit 1 of the IAR
2	IAR2	Bit 2 of the IAR
3	T/I	T bit: (Read only) Logical 0: temperature normal (default value) Logical 1: temperature above 160°C (all drivers shut off) I bit : (write only) Logical 0: INT pin disabled Logical 1: COD interrupts enabled via INT pin‘

IAR2-IAR0 address the status groups and the LER as shown below:

IAR2	IAR1	IAR0	Select
0	0	0	LVD
0	0	1	OLD
0	1	0	COD
0	1	1	LEC
1	0	0	RESERVED
1	0	1	RESERVED
1	1	0	LER
1	1	1	TOR

The contents and format of the status groups and the LER are as follows :

LVD:

Bit	Logical 1	Logical 0 (default value)
0	O0 low voltage	O0 voltage normal
1	O1 low voltage	O1 voltage normal
2	O2 low voltage	O2 voltage normal
3	O3 low voltage	O3 voltage normal

The Low Voltage Detector (LVD) indicates the voltage level on the output lines, even when the lines are disabled. The low-voltage condition becomes active (logical 1) if the output reaches the Low Voltage Threshold (VLVD).

LEC:

Bit	Logical 1	Logical 0
0	SWITCH ON	SWITCH OFF
1	SWITCH ON	SWITCH OFF
2	SWITCH ON	SWITCH OFF
3	SWITCH ON	SWITCH OFF

The Line Enable Command (LEC) indicates the status of the DMOS SWITCH OUTPUT.

OLD:

Bit	Logical 1	Logical 0 (default value)
0	O0 open loop	O0 current normal
1	O1 open loop	O1 current normal
2	O2 open loop	O2 current normal
3	O3 open loop	O3 current normal

The Open Loop Detector (OLD) indicates the open-loop condition on the output lines. The open-loop condition becomes active (logical 1) if the current on the line drops below the threshold value ISOC.

COD:

Bit	Logical 1	Logical 0 (default value)
0	O0 current overload	O0 current normal
1	O1 current overload	O1 current normal
2	O2 current overload	O2 current normal
3	O3 current overload	O3 current normal

The Current Overload Detector (COD) indicates the current-overload condition on the output lines. The overload condition becomes active (logical 1) if the output current approaches the value programmed by an external resistor between ILIM and VBB.

TOR :

Bit	Logical 1 (default value)	Logical 0
0	O0 operational	O0 off
1	O1 operational	O1 off
2	O2 operational	O2 off
3	O3 operational	O3 off

The Thermal Overload Register (TOR) contains the overload status of the output line drivers. If the device temperature reaches 130^{o}C, then the output line drivers that are in the current-overload condition will be switched off. The corresponding bits in the TOR will be set to a logical 0. To initialize any of the bits in the TOR, the microprocessor must first turn off the output line drivers via the LER. However, the TOR bits cannot be deactivated if the 160^{o}C detector is active. The µp may re-enable the output drivers via the LER after the TOR condition is removed. The TOR is a read-only register.

LER :

Bit	Logical 1	Logical 0 (default value)
0	O0 on	O0 off
1	O1 on	O1 off
2	O2 on	O2 off
3	O3 on	O3 off

The Line Enable Register (LER) is used to enable or disable the individual output line drivers. The output line will only become active if the corresponding bit in the TOR is set to a logical 1. The LER can be written directly and read indirectly.

ABSOLUTE MAXIMUM RATINGS (T_A = 0°C to 70°C)

Parameter	Value
Voltage from Digital Input to DGND	-0.4V to V_{CC}
Voltage from V_{CC} to DGND	-0.4V to +7V
Voltage from V_{BB} to DGND	-130V to +0.4V
100ns Pulse voltage from Si to DGND (See Notes)	-130V to +2V
Voltage from BGND to DGND	+0.5V, -3V
Storage Temperature	T = -60°C to +150°C

Note : Si stands for O0, O1, O2 or O3 outputs.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol1	Min.	Max.	Units
(*) Ambient Temperature for standard type	T_A	0	70	°C
for ext. temperature type	T_A	-40	85	°C
Supply Voltage	V_{CC}	4.75	5.25	V
	V_{BB}	-115	-38	V
	DGND	0	0	V
	BGND	-3	+0.5	V
Programmed Limiting Current	I_{SLIM}		120	mA

Note: The test condition is specified with a diode in series with V_{BB}.
(*): Specifications in this data sheet are guaranteed by testing from 0°C to +70°C. For extended temperature range types, performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

ORDERING TYPES:

STLC5444B1, PDIP24 package: 0 to 70°C Temperature range.
STLC5444FN, PLCC44 package: 0 to 70°C Temperature range.
STLC5444B1-X, PDIP24 package: -40 to 85°C Temperature range.
STLC5444FN-X, PLCC44 package: -40 to 85°C Temperature range.

APPLICATION HINT

In the Absolute Maximum Ratings table it is specified that the voltage applied on the $-V_{bat}$ pin should never exceed by more than 0.4V the voltage applied on the Ground pin.

As long as the external circuitry assures compliance with the above, no more considerations are needed.

In some cases however it may be not possible to exclude that conditions may occur (hot insertion, power supply transients, etc.) where the negative supply has a transient overshoot above ground voltage. Then a protection circuitry that clamps such overshoot can add to the equipment reliability. Such protection can be designed taking into considerations that typically the devices behave as follows:

- if the V_{bat} pin is not connected, and the other pins are normally biased, the chip generates on it an open circuit voltage of +420mV.
- if all the other pins are normally biased and the $-V_{bat}$ pin forced at +600mV, a current of 10mA flows into it. At the same time from +5V a current of 4mA is absorbed (this low current from +5V simply means that no parasitic latch-ups are triggered inside the chip). No deterioration of the device occurs.
- if all the other pins are normally biased, and the $-V_{bat}$ pin is forced at +1.5V for a transient period, no deterioration of the device occurs. Transient period can be considered any time interval that lasts for less than 10µs and is not repeated more than 5000 times during the device lifetime.

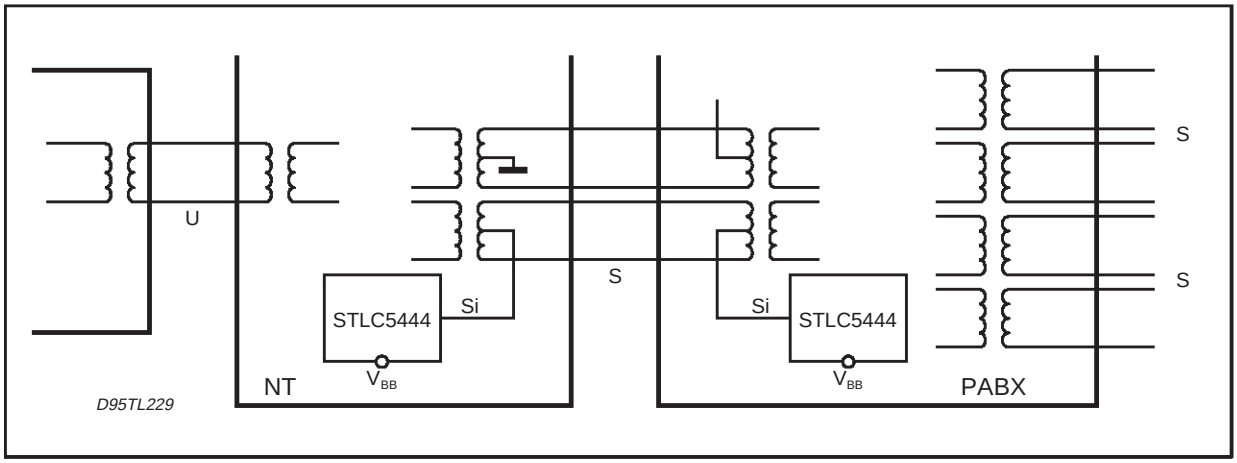
COUNTER FEEDING

It is possible that, in some applications, a communication channel that the STLC5444 feeds, is also biased at the other end by another feeding device.

What considerations apply to the STLC5444 in this case?

Let's use a generic example for reference (see Fig. 3)

Figure 3: Typical PABX connection.

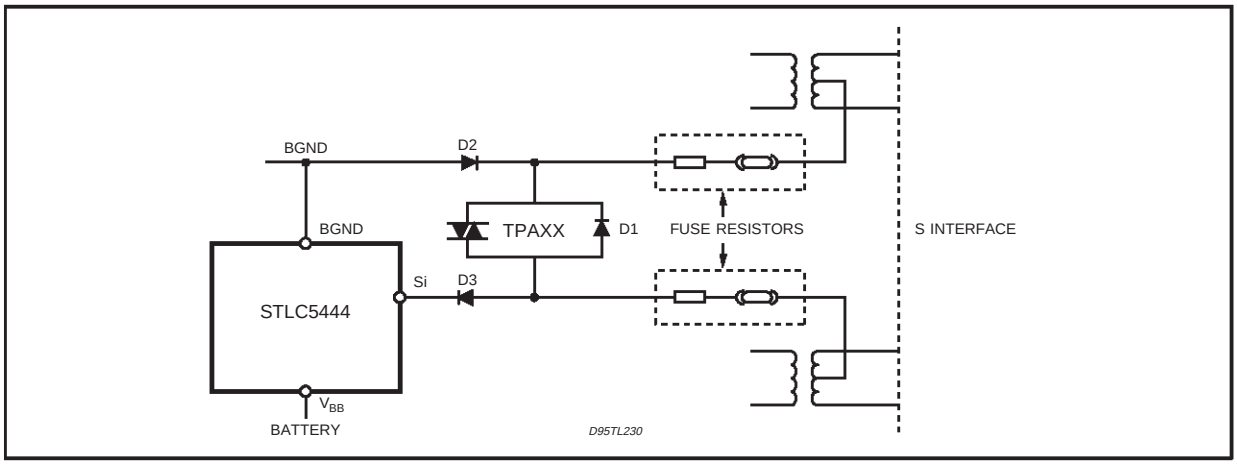


A PABX with S-interfaces may have some of them connected to Terminal Equipments, and one to the S-interface of a Nertwork Termination. The S-interface of the PABX connected to the NT has one channel of the STLC5444 available for feeding. It will be programmed in the "OFF" state to avoid interference with the feeding coming from the NT (of course the feeding coming from the NT will not be loaded by this PABX connection).

The following considerations are relevant in the above example:

1) The VBB of the STLC5444 in the PABX must be equal or more negative than the feeding voltage coming from the NT (unless decoupling diodes are externally provided - see 4)
2) The STLC5444 channel of the PABX must be programmed OFF.
3) In the channel of the STLC5444 on the PABX side, the only effect will be on the relevant LVD bit that will be set to 1 if the feeding voltage coming from the NT is 3V more positive than the local VBB. No interrupts or alarms are generated.
4) It is good common practice to provide every S-interface with protection circuitry against transient overvoltages (see Fig. 4). This includes a diode in series with each Si pin of the STLC5444. If this is the case, absolute levels of local VBB and NT feeding are no concern at all. (If such diodes are not present, care must be paid to the power supply of the PABX, and to the connected circuits. When the PABX supply is OFF, the NT feeding will find a connection through the relevant channel of the STLC5444 to the VBB point).

Figure 4: Protection of the STLC5444 against overvoltage.



NOTE

Possible effect on the device of a Vbat variation

Be aware that a variation of Vbat during operation, when the switches are on can cause anomalous behaviour. To avoid that a turn-off occurs the variation should have a rise time equal or lower than 20V/µs (fig. 5), and a fall time equal or lower than 2.0V/µs (fig.6).

Figure 5: Typical rise time behaviour.

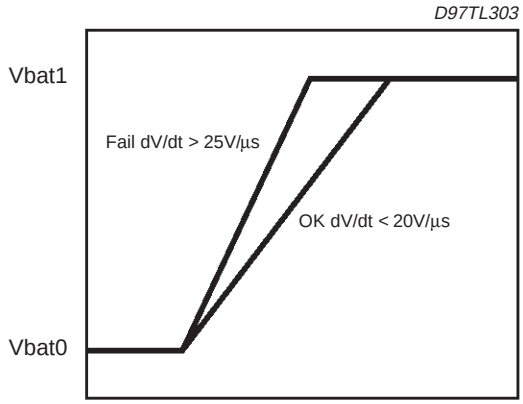
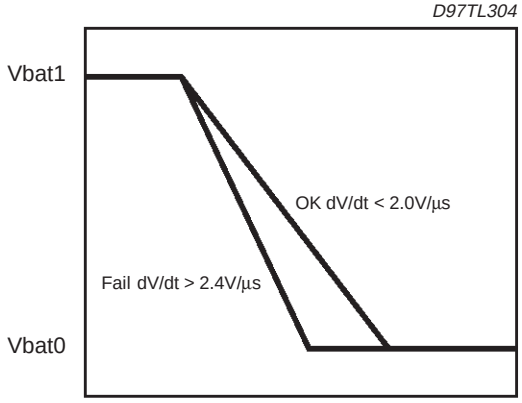
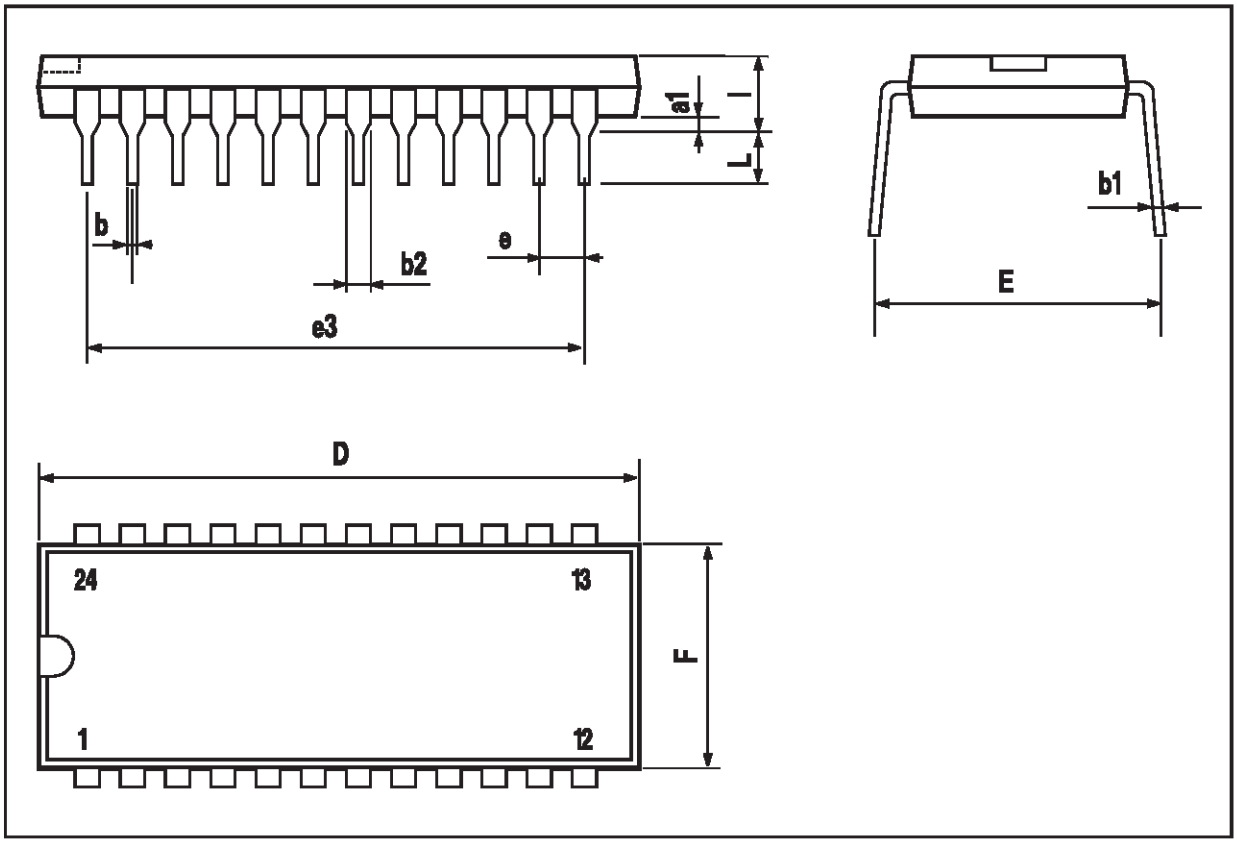


Figure 6: Typical fall time behaviour.



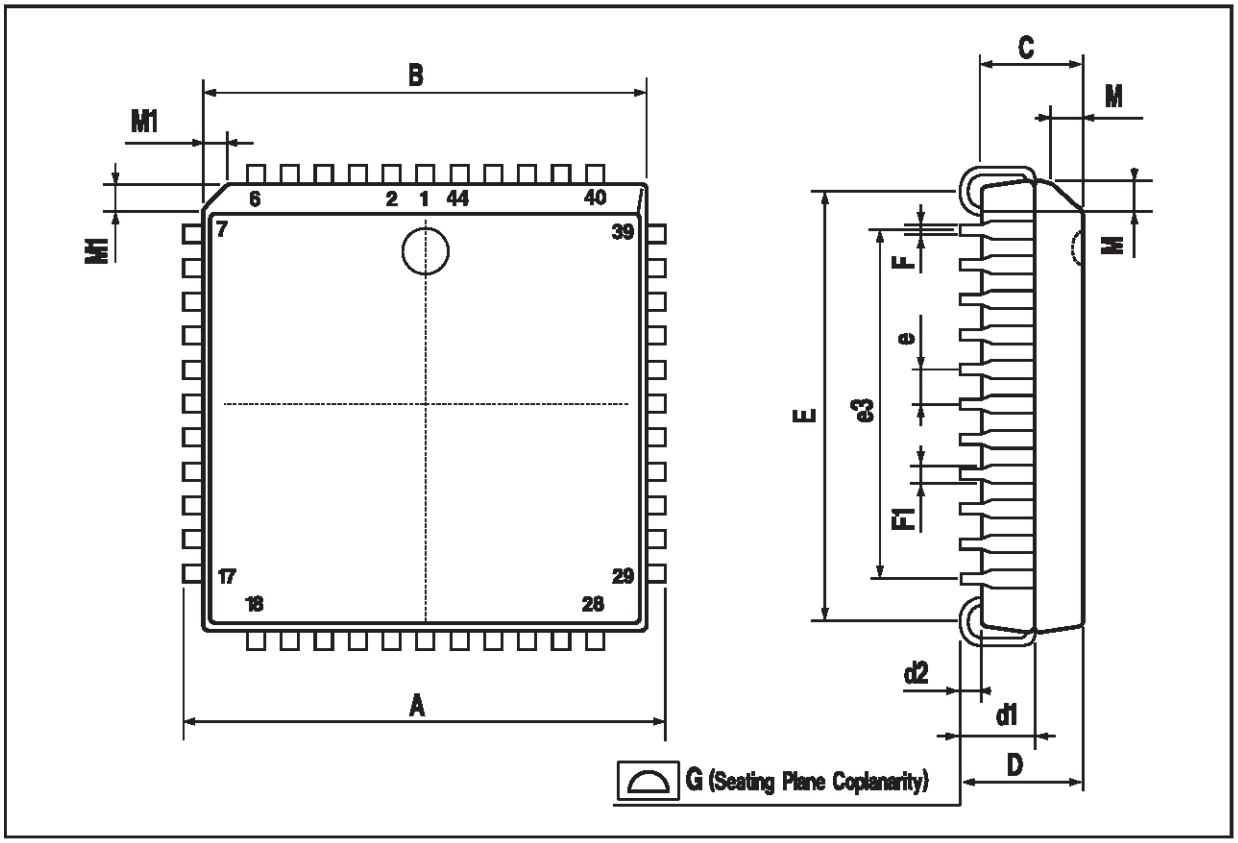
DIP24 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	



PLCC44 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	



ESD - The SGS-THOMSON Internal Quality Standards set a target of 2 KV that each pin of the device should withstand in a series of tests based on the Human Body Model (MIL-STD 883 Method 3015): with C = 100pF; R = 1500Ω and performing 3 pulses for each pin versus V_{CC} and GND.

Device characterization showed that, in front of the SGS-THOMSON Internaly Quality Standards, all pins of STLC5444 withstand at least 1000V.

The above points are not expected to represent a pratical limit for the correct device utilization nor for its reliability in the field. Nonetheless they must be mentionned in connection with the applicability of the different SURE 6 requirements to STLC5444.