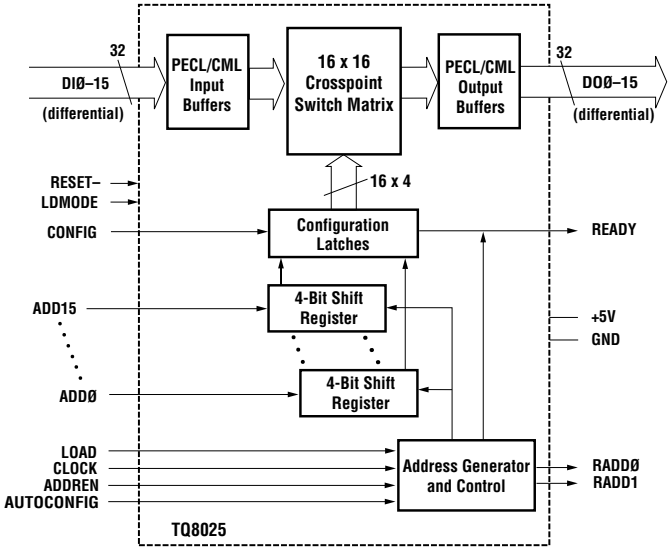


The TQ8025 is a non-blocking 16 x 16 digital crosspoint switch capable of data rates greater than 2.5 gigabits per second per port. With a fully differential internal data path and PECL/CML I/O, the TQ8025 offers an extremely high data rate with exceptional signal fidelity. The use of fully differential logic results in low crosstalk, jitter, and signal skew. The TQ8025 is ideally suited for digital video, data communications, telecommunication switching, and cross-connect applications.

The non-blocking architecture uses 16 fully independent 16:1 multiplexers which allow each output port to be independently programmed to any input port. The TQ8025 offers two programming options: a flexible port-by-port option, and a fast configuration option.

Using the fast configuration option, all 16 switch ports are programmed within 80ns by serially loading four 16-bit input port selection words. Two output pins (RADD0,1) are provided to drive an external RAM (n x 4 x 16 bits) used to store the switch configuration. An Autoconfigure option automatically transfers the new configurations into the switch core. Autoconfiguration occurs after the last input selection word is clocked into the programming registers.

Data integrity is maintained on all unchanged data paths for both the port-by-port and fast configuration options.

TQ8025

PRELIMINARY DATA SHEET

2.5 Gigabit/sec 16x16 Digital Crosspoint Switch

SWITCHING PRODUCTS

Features

- *16 PECL/CML fully differential (back-terminated) outputs*
- *>2.5 Gb/s data bandwidth per channel*
- *>40 Gb/s aggregate bandwidth*
- *Non-blocking architecture*
- *80 ns configuration time*
- *Autonomous control of external RAM for configuration data*
- *Low jitter and signal skew*
- *±100 ps delay match (one input to all outputs)*
- *Fully differential data path*
- *132-pin MLC package with heat spreader*

Applications

- *SONET OC-48 data path*
- *Double-speed Fibre Channel*
- *Hubs and routers*
- *High-definition video switching*
- *Parallel processing*

Specifications

Table 1. Absolute Maximum Ratings [4]

Storage temperature	T_{STORE}	–65 °C to +150 °C
Junction temperature	T_{CH}	150 °C
Case temperature with bias [1]	T_C	T_J = 150 °C
Supply voltage [2]	V_{CC}	0 V to +7.0 V
Voltage to any input [2]	V_{IN}	–0.5 V to V_{CC} + 0.5 V
Voltage to any output [2]	V_{OUT}	–0.5 V to V_{CC} + 0.5 V
Current to any input [2]	I_{IN}	–1.0 mA to +1.0 mA
Current from any output [2]	I_{OUT}	40 mA
Power dissipation of output [3]	P_{OUT}	50 mW

Notes: 1. T_C is measured at the case top.
2. All voltages are measeured with respect to GND 0V and are continuous.
3. $P_{OUT} = (V_{CC} – V_{OUT}) \times I_{OUT}$.
4. Absolute maximum ratings in this table are those beyond which the device's performance may be impaired and/or permanent damage may occur.

Table 2. Recommended Operating Conditions [4]

Symbol	***Parameter***	***Min***	***Typ***	***Max***	***Units***	***Notes***
T_C	Case Operating Temperature	0	—	85	°C	1, 3
V_{CC}	Supply Voltage	4.75	—	5.25	V	
V_{TT}	Load Termination Supply Voltage		V_{CC} – 2.0		V	2
I_{CC}	Current Positive Supply	—	—	2.1	A	
R_{LOAD}	Output Termination Load Resistance		50		Ω	2
Θ_{JC}	Thermal Resistance Channel to Case			4.5	°C/W	

Notes: 1. T_C measured at case top. Use of adequate heatsink is required.
2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions.
3. Contact the Factory for extended temperature range applications.
4. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified.

Table 3. DC Characteristics — CML I/O[5]

Symbol	*Description*	*Test Conditions*	*Min*	*Nom*	*Max*	*Unit*
V_{COM}	Common mode voltage	(Note 1)	V_{CC} – 600	—	V_{CC}	mV
V_{DIFF}	Differential voltage	(Note 1)	400	—	1200	mV
V_{IH}	Input HIGH voltage	(Note 2)		—	V_{CC}	mV
V_{IL}	Input LOW voltage		V_{CC} – 1100	—		mV
V_{OH}	Output HIGH voltage	(Note 3)	V_{CC} – 100	—	V_{CC}	mV
V_{OL}	Output LOW voltage	(Note 3)	V_{CC} – 1100	—	V_{CC} – 600	mV
I_{OH}	Output HIGH current	(Note 3, 4)	20	23	30	mA
I_{OL}	Output LOW current	(Note 3, 4)	0	5	8	mA

Table 4. DC Characteristics — PECL I/O[5]

Symbol	*Description*	*Test Conditions*	*Min*	*Nom*	*Max*	*Unit*
V_{COM}	Common mode voltage	(Note 1)	V_{CC} – 1500	—	V_{CC} – 1100	mV
V_{DIFF}	Differential voltage	(Note 1)	400	—	1200	mV
V_{IH}	Input HIGH voltage	(Note 2)		—	V_{CC} – 500	mV
V_{IL}	Input LOW voltage		V_{CC} – 2100	—		mV
V_{OH}	Output HIGH voltage	(Note 3)	V_{CC} – 1100	—	V_{CC} – 600	mV
V_{OL}	Output LOW voltage	(Note 3)	V_{CC} – 2100	—	V_{CC} – 1600	mV
I_{OH}	Output HIGH current	(Note 4)	20	23	30	mA
I_{OL}	Output LOW current	(Note 4)	0	5	8	mA
C_{IN}	Input capacitance		—	—	TBD	pF
C_{OUT}	Output capacitance		—	—	TBD	pF
VESD	ESD breakdown rating	(Note 5)	Class I	—	—	

Table 5. DC Characteristics — TTL I/O[5]

Symbol	*Description*	*Test Conditions*	*Min*	*Nom*	*Max*	*Unit*
V_{IH}	Input HIGH voltage		2.0	—	V_{CC}	V
V_{IL}	Input LOW voltage		0	—	0.8	V
I_{IH}	Input HIGH current	$V_{(IHMAX)}$	—	—	200	uA
I_{IL}	Input LOW current	$V_{(ILMIN)}$	–400	–200	—	uA
V_{OH}	Output HIGH voltage	I_{OH} = 50 mA	2.4	—	V_{CC}	V
V_{OL}	Output LOW voltage	I_{OH} = –20 mA	0	—	0.4	V
C_{IN}	Input capacitance		—	—	TBD	pF
C_{OUT}	Output capacitance		—	—	TBD	pF
VESD	ESD breakdown rating	(Note 5)	Class I	—	—	

Notes (Tables 3, 4, and 5):
1. *Differential inputs.*
2. *V_{REF} = 1300 mV.*
3. *R_{LOAD} = 50 ohms to $V_{TT} = V_{CC} – 2.0$ V.*
4. *Not tested; consistent with V_{OH} and V_{OL} tests.*
5. *Specifications apply over recommended operating ranges.*

SWITCHING PRODUCTS

Table 6. AC Characteristics

Symbol	*Description*	*Test Conditions*	*Min*	*Typ*	*Max*	*Unit*
T_{PW}	D(0:15) minimum pulse width	(Note 1)	360	—	—	ps
$T_{R/F}$	O(0:15) rise/fall time 20-80%	(Note 1)	—	—	150	ps
T_{PD}	D(0:15), O(0:15) delay time	(Note 1)	—	—	2.5	ns
T_{SKEW}	Path delay matching	(Note 1)		300		ps
T_{JITTER}	Jitter	(Note 2)	—	50	—	ps pk–pk

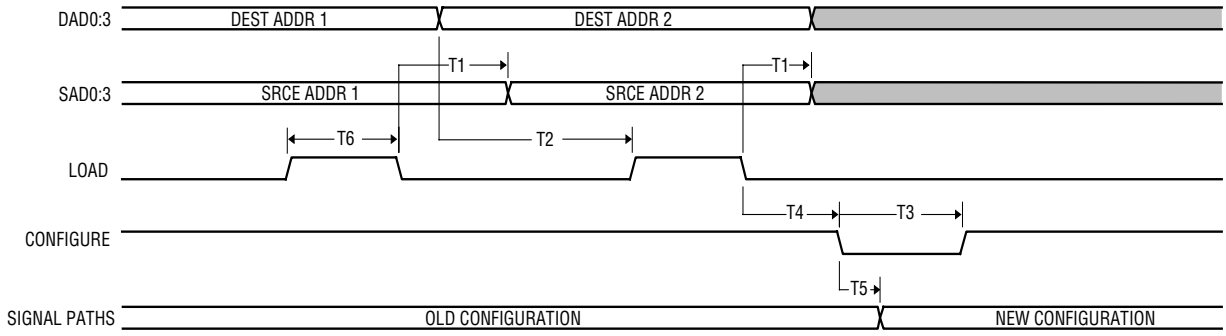
Notes: 1. Minimum V_{OH} to maximum V_{OL} levels.
2. Crossing of (On)—(NOn) measured with $2^{23} – 1$ PRBS, measured over extended time.

Table 7. TQ8025 Timing — Normal Configure Mode [1]

Symbol	*Parameter*	*Min.*	*Max.*	*Units*
T1	Hold LOAD low to SAD0:3, DAD0:3	2		ns
T2	Setup DAD0:3 to LOAD high	0		ns
T3	CONFIGURE pulse low time	10		ns
T4	Setup LOAD low to CONFIGURE low	3		ns
T5	CONFIGURE low to SIGNAL PATHS updated	4		ns
T6	LOAD pulse width high	TBD		ns

Notes: 1. LDMODE = 0; AUTOCONFIG = Don't Care, RESET– = 1, CLOCK = Don't Care.

Figure 1. TQ8025 Timing — Normal Configure Mode



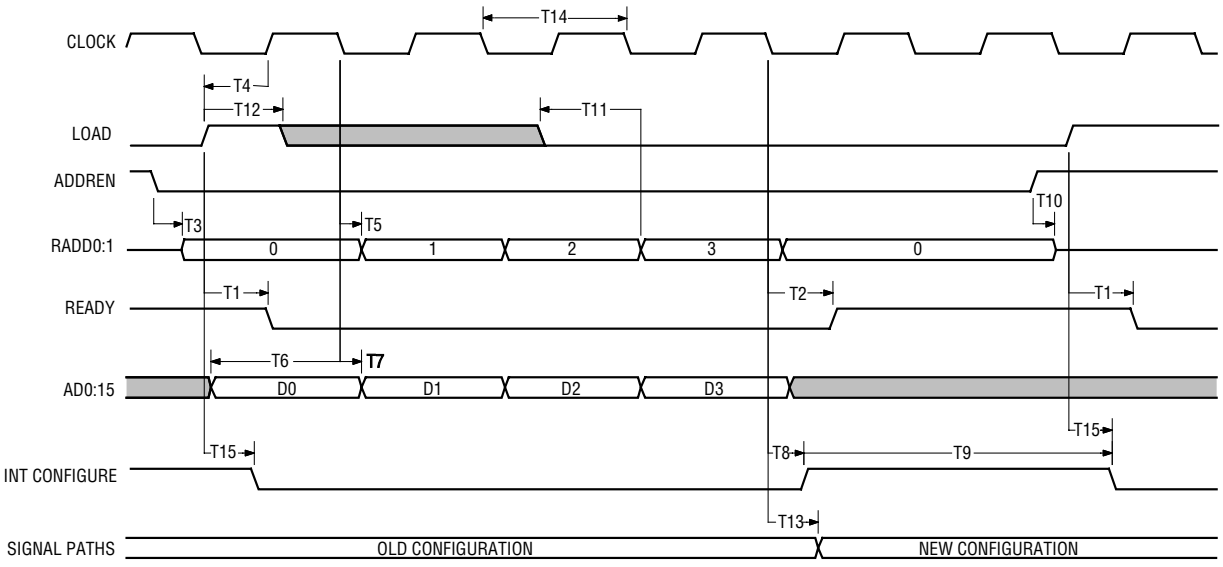
LDMODE=0; AUTOCONFIG = Don't Care, RESET– = 1, CLOCK = Don't Care.

Table 8. TQ8025 Timing — RAM Loading, Auto-Configure Mode [1]

Symbol	*Parameter*	*Min.*	*Max.*	*Units*
T1	LOAD high to READY low	3		ns
T2	CLOCK low to READY high	3		ns
T3	ADDREN low to RADD enabled	3		ns
T4	Setup LOAD high to CLOCK high	4		ns
T5	CLOCK low to RADD increment	2		ns
T6	AD0:15 setup before CLOCK low	0		ns
T7	AD0:15 hold time after CLOCK low	2		ns
T8	CLOCK low to INT CONFIGURE high	2		ns
T9	CONFIGURE low pulse width	10		ns
T10	ADDREN high to RADD tristate	3		ns
T11	LOAD low prior to 3rd CLOCK low	4		ns
T12	LOAD high pulse	TBD		ns
T13	CLOCK low to SIGNAL PATHS updated	4		ns
T14	CLOCK period	20		ns
T15	LOAD high to INT CONFIGURE low	TBD		ns

Notes: 1. LDMODE = 1; AUTOCONFIG = 1, RESET– = 1, CONFIG = 1.

Figure 2. TQ8025 Timing — RAM Loading, Auto-Configure Mode



LDMODE = 1; AUTOCONFIG = 0, RESET– = 1.

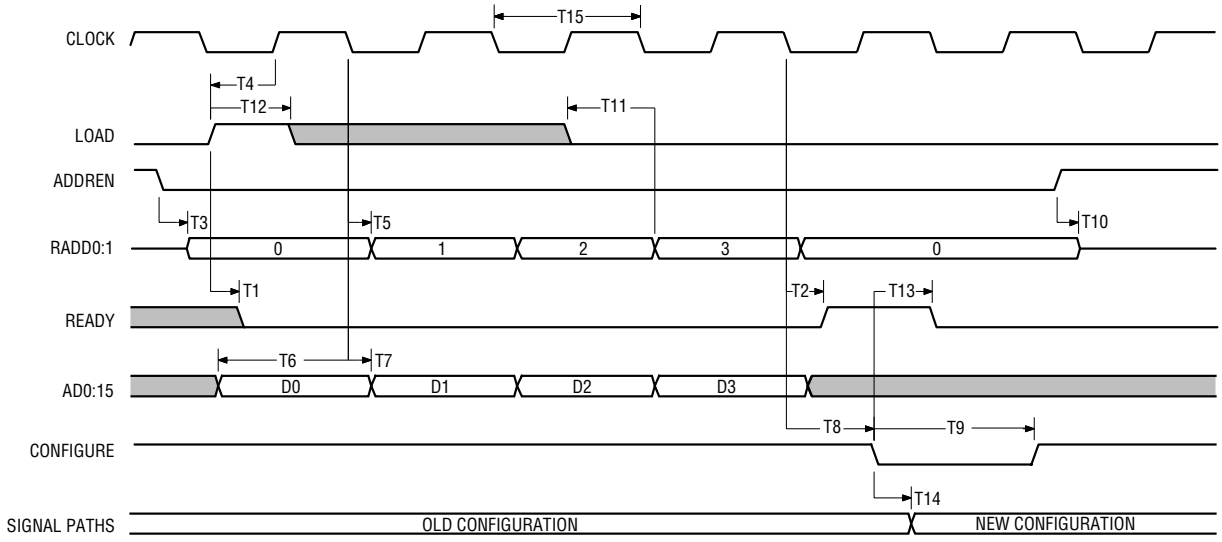
Note: INT CONFIGURE is an internal signal shown for clarity of operation.

Table 9. TQ8025 Timing — RAM Loading, External Configure Pulse Mode [1]

Symbol	*Parameter*	*Min.*	*Max.*	*Units*
T1	LOAD high to READY low	3		ns
T2	CLOCK low to READY high	3		ns
T3	ADDREN low to RADD enabled	3		ns
T4	Setup LOAD high to CLOCK high	4		ns
T5	CLOCK low to RADD increment	2		ns
T6	AD0:15 setup before CLOCK low	0		ns
T7	AD0:15 hold time after CLOCK low	2		ns
T8	Setup last CLOCK before CONFIGURE low	2		ns
T9	CONFIGURE low pulse width	10		ns
T10	ADDREN high to RADD tristate	3		ns
T11	LOAD low prior to 3rd CLOCK low	4		ns
T12	LOAD high pulse	TBD		ns
T13	CONFIGURE low to READY low	TBD		ns
T14	CONFIGURE low to SIGNAL PATHS updated	4		ns
T15	CLOCK period	20		ns

Notes: 1. LDMODE = 1; AUTOCONFIG = 0, RESET– = 1.

Figure 3. TQ8025 Timing — RAM Loading, External Configure Pulse Mode



LDMODE = 1; AUTOCONFIG = 1, RESET– = 1, CONFIG = 1.

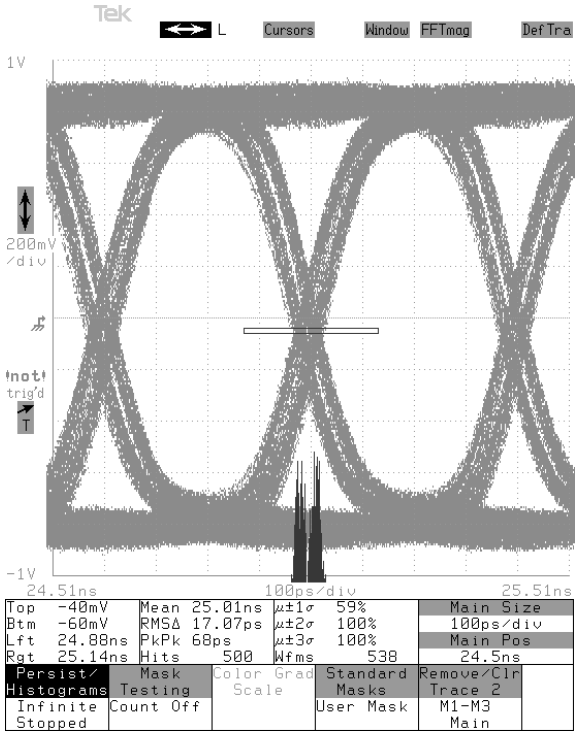
Typical Performance

Data Rate: 2.5Gb/s

Data Pattern: 2^7 PRBS

Note: Measured jitter is 68ps pk-pk.

Signal source jitter is 32ps pk-pk.



Rise and Fall

Data Rate: 2.5Gb/s

Rise Time: 115ps

Fall Time: 109ps

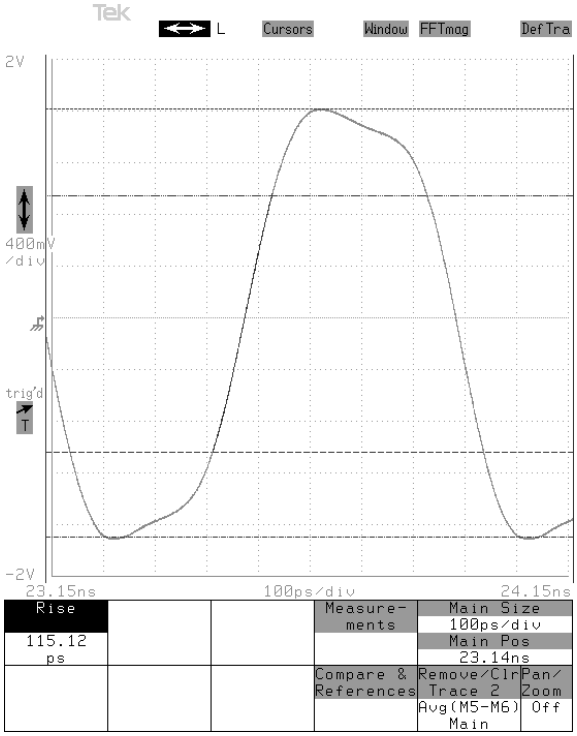


Figure 4. TQ8025 pinout — top view

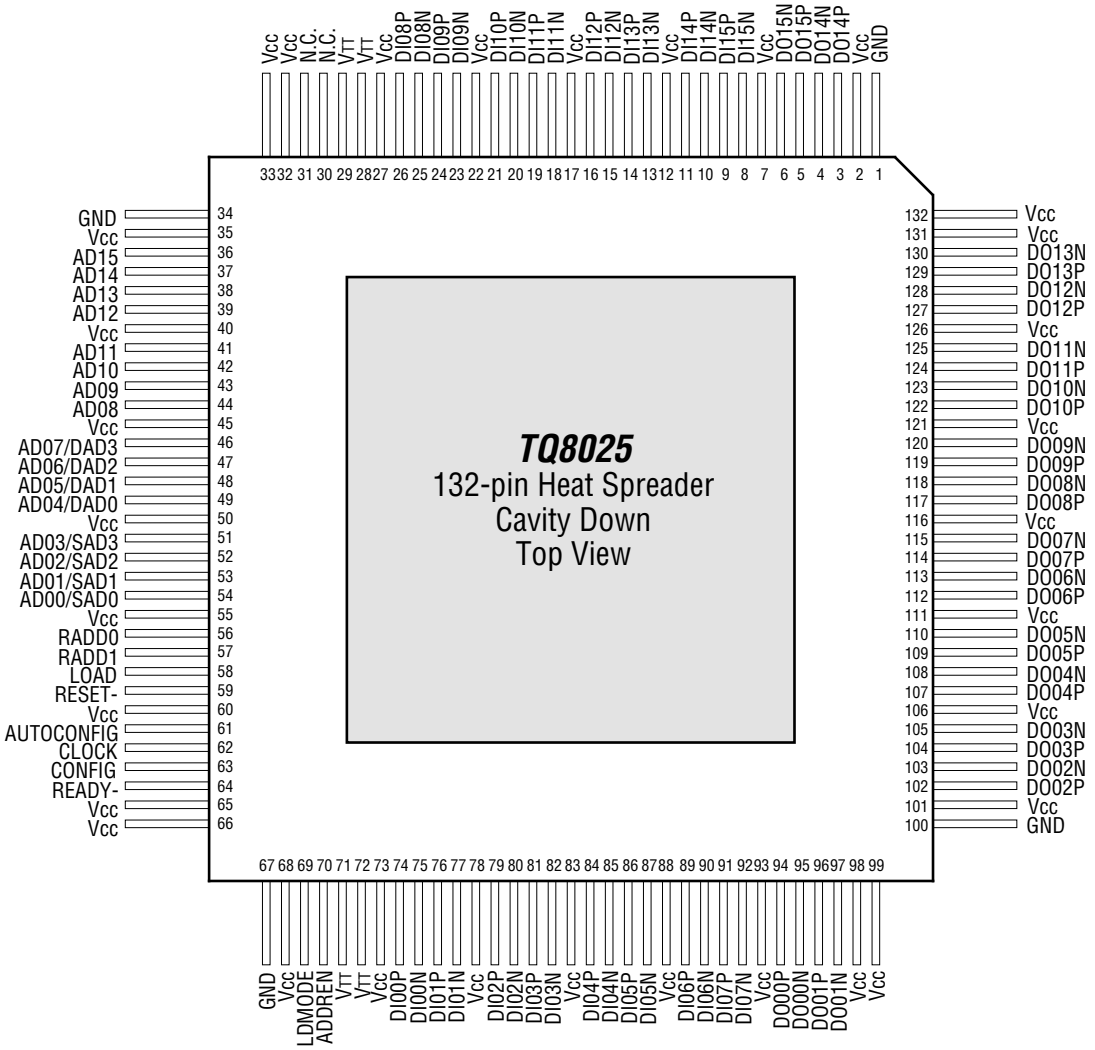
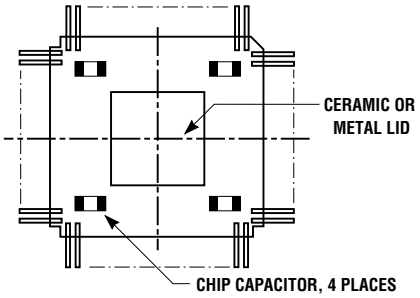


Table 10. TQ8025 Pin Descriptions

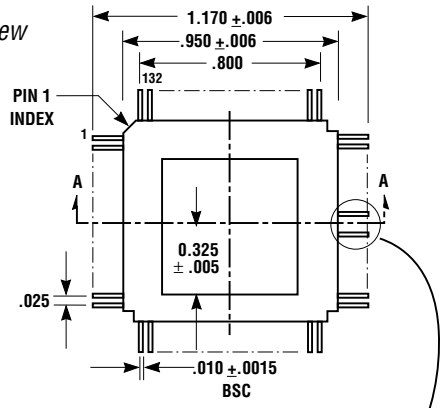
Signal	*Name/Level*	*Description*
DI00P-DI15P DI0N-DI15N	Data input true and complement Differential CML/PECL input	Differential data input ports. VH = 0 V, VL = –300 mV max. Internal 50-ohm terminations to VTT (CML = 0 V;ECL = –2.0 V).
DO0P-DO15P, DO0N-DO15N	Data output true and complement Differential CML/PECL output	Differential data output ports. 600 mV min. differential swing.
AD00:15	Input address; TTL input	Serial input address, LSB first in time; ADn programs output port n.
RADD0:1	RAM address; TTL output, tristate	Used to generate address 0-3 during configure load from RAM.
ADDREN	Enable RADD0:2; TTL input	When low, enables RADD0:1; when high, forces RADD0:1 tristate.
CLOCK	Clock; TTL input	Controls cycle time of address generator and AUTOCONFIG.
AUTOCONFIG	Configure mode; TTL input	When high, internal CONFIGURE is automatically generated.
READY	READY; open-drain output	Indicates end of AUTOCONFIG or end of address LOAD cycle when high. Reset low by RESET-, CONFIG low, or LOAD rising. Requires external pullup to V_{CC}.
LOAD	LOAD; TTL input	For LDMODE=1, ADDREN=0: AUTOCONFIG=0, rising LOAD causes ADDR0:1 to generate RAM addresses, then READY is asserted after four clock ticks. For AUTOCONFIG=1, LOAD rising causes ADDR0:1 to generate addresses, causing an internal CONFIG to be generated, after which READY is asserted. For LDMODE=0, see SAD0:3 and DAD0:3.
CONFIGURE	CONFIGURE; TTL input	Used to load address contents of internal address registers. Active LOW. Crosspoint will be configured within 4 ns (objective) of CONFIG falling low.
LDMODE	Load Mode; TTL input	When floated high, AD0-15 are used for configuration. When tied low, SAD0-3 and DAD0-3 are used for configuration. When AUTOCONFIG is disabled, and AD08-15 are ignored.
SAD0:3	Source Address; TTL inputs	When LDMODE is low, specifies input address to be connected to output port specified by DAD0:3. Latched by falling LOAD (LDMODE=0).
DAD0:3	Destination Address; TTL input	When LDMODE is low, specifies output address to be connected to input port specified by SAD0:3. Latched by falling LOAD (LDMODE=0).
VCC, GND, VTT	+5V, Ground; Termination Voltage	Power and ground pins. V_{TT} = GND for CML inputs; V_{TT} = V_{CC} – 2V for PECL inputs.
RESET–	Reset; TTL Input	While low, programs all output ports to connect to input port 0. Strobing CONFIG after reset restores user port programming if device power was stable since last user programming and during RESET–. Active low, Schmitt triggered.

Figure 5. Mechanical Dimensions

Bottom view

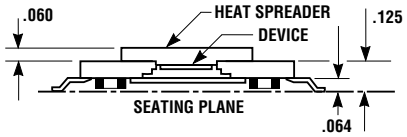


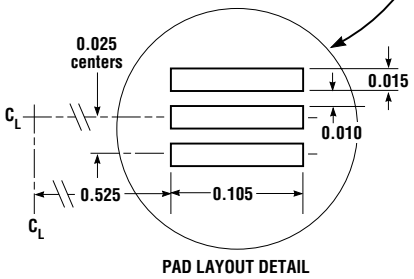
Top view



1. Part is symmetrical about the center axes.
2. Centerline bisects center pin in both directions.
3. See pad detail below.

Section A-A





PAD LAYOUT DETAIL

Ordering Information

TQ8025	*2.5 Gb/s 16x16 Crosspoint Switch*

Additional Information

For latest specifications, additional product information,
worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel: (503) 615-9000**
Email: sales@tqs.com **Fax: (503) 615-8900**

For technical questions and additional information on specific applications:

Email: applications@tqs.com

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