DATA SHEET

TSA5526; TSA5527
1.3 GHz universal bus-controlled TV synthesizers

Product specification
Supersedes data of 1995 Mar 22
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Philips Semiconductors

PHILIPS

1.3 GHz universal bus-controlled TV synthesizers

TSA5526; TSA5527

FEATURES

- Complete 1.3 GHz single chip system
- Four PNP band switch buffers (40 mA)
- 33 V output tuning voltage
- In-lock detector
- 5-step ADC
- 15-bit programmable divider
- Programmable reference divider ratio (512, 640 or 1024)
- Programmable charge-pump current (60 or 280 μA)
- Programmable automatic charge-pump current switch
- Varicap drive disable
- Universal bus protocol I²C-bus or 3-wire bus:
  - bus protocol for 18 or 19 bits transmission (3-wire bus)
  - extra protocol for 27 bits for test and features (3-wire bus)
  - address plus 4 data bytes transmission (I²C-bus write mode)
  - address plus 1 status byte transmission (I²C-bus read mode)
  - three independent I²C-bus addresses
- Low power and low radiation.

APPLICATIONS

- TV tuners and front ends
- VCR tuners.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TSA5526M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5526T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TSA5527M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5527T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TSA5526AM	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5526AT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TSA5527AM	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5527AT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage (+5 V)		4.5	–	5.5	V
V_{CC2}	band switch supply voltage (12 V)		V_{CC1}	12	13.5	V
I_{CC1}	supply current		–	20	25	mA
I_{CC2}	band switch supply current	note 1	–	50	55	mA
f_{RF}	RF input frequency		64	–	1300	MHz
$V_{i(RF)}$	RF input voltage	f_i = 80 to 150 MHz	–25	–	3	dBm
		f_i = 150 to 1000 MHz	–28	–	3	dBm
		f_i = 1000 to 1300 MHz	–15	–	3	dBm
f_{xtal}	crystal oscillator input frequency		3.2	4.0	4.48	MHz
$I_{o(PNP)}$	PNP band switch buffers output current	note 2	4	–	50	mA
P_{tot}	total power dissipation	note 3	–	250	400	mW
T_{stg}	storage temperature		–40	–	+150	°C
T_{amb}	operating ambient temperature		–20	–	+85	°C

Notes

1. One band switch buffer ON, I_o = 40 mA.
2. One band switch buffer ON, I_o = 40 mA; two buffers ON, maximum sum of I_o = 50 mA.
3. The power dissipation is calculated as follows:

$$P_D = V_{CC1} \times I_{CC1} + V_{CC2} \times (I_{CC2} - I_o) + I_o \times V_{CE(satPNP)} + (V33/2)^2/27k\Omega.$$

GENERAL DESCRIPTION

The device is a single-chip PLL frequency synthesizer designed for TV and VCR tuning systems. The circuit consists of a divide-by-eight prescaler with its own preamplifier, a 15-bit programmable divider, a crystal oscillator and its programmable reference divider and a phase/frequency detector combined with a charge-pump which drives the tuning amplifier and the 33 V output. Four high-current PNP band switch buffers are provided for band switching. Two PNP buffers can be switched on simultaneously. The sum of the collector currents is limited to 50 mA.

Depending on the reference divider ratio (512, 640 or 1024), the phase comparator operates at 3.90625 kHz, 6.25 kHz or 7.8125 kHz using a 4 MHz crystal.

The device can be controlled in accordance with the I^2C-bus format or the 3-wire bus format depending on the voltage applied to the SW input (see Table 2). In the 3-wire bus mode (SW = HIGH) pin 12 is the LOCK output. The lock output is LOW when the PLL loop is locked. In the I^2C-bus mode (SW = LOW) the LOCK detector bit FL is set to logic 1 when the loop is locked and is read on the SDA line (status byte) during a read operation. The ADC input is available on pin 12 for AFC control in the I^2C-bus mode only. The ADC code is read during a read operation on the I^2C-bus. In the test mode pin 12 is used as a test output for f_{ref} and $\frac{1}{2}f_{div}$ in the I^2C-bus mode and the 3-wire bus mode (see Table 6).

When the automatic charge-pump current switch mode is activated, depending on the device given in Table 6, and when the loop is phase-locked, the charge-pump current value is automatically switched to LOW.

This action is taken to improve the carrier-to-noise ratio. The status of this feature can be read in the ACPS flag during a read operation on the I^2C-bus (see Table 8).

I^2C-bus format (SW = LOW)

Five serial bytes (including address byte) are required to address the device, select the VCO frequency, program the four PNP band switch buffers, set the charge-pump current and the reference divider ratio.

The device has three independent I^2C-bus addresses which can be selected by applying a specific voltage on the CE input (see Table 5). The general address C2 is always valid. When the I^2C-bus format is fully used, TSA5526 and TSA5527 are equal.

3-wire bus format (SW = V_{CC1} or open-circuit)

Data is transmitted to the device during a HIGH level on the CE input (enable line pin 15). The device is compatible with 18-bit and 19-bit data formats. The first four bits are used to program the PNP band switch buffers and the remaining bits are used to control the programmable divider. A 27-bit data format may also be used to set the charge-pump current, the reference divider ratio and for test purposes. The differences between TSA5526 and TSA5527 are given in Table 1.

When the 27-bit format is used, the TSA5526 and TSA5527 are equal and the reference divider is controlled by the RSA and RSB bits (see Table 7 and Figs 3, 4 and 5).

Table 1 Differences between TSA5526 and TSA5527

TYPE NUMBER	DATA WORD	REFERENCE DIVIDER	FREQUENCY STEP (kHz)
TSA5526	18-bit	512(1)	62.5
TSA5526	19-bit	1024(1)	31.25
TSA5527	19-bit	640(2)	50

Notes

1. The selection of the reference divider is given by an automatic identification of the data word length.
2. The reference divider is set to 640 at power-on reset.

BLOCK DIAGRAM

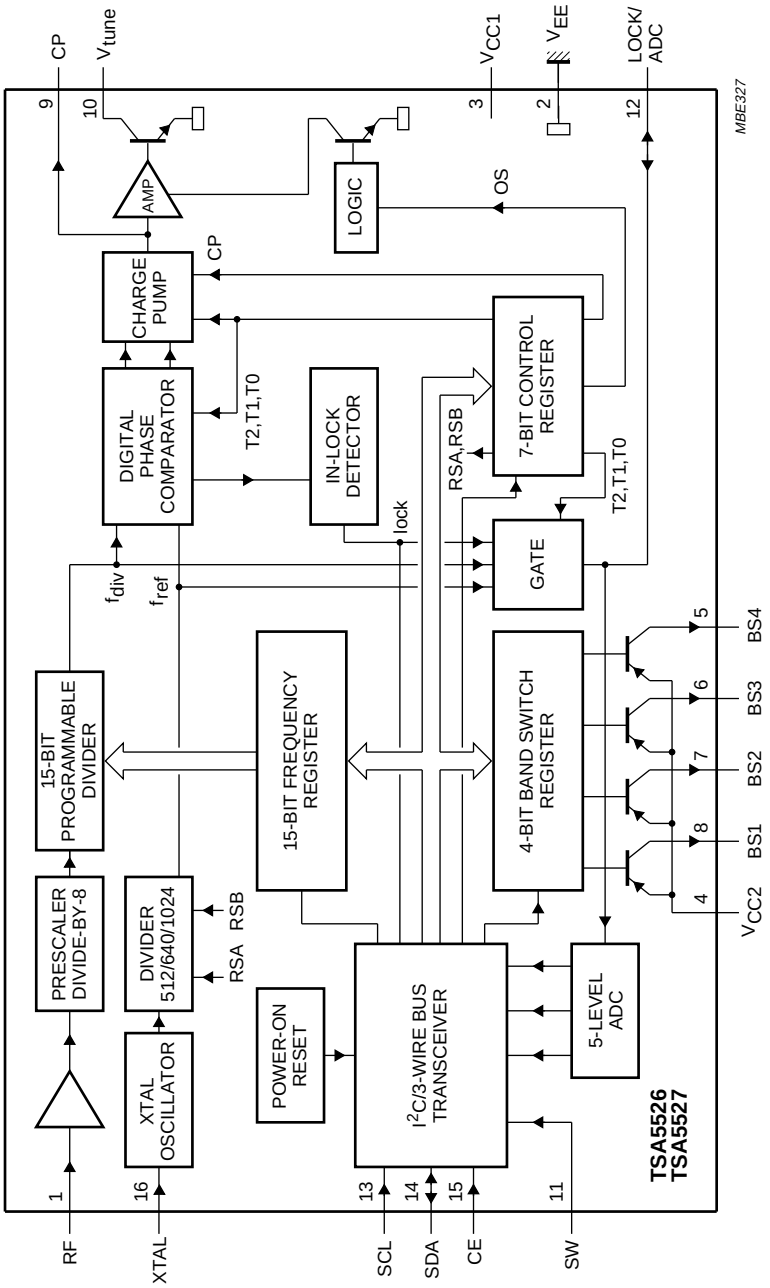


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RF	1	RF signal input
V_{EE}	2	ground
V_{CC1}	3	supply voltage (+5 V)
V_{CC2}	4	band switch supply voltage (+12 V)
BS4	5	PNP band switch buffer output 4
BS3	6	PNP band switch buffer output 3
BS2	7	PNP band switch buffer output 2
BS1	8	PNP band switch buffer output 1
CP	9	charge-pump output
V_{tune}	10	tuning voltage output
SW	11	bus format selection input, I²C-bus or 3-wire
LOCK/ADC	12	lock detector output (3-wire bus/ ADC input (I²C-bus)
SCL	13	serial clock input
SDA	14	serial data input/output
CE	15	chip enable/address selection input
XTAL	16	crystal oscillator input

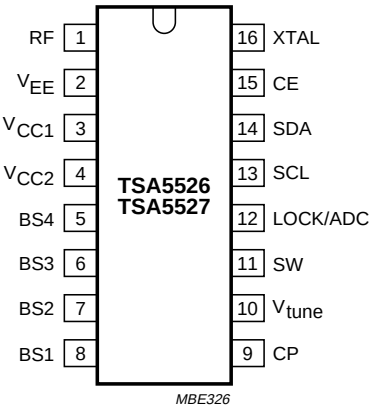


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The device is controlled via the I²C-bus or the 3-wire bus depending on the voltage applied to the SW input (pin 11). A HIGH level on the SW input enables the 3-wire bus inputs which are CE (Chip Enable), SDA (serial data input) and SCL (serial clock input). A LOW level on the SW input enables the I²C-bus inputs which are AS (Address Selection input), SDA (serial data input/output) and SCL (serial clock input). The bus format selection is given in Table 2.

I²C-bus mode (SW = LOW); see Table 3

WRITE MODE (R/W = 0)

Data bytes can be sent to the device after the address transmission (first byte). Four data bytes are required to fully program the device. The bus transceiver has an auto-increment facility which permits the programming of the device within one single transmission (address + 4 data bytes).

The device can also be partially programmed providing that the first data byte following the address is Divider Byte 1 (DB1) or the Control Byte (CB). The bits in the data bytes are defined in Table 3.

The first bit of the first data byte transmitted indicates whether frequency data (first bit = logic 0) or control and band switch data (first bit = logic 1) will follow. Until an I²C-bus STOP command is sent by the controller, additional data bytes can be entered without the need to readdress the device. The frequency register is loaded after the 8th clock pulse of the second Divider Byte (DB2), the control register is loaded after the 8th clock pulse of the Control Byte (CB) and the band switch register is loaded after the 8th clock pulse of the Band switch Byte (BB).

I²C-BUS ADDRESS SELECTION

The module address contains programmable address bits (MA1 and MA0) which offer the possibility of having several synthesizers (up to 3) in one system by applying a specific voltage to the CE input.

The relationship between MA1 and MA0 and the input voltage applied to the CE input is given in Table 5.

Table 2 Bus format selection

PIN	NAME	3-WIRE BUS MODE	I²C-BUS MODE
11	SW	OPEN or HIGH	LOW
12	LOCK/ADC	LOCK/TEST output	ADC input/TEST output
13	SCL	clock input	SCL input
14	SDA	data input	SDA input/output
15	CE	chip enable input	address selection input

Table 3 I²C-bus data format

BYTE	MSB	DATA BYTE						LSB	SLAVE ANSWER
Address Byte (ADB)	1	1	0	0	0	MA1	MA0	R/W = 0	A
Divider Byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A
Divider Byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control Byte (CB)	1	CP	T2	T1	T0	RSA	RSB	OS	A
Band switch Byte (BB)	X	X	X	X	BS4	BS3	BS2	BS1	A

Table 4 Description of Table 3

SYMBOL	DESCRIPTION
A	acknowledge
MA1 and MA0	programmable address bits (see Table 5)
N14 to N0	programmable divider bits; $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2 + N0$
CP	charge-pump current; CP = 0 = 60 μA; CP = 1 = 280 μA (default)
T2 to T0	test bits (see Table 6); for normal operation T2 = 0, T1 = 0 and T0 = 1 (default)
RSA and RSB	reference divider ratio select bits (see Table 7)
OS	tuning amplifier control bit; for normal operation OS = 0 and tuning voltage is ON (default); when OS = 1 tuning voltage is OFF (high impedance)
BS4 to BS1	PNP band switch buffers control bits; when BS_n = 0 buffer n is OFF; when BS_n = 1 buffer n is ON
X	don't care

Table 5 I²C-bus address selection

VOLTAGE APPLIED TO THE CE INPUT (SW = LOW)	MA1	MA0
0 V to $0.1V_{CC1}$	0	0
Always valid	0	1
$0.4V_{CC1}$ to $0.6V_{CC1}$	1	0
$0.9V_{CC1}$ to V_{CC1}	1	1

Table 6 Test bits

T2	T1	T0	TSA5526; TSA5527	TSA5526A; TSA5527A	REMARKS
0	0	0	normal operation with automatic charge-pump switch ON	automatic charge-pump switch OFF	
0	0	1	normal operation with automatic charge-pump switch OFF	automatic charge-pump switch ON	status at POR
0	1	X	charge-pump is OFF	charge-pump is OFF	
1	1	0	charge-pump is sinking current	charge-pump is sinking current	
1	1	1	charge-pump is sourcing current	charge-pump is sourcing current	
1	0	0	f_{ref} is available at LOCK output	f_{ref} is available at LOCK output	the ADC cannot be used when test mode is active
1	0	1	$\frac{1}{2}f_{div}$ is available at LOCK output	$\frac{1}{2}f_{div}$ is available at LOCK output	the ADC cannot be used when test mode is active

Table 7 Ratio select bits

RSA	RSB	REFERENCE DIVIDER
X	0	640
0	1	1024
1	1	512

READ MODE (R/W = LOGIC 1); see Table 8

Data can be read from the device by setting the R/W bit to logic 1. After the slave address has been recognized, the device generates an acknowledge pulse and the first data byte (status byte) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a HIGH level of the SCL clock signal. A second data byte can be read from the device if the microcontroller generates an acknowledge on the SDA line (master acknowledge). End of transmission will occur if no master acknowledge occurs.

The device will then release the data line to allow the microcontroller to generate a stop condition. The POR flag is set to logic 1 at power-on. The flag is reset when an end-of-data is detected by the device (end of a read sequence). Control of the loop is made possible with the in-lock flag (FL) which indicates when the loop is locked (FL = logic 1).

The Automatic Charge-Pump Switch flag (ACPS) is LOW when the automatic charge-pump switch mode is ON and the loop is locked. In other conditions ACPS = logic 1. When ACPS = logic 0, the charge-pump current is forced to the LOW value.

A built-in ADC is available at pin 12 (I^2C-bus only). This converter can be used to apply AFC information to the microcontroller from the IF section of the television. The relationship between the bits A2 to A0 is given in Table 9.

Table 8 Read data format

BYTE	MSB	DATA BYTE						LSB	SLAVE ANSWER
Address Byte (ADB)	1	1	0	0	0	MA1	MA0	R/W = 1	A(1)
Status Byte (SB)	POR(2)	FL(3)	ACPS(4)	1	1	A2(5)	A1(5)	A0(5)	–

Notes

1. A = acknowledge.
2. POR = power-on reset flag (POR = logic 1 at power-on).
3. FL = in-lock flag (FL = logic 1 when the loop is locked).
4. ACPS = automatic charge-pump switch flag (active ACPS = logic 0; non-active ACPS = logic 1).
5. A2 to A0 = digital outputs of the 5-level ADC.

Table 9 ADC levels

VOLTAGE APPLIED AT ADC INPUT(1)	A2	A1	A0
$0.6V_{CC1}$ to V_{CC1}	1	0	0
$0.45V_{CC1}$ to $0.6V_{CC1}$	0	1	1
$0.3V_{CC1}$ to $0.45V_{CC1}$	0	1	0
$0.15V_{CC1}$ to $0.3V_{CC1}$	0	0	1
0 to $0.15V_{CC1}$	0	0	0

Note

1. Accuracy is $\pm 0.03V_{CC1}$.

3-wire bus mode (SW = open-circuit or V_{CC1}); see Figs 3**,** 4 and 5

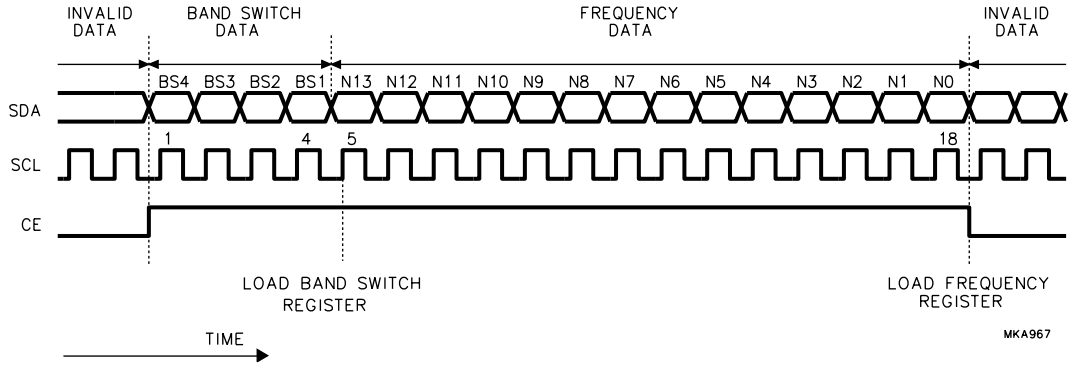
During a HIGH level on the CE input, the data is clocked into the data register at the HIGH-to-LOW transition of the clock pulse. The first four bits control the band switch buffers and are loaded into the internal band switch register on the 5th rising edge of the clock pulse.
The frequency bits are loaded into the frequency register at the HIGH-to-LOW transition of the chip enable line when an 18-bit or 19-bit data word is transmitted.

At power-on the charge-pump current is set to 280 μA, the tuning voltage output is disabled (V_{tune} = 33 V in application; see Fig.12), the test bits T2, T1 and T0 are set to the 0 0 1 state in the normal mode with ACPS OFF for TSA55226; TSA5527 and ACPS ON for TSA5526A; TSA5527A. RSB is set to logic 1 (TSA5526) or logic 0 (TSA5527). When an 18-bit data word is transmitted, the most significant bit of the divider N14 is internally set to logic 0 and bit RSA is set to logic 1. When a 19-bit data word is transmitted, bit RSA is set to logic 0.

When a 27-bit word is transmitted, the frequency bits are loaded into the frequency register on the 20th rising edge of the clock pulse and the control bits at the HIGH-to-LOW transition of the chip enable line. In this mode, the reference divider is given by the RSA and RSB bits (see Table 7). The test bits T2, T1 and T0, the charge-pump bit CP, the ratio select bit RSB and the OS bit can only be selected or changed with a 27-bit transmission. They remain programmed if an 18-bit or a 19-bit transmission occurs. Only RSA is controlled by the transmission length when the 18-bit or 19-bit format is used.

A data word of less than 18 bits will not affect the frequency register of the device. The definition of the bits is unchanged compared to the I^2C-bus mode.

The power-on detection threshold voltage V_{POR} is fixed to V_{CC1} = 2 V at room temperature. Below this threshold, the device is reset to the power-on state previously described.

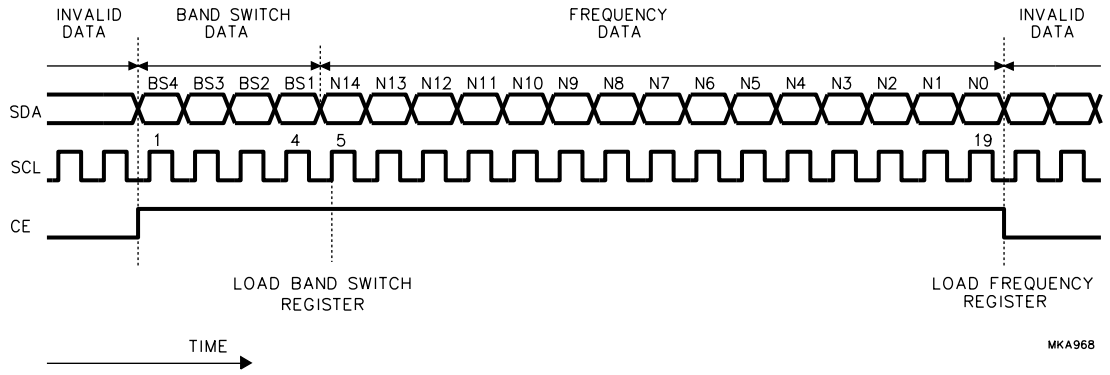


For TSA5526 bit RSB = logic 1 at power-on; the reference divider is 512 or 1024.

For TSA5527 bit RSB = logic 0 at power-on; the reference divider is 640.

For TSA5526 and TSA5527 the value of RSB can also be programmed by using the 27-bit data format. When returning to the normal mode, bit RSB remains as programmed with the 27-bit data word.

Fig.3 Normal mode; 18-bit data format (RSA = 1).

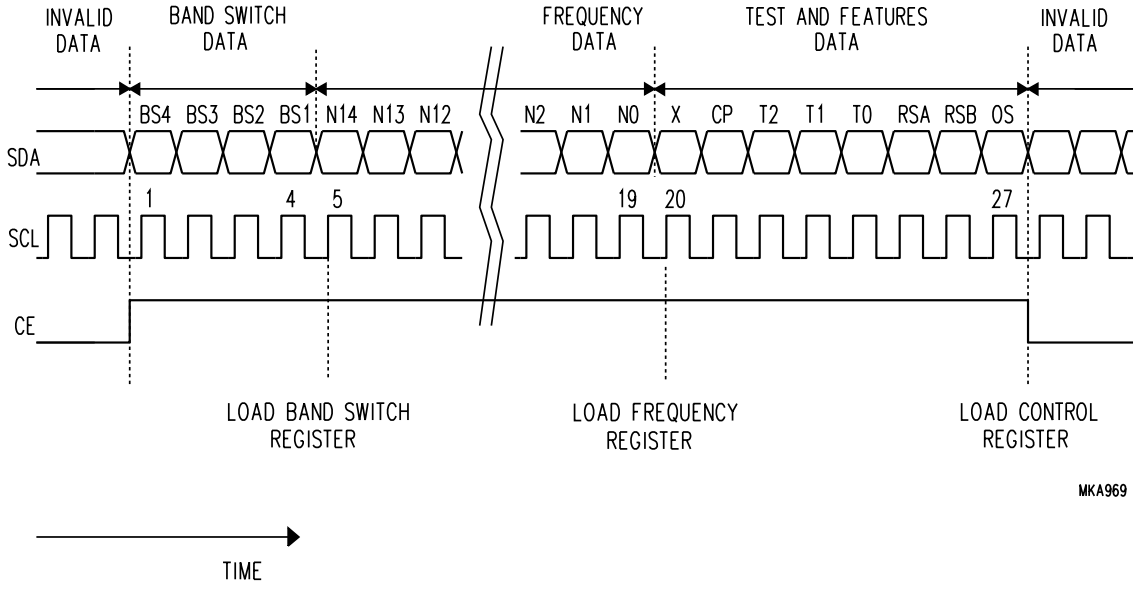


For TSA5526 bit RSB = 1 at power-on; the reference divider is 512 or 1024.

For TSA5527 bit RSB = 0 at power-on; the reference divider is 640.

For TSA5526/TSA5527 the value of RSB can also be programmed by using the 27-bit data format. When returning to the normal mode, bit RSB remains as programmed with the 27-bit data word.

Fig.4 Normal mode; 19-bit data format (RSA = 0).



For TSA5526 bit RSB = 1 at power-on; the reference divider is 512 or 1024.

For TSA5527 bit RSB = 0 at power-on; the reference divider is 640.

For TSA5526/TSA5527 the value of RSB can also be programmed by using the 27-bit data format. When returning to the normal mode, bit RSB remains as programmed with the 27-bit data word.

Fig.5 Test and features mode; 27-bit data format.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC1}	supply voltage; +5 V (pin 3)	–0.3	+6.0	V
V_{CC2}	band switch supply voltage; +12 V (pin 4)	–0.3	+16	V
$V_{i(RF)}$	prescaler input voltage (pin 1)	–0.3	V_{CC1}	V
$V_{o(BSn)}$	band switch buffers output voltage (pins 5 to 8)	–0.3	V_{CC2}	V
$I_{o(BSn)}$	band switch buffers output current	–1	+50	mA
$V_{o(CP)}$	charge-pump output voltage (pin 9)	–0.3	V_{CC1}	V
$V_{o(tune)}$	output tuning voltage (pin 10)	–0.3	+35	V
$V_{i(SW)}$	input switching voltage (pin 11)	–0.3	V_{CC1}	V
$V_{o(LOCK)}$	lock output voltage (pin 12)	–0.3	V_{CC1}	V
$V_{i(SCL)}$	serial clock input voltage (pin 13)	–0.3	+6.0	V
$V_{i/o(SDA)}$	serial data input/output voltage (pin 14)	–0.3	+6.0	V
$I_{o(SDA)}$	serial data output current	–1	+10	mA
$V_{i(CE)}$	chip enable input voltage (pin 15)	–0.3	+6.0	V
$V_{i(xtal)}$	crystal oscillator input voltage (pin 16)	–0.3	V_{CC1}	V
T_{stg}	storage temperature	–40	+150	°C
T_j	maximum junction temperature	–	+150	°C
t_{sc}	short-circuit time; every pin except pin 4 to pin 3 and every pin to pin 2; note 1	–	10	s

Note

1. Short-circuit between V_{CC1} and V_{CC2} is allowed provided the voltage applied to V_{CC2} is less than the 6 V maximum rating at V_{CC1}.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SO16	110	K/W
	SSOP16	142	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling bipolar devices. Every pin withstands the ESD test in accordance with *"MIL-STD-883C*" category B (2000 V). Every pin withstands the ESD test in accordance with Philips Semiconductors Machine Model 0 Ω, 200 pF (200 V).

CHARACTERISTICS

V_{CC1} = 4.5 to 5.5 V; V_{CC2} = V_{CC1} to 13.2 V; T_{amb} = –20 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC1}	supply voltage		4.5	–	5.5	V
V_{CC2}	band switch buffers supply voltage		V_{CC1}	–	13.5	V
I_{CC1}	supply current	at power-on	–	20	25	mA
I_{CC2}	band switch buffers supply current	at power-on	–	0.5	1.0	mA
		one band switch buffer is ON; I_{source} = 40 mA	–	50	55	mA
		two band switch buffers are ON; I_{source} = 40 mA + 5 mA (any combination)	–	56	62	mA
V_{POR}	supply voltage below which POR is active		1.5	2.0	–	V
f_{RF}	RF input frequency		64	–	1300	MHz
DR	divider ratio	15-bit frequency word	256	–	32767	
		14-bit frequency word	256	–	16383	
f_{xtal}	crystal oscillator input frequency	R_{xtal} = 25 to 300 Ω	3.2	4	4.48	MHz
Z_{xtal}	crystal oscillator input impedance (absolute value)	f_i = 4 MHz	600	1200	–	Ω
Prescaler (see Figs 6 **and** 7)						
$V_{i(RF)}$	RF input level	f_i = 80 to 150 MHz	–25	–	3	dBm
		f_i = 150 to 1000 MHz	–28	–	3	dBm
		f_i = 1000 to 1300 MHz	–15	–	3	dBm
$Z_{i(RF)}$	input impedance	see Fig.8				
PNP band switch buffers outputs (pins 5 to 8)						
I_{LO}	output leakage current	V_{CC2} = 13.5 V; V_o = 0 V	–10	–	–	µA
$V_{o(sat)}$	output saturation voltage	I_{source} = 40 mA; $V_{o(sat)} = V_{CC2} - V_o$	–	0.2	0.4	V
LOCK output (PNP collector output) 3 wire bus mode (pin 12)						
$I_{o(ool)}$	output current when out-of-lock	V_{CC1} = 5.5 V; V_o = 5.5 V	–	–	100	µA
$V_{osat(ool)}$	output saturation voltage when out-of-lock	I_{source} = 200 µA; $V_{o(sat)} = V_{CC1} - V_o$	–	0.4	0.8	V
$V_{o(LOCK)}$	lock output voltage		–	0.01	0.4	V
ADC input (I^2C-bus mode) pin 12						
$V_{i(ADC)}$	ADC input voltage	see Table 9	0	–	V_{CC1}	V
$I_{IH(ADC)}$	HIGH level input current	$V_{ADC} = V_{CC1}$	–	–	10	µA
$I_{IL(ADC)}$	LOW level input current	V_{ADC} = 0 V	–10	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SW input (bus format switch)						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3	–	V_{CC1}	V
I_{IH}	HIGH level input current	$V_{SW} = V_{CC1}$	–	–	10	µA
I_{IL}	LOW level input current	$V_{SW} = 0$ V	–100	–	–	µA
CE input (chip enable/address selection)						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3	–	5.5	V
I_{IH}	HIGH level input current	$V_{CE} = 5.5$ V	–	–	10	µA
I_{IL}	LOW level input current	$V_{CE} = 0$ V	–10	–	–	µA
SCL and SDA inputs						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	5.5	V
I_{IH}	HIGH level input current	$V_{BUS} = 5.5$ V; $V_{CC1} = 0$ V	–	–	10	µA
		$V_{BUS} = 5.5$ V; $V_{CC1} = 5.5$ V	–	–	10	µA
I_{IL}	LOW level input current	$V_{BUS} = 1.5$ V; $V_{CC1} = 0$ V	–	–	10	µA
		$V_{BUS} = 0$ V; $V_{CC1} = 5.5$ V	–10	–	–	µA
f_{clk}	clock frequency		–	100	400	kHz
SDA outputs (I^2C-bus mode)						
I_{LO}	output leakage current	$V_{SDA} = 5.5$ V	–	–	10	µA
V_o	output voltage	$I_{sink} = 3$ mA	–	–	0.4	V
Charge-pump output CP						
$\|I_{ICPH}\|$	HIGH charge-pump current	CP = 1	–	280	–	µA
$\|I_{ICPL}\|$	LOW charge-pump current	CP = 0	–	60	–	µA
V_{CP}	output voltage	in-lock; $T_{amb} = 25$ °C	–	1.95	–	V
$I_{LI(off)}$	off-state leakage current	T2 = 0; T1 = 1	–15	–0.5	+15	nA
Tuning voltage output V_{tune}						
$I_{LO(off)}$	leakage current when switched-off	OS = 1; $V_{tune} = 33$ V	–	–	10	µA
V_o	output voltage when the loop is closed	OS = 0; T2 = 0; T1 = 0; T0 = 1; $R_L = 27$ kΩ; $V_{tune} = 33$ V	0.2	–	32.7	V
3-wire bus timing (see Figs 6 **and** 7)						
t_{HIGH}	clock high time		2	–	–	µs
$t_{SU;DAT}$	data set-up time		2	–	–	µs
$t_{HD;DAT}$	data hold time		2	–	–	µs
$t_{SU;ENSCL}$	enable to clock set-up time		10	–	–	µs
$t_{HD;ENDAT}$	enable to data hold time		2	–	–	µs
t_{EN}	enable between two transmissions		10	–	–	µs
$t_{HD;ENSCL}$	enable to clock active edge hold time		6	–	–	µs

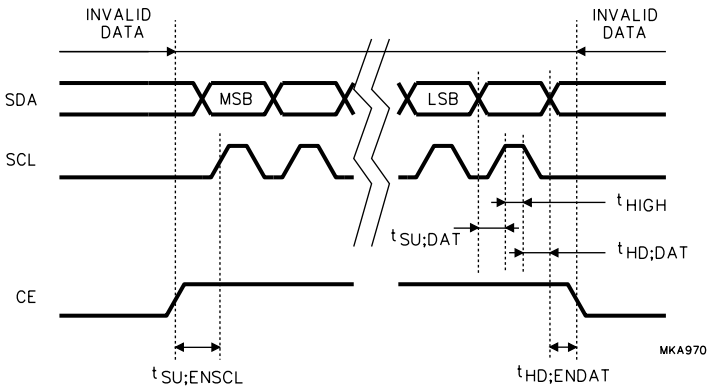


Fig.6 Timing diagram for 3-wire bus; SDA, SCL and CE.

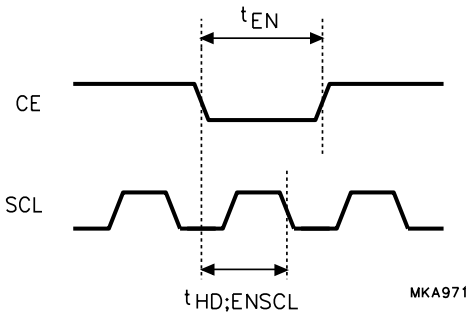


Fig.7 Timing diagram for 3-wire bus; CE and SCL.

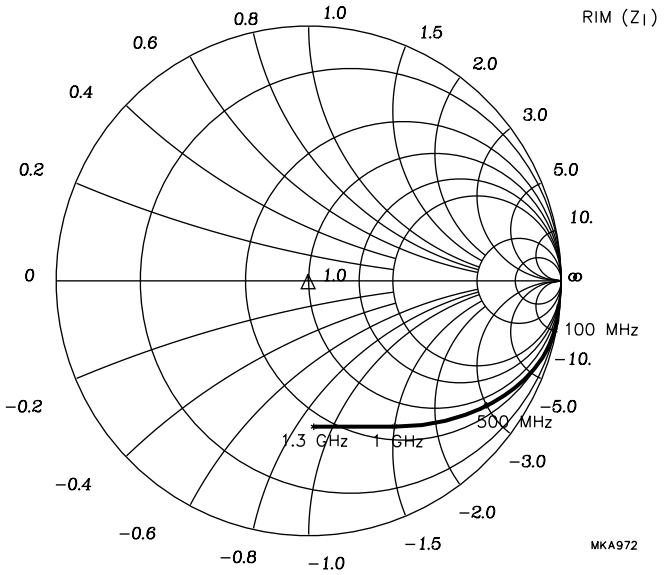


Fig.8 Prescaler Smith chart of typical input impedance at pin 1.

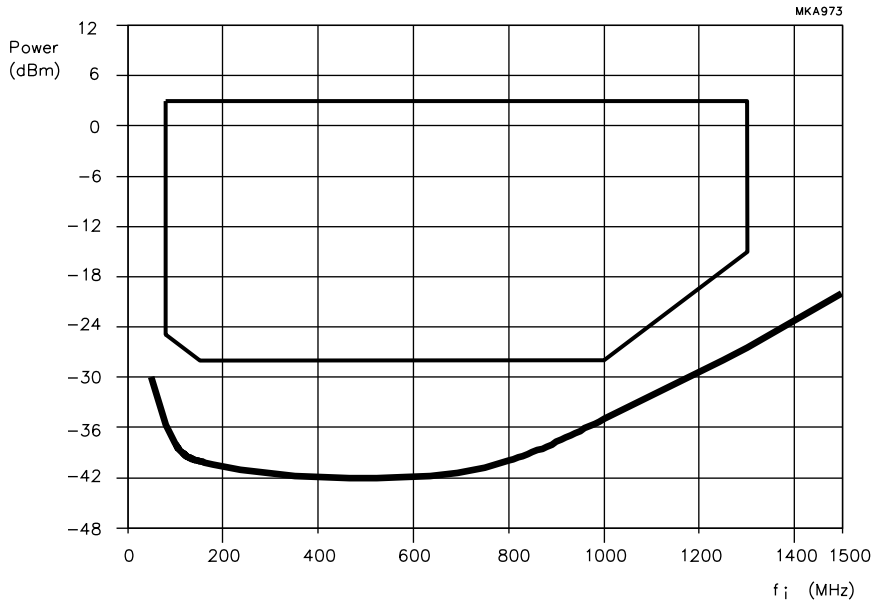


Fig.9 Prescaler typical input sensitivity curve.

INTERNAL PIN CONFIGURATION

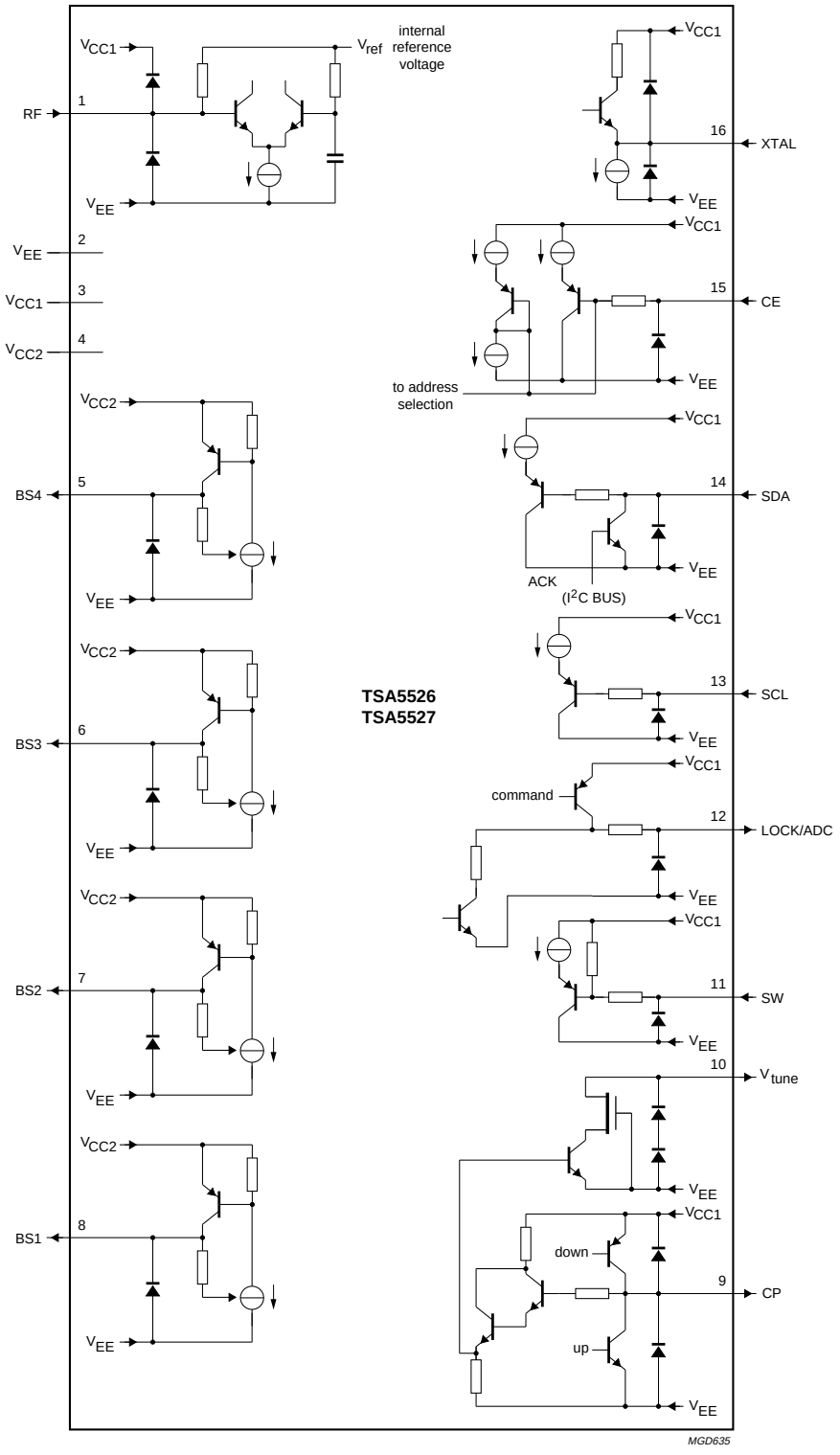


Fig.10 Internal pin configuration.

APPLICATION INFORMATION

Tuning amplifier

The tuning amplifier is capable of driving the varicap voltage without an external transistor. The tuning voltage output must be connected to an external load of 27 kΩ which is connected to the tuning voltage supply rail. Figs 11 and 12 show a possible loop filter. The component values depend on the oscillator characteristics and the selected reference frequency.

Crystal oscillator

The crystal oscillator uses a 4 MHz crystal connected in series with an 18 pF capacitor thereby operating in the series resonance mode. Connecting the oscillator to the supply voltage is preferred but it can, however, also be connected to ground.

Examples of I²C-bus sequences (SW = LOW)

Tables 10 to 14 show the various sequences where f_{osc} = 100 MHz, BS4 = ON, I_{CP} = 280 µA, N = 512, f_{xtal} = 4 MHz, S = START, A = acknowledge and P = STOP. The sequence is as follows:
START + address byte + divider byte 1 + divider byte 2 + control byte + band switch byte + STOP.

For the complete sequence see Table 10 (sequence 1) or Table 11 (sequence 2).

Table 10 Complete sequence 1

S	C2	A	06	A	40	A	CE	A	08	A	P

Table 11 Complete sequence 2

S	C2	A	CE	A	08	A	06	A	40	A	P

Table 12 Divider bytes only sequence

S	C2	A	06	A	40	A	P

Table 13 Control and band switch bytes only sequence

S	C2	A	CE	A	08	A	P

Table 14 Control byte only sequence

S	C2	A	CE	A	P

Other sequences are not allowed in the write mode.

Table 15 One status byte acquisition

S	C3	A	XX[1]	X[2]	P

Notes

1. XX = the read status byte.
2. X = no acknowledge from the master means end of sequence.

Table 16 Two status byte acquisition

S	C3	A	XX(1)	A	XX(1)	X(2)	P

Notes

1. XX = the read status byte.
2. X = no acknowledge from the master means end of sequence.

Other I^2C-bus addresses may be selected by applying an appropriate voltage to the CE input.

Examples of 3-wire bus sequences (TSA5526; SW = OPEN)

Table 17 18-bit sequence (f_{osc} = 800 MHz, BS4 = ON)

1	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0

The reference divider is automatically set to 512 unless RSB has been programmed to 0 during a 27-bit sequence (see Table 19).

Table 18 19-bit sequence (f_{osc} = 650 MHz, BS3 = ON)

0	1	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	0	0

The reference divider is automatically set to 1024 unless RSB has been programmed to 0 during a 27-bit sequence (see Table 19).

Table 19 27-bit sequence (f_{osc} = 750 MHz, BS1 = ON, N = 640, I_{cp} = 60 μA, no test function)

0	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0

Table 20 19-bit sequence

0	0	0	1	0	1	0	1	1	1	0	1	1	1	0	0	0	0	0

This sequence will program f_{osc} to 600 MHz in 50 kHz steps. I_{CP} remains at 60 μA.

Table 21 18-bit sequence

0	0	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	0

This sequence will program f_{osc} to 600 MHz in 50 kHz steps. I_{CP} remains at 60 μA.

Table 22 27-bit sequence (f_{osc} = 650 MHz, BS1 = ON)

0	0	0	1	1	0	1	0	0	0	1	0	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0

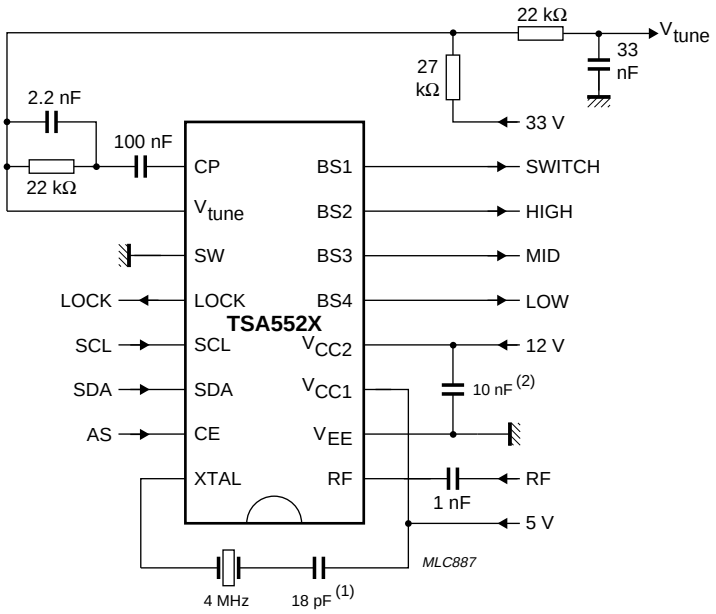
This sequence sets RSA to 0, RSB to 1 and CP to 1. After this sequence I_{CP} = 280 μA, N = 1024 (19-bit transmission) and N = 512 (18-bit transmission), RSB = 1.

Example of 3-wire bus sequence (TSA5527; SW = OPEN)

Table 23 19-bit sequence (f_{osc} = 700 MHz, BS3 = ON)

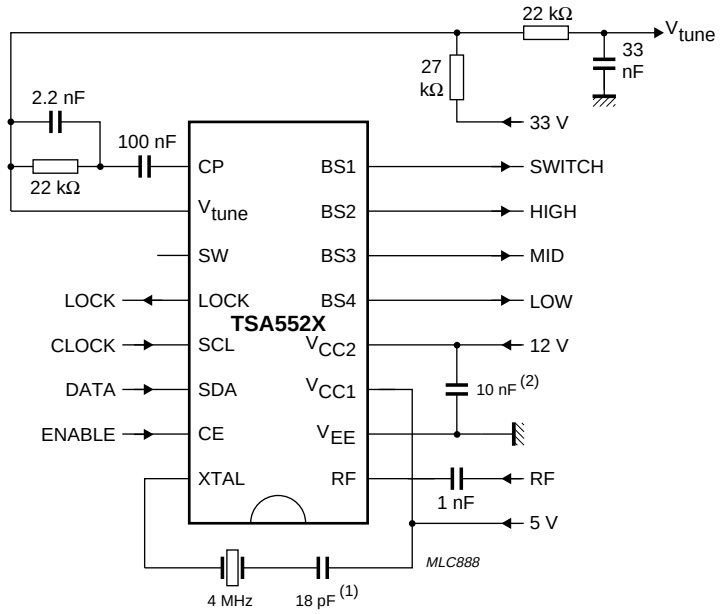
0	1	0	0	0	1	1	0	1	1	0	1	0	1	1	0	0	0	0

N = 640 unless RSB has been programmed to 0 during a 27-bit sequence.



(1) Connection to ground is also allowed.
(2) Capacitor prevents parasitic oscillation on the V_{CC2} line.

Fig.11 Typical I²C-bus application.



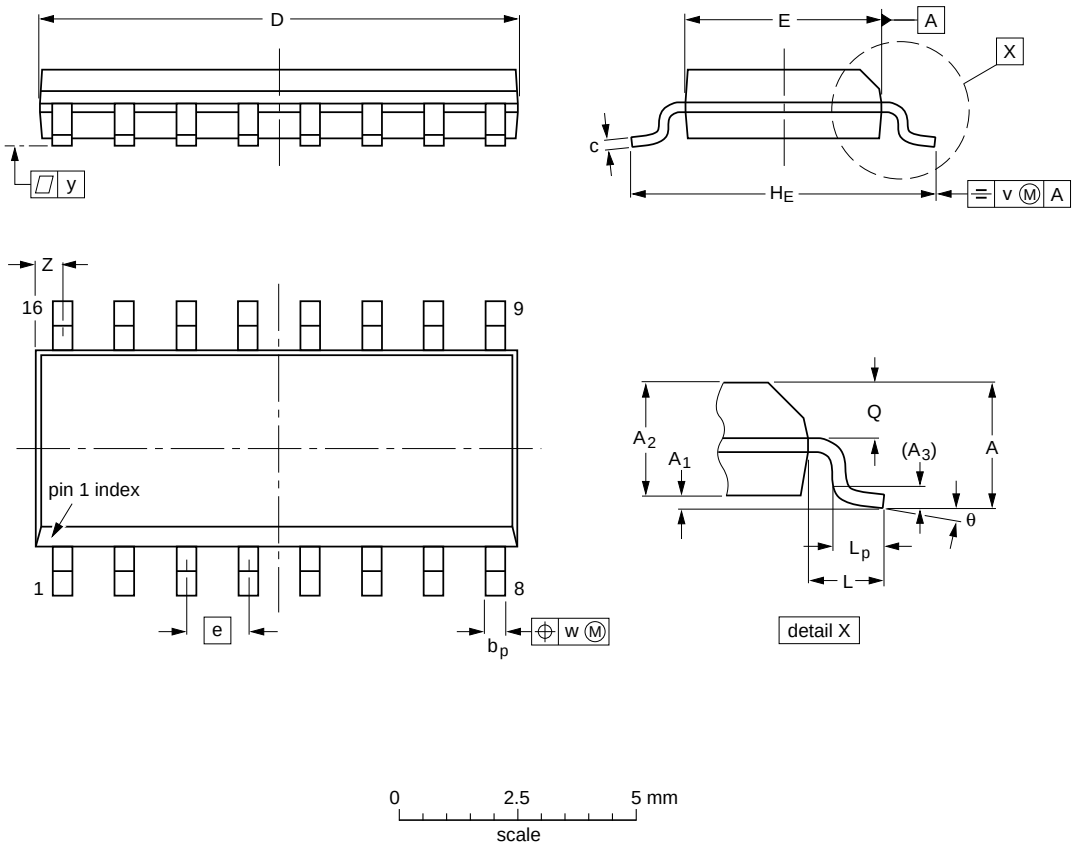
(1) Connection to ground is also allowed.

(2) Capacitor prevents parasitic oscillation on the V_{CC2} line.

Fig.12 Typical 3-wire bus application.

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

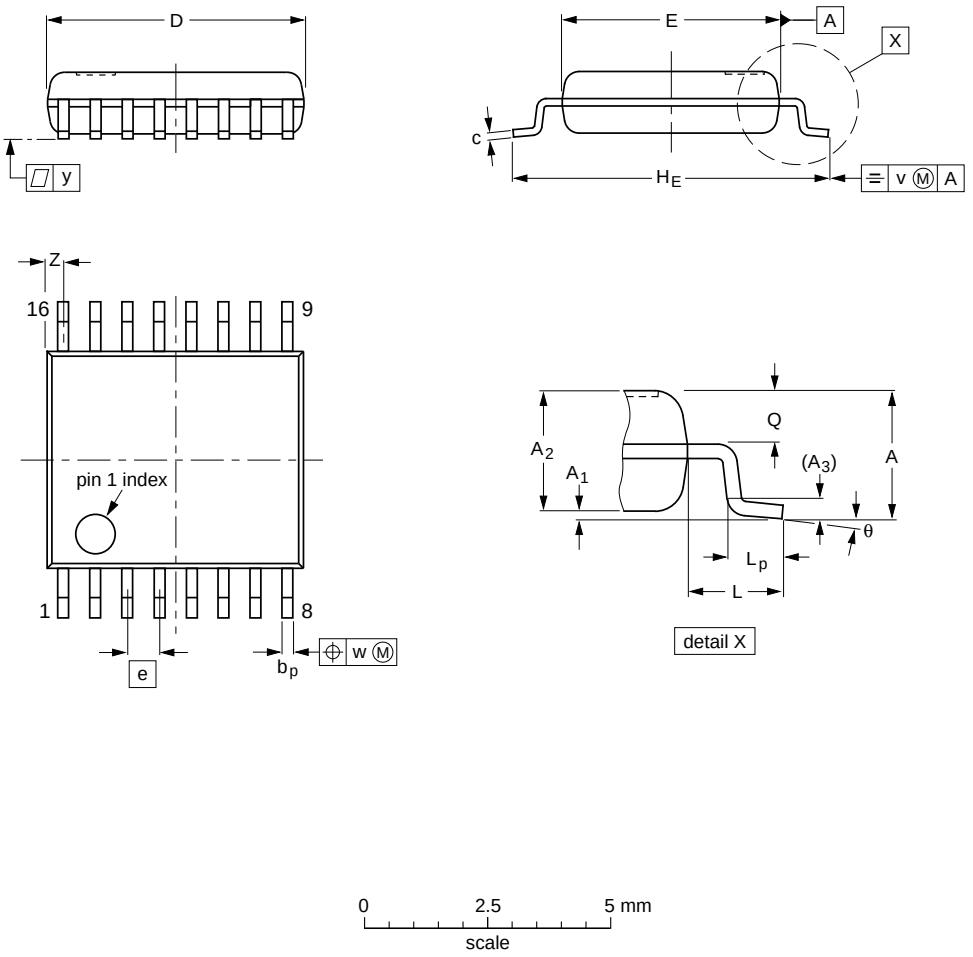
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm **SOT369-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1						~~94-04-20~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
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