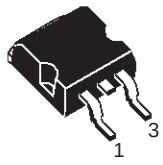
STB80NF55L-06

N - CHANNEL 55V - 0.005 Ω - 80A D^2PAK
STripFET™ POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STB80NF55L-06	55 V	< 0.0065 Ω	80 A

- TYPICAL $R_{DS(on)}$ = 0.005 Ω
- LOW THRESHOLD DRIVE
- LOGIC LEVEL DEVICE
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL

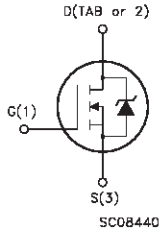


D^2PAK
TO-263
(Suffix "T4")

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	55	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	55	V
V_{GS}	Gate-source Voltage	± 20	V
I_D	Drain Current (continuous) at T_c = 25 °C	80	A
I_D	Drain Current (continuous) at T_c = 100 °C	57	A
I_{DM}(•)	Drain Current (pulsed)	320	A
P_{tot}	Total Dissipation at T_c = 25 °C	210	W
	Derating Factor	1.4	W/°C
E_{AS}(1)	Single Pulse Avalanche Energy	1	J
T_{stg}	Storage Temperature	-65 to 175	°C
T_j	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area (1) starting T_j = 25 °C, I_D =40A , V_{DD} = 30V

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case Max	0.71	$^oC/W$
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient Max	62.5	$^oC/W$
T_l	Maximum Lead Temperature For Soldering Purpose	300	^oC

ELECTRICAL CHARACTERISTICS (T_{case} = 25 ^oC unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	55			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0) V_{DS} = Max Rating V_{DS} = Max Rating T_c =125 ^oC				1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	1	1.6	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 40 A V_{GS} = 5 V I_D = 40 A		0.005 0.0055	0.0065 0.008	Ω Ω
$I_{D(on)}$	On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ V_{GS} = 10 V	80			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ I_D =18 A		20		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		7600 990 270		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 27 V I_D = 40 A R_G = 4.7 Ω V_{GS} = 4.5 V (Resistive Load, see fig. 3)		75 300		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 44 V I_D = 80 A V_{GS} = 5 V		97 25 46	100	nC nC nC

SWITCHING OFF

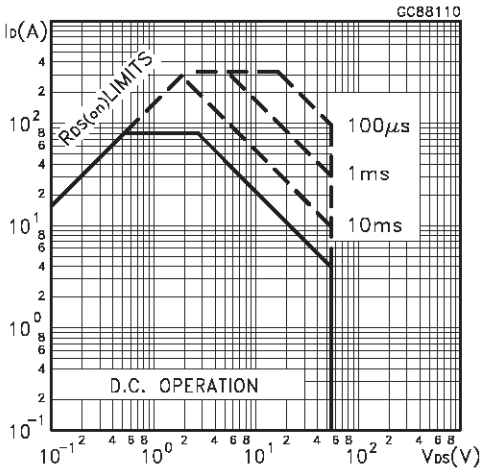
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 27 V I_D = 40 A R_G = 4.7 Ω V_{GS} = 4.5 V (Resistive Load, see fig. 3)		210 160		ns ns
$t_{d(off)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	Vclamp = 44 V I_D = 80 A R_G = 4.7 Ω V_{GS} = 4.5 V (Inductive Load, see fig. 5)		90 230 350		ns ns ns

SOURCE DRAIN DIODE

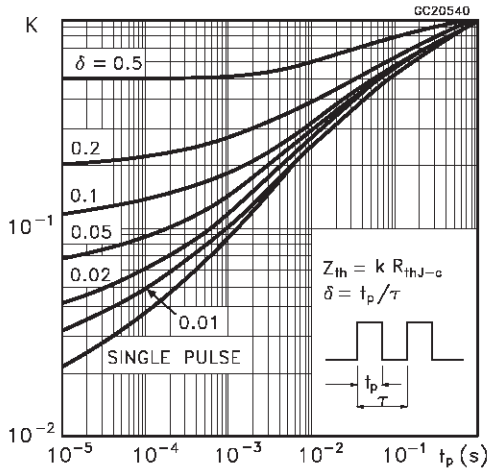
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				80 320	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 80 A V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 80 A di/dt = 100 A/µs V_{DD} = 25 V T_j = 150 °C (see test circuit, fig. 5)		75 190 5.1		ns nC A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

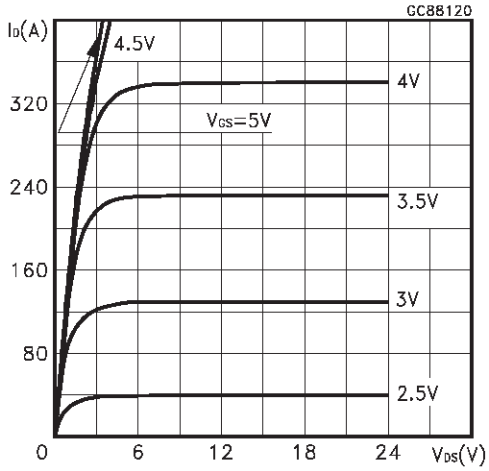
Safe Operating Area



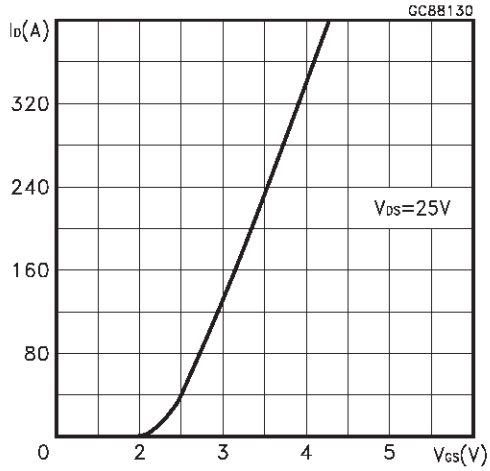
Thermal Impedance



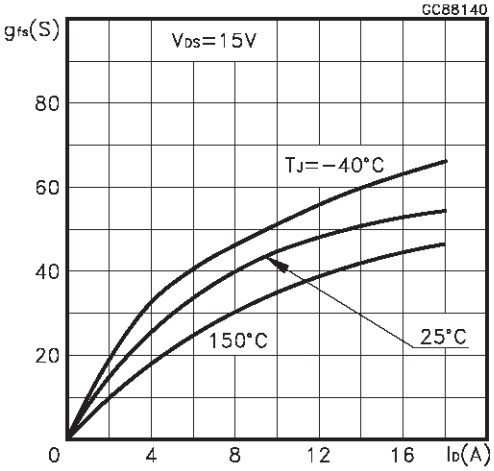
Output Characteristics



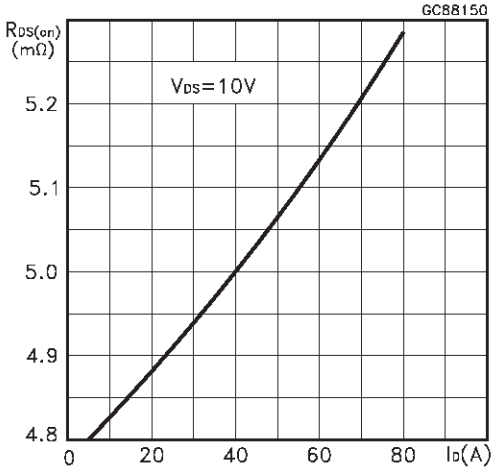
Transfer Characteristics



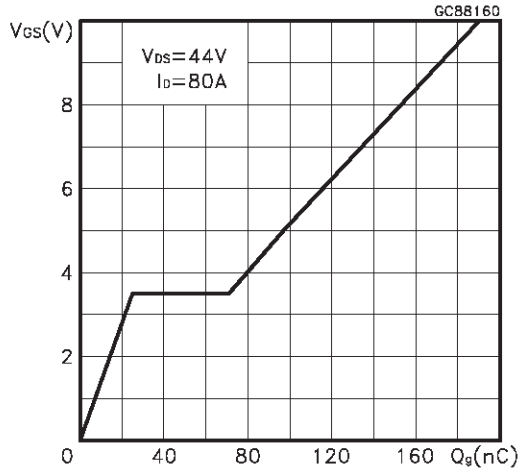
Transconductance



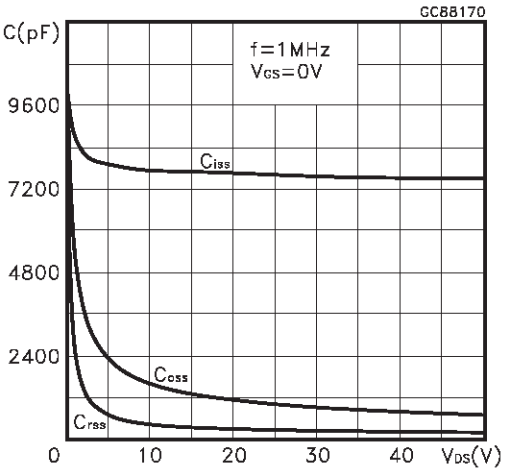
Static Drain-source On Resistance



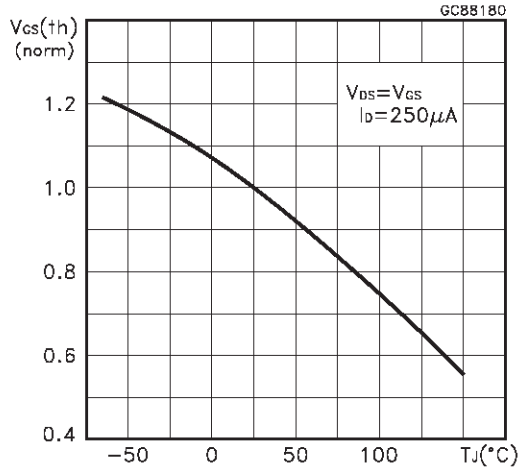
Gate Charge vs Gate-source Voltage



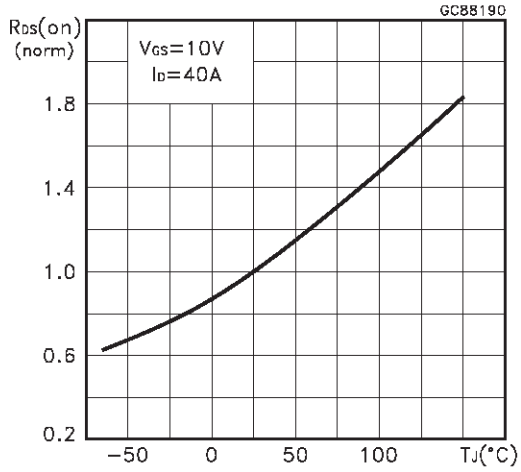
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

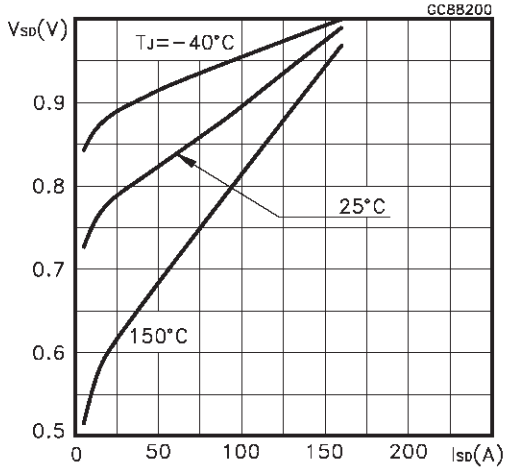


Fig. 1: Unclamped Inductive Load Test Circuit

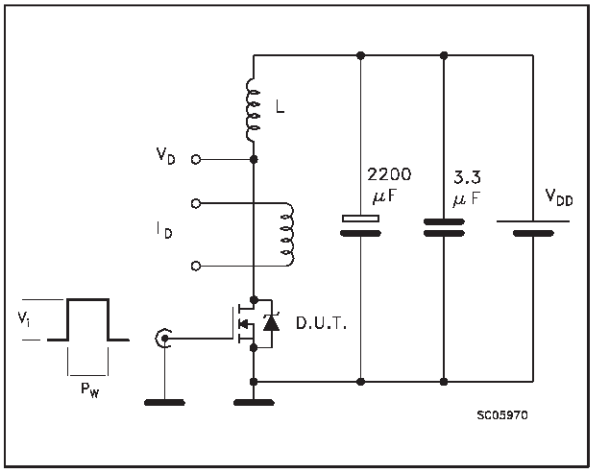


Fig. 2: Unclamped Inductive Waveform

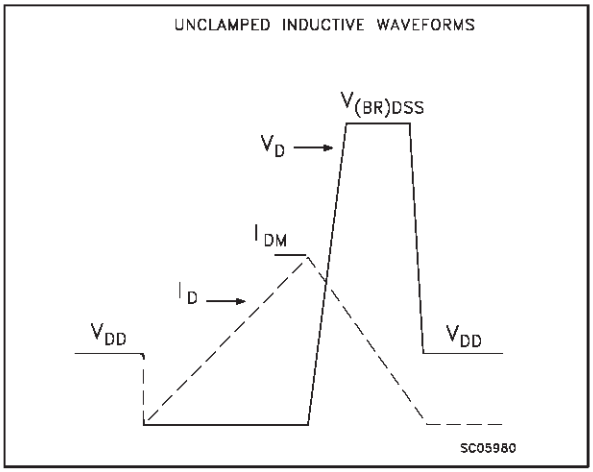


Fig. 3: Switching Times Test Circuits For Resistive Load

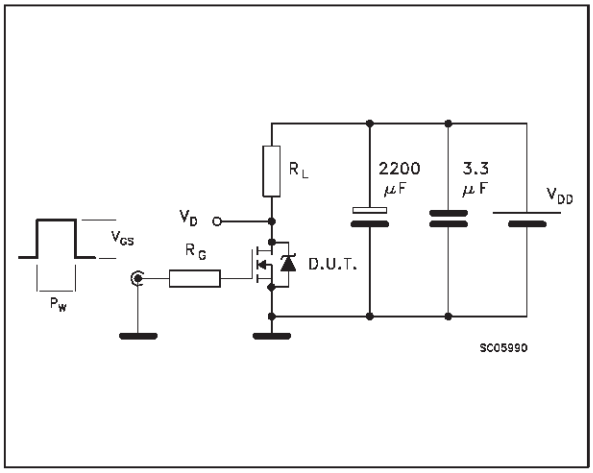


Fig. 4: Gate Charge test Circuit

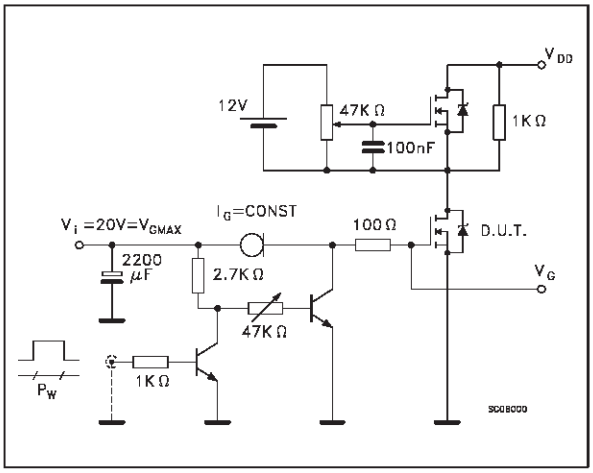
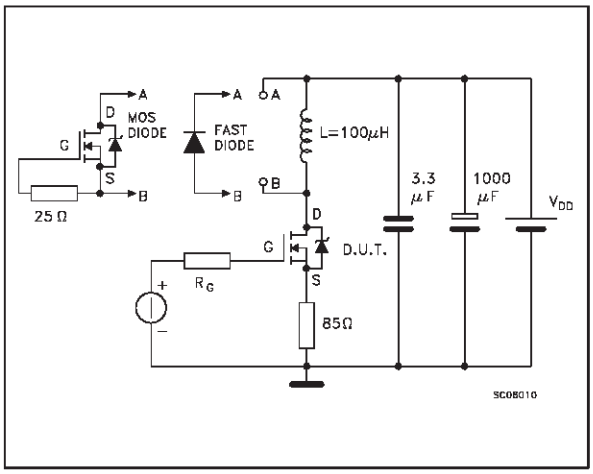
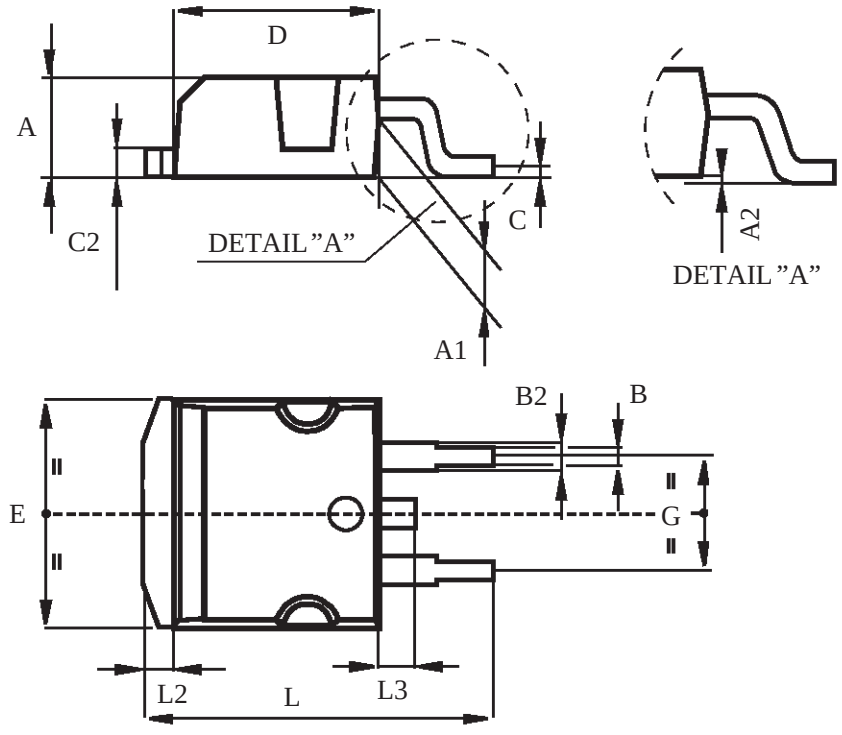


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-263 (D^2PAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.21		1.36	0.047		0.053
D	8.95		9.35	0.352		0.368
E	10		10.4	0.393		0.409
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068



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