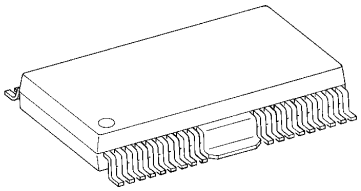
TENTATIVE TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62716F

16 BIT SHIFT REGISTER, LATCHES & CONSTANT CURRENT DRIVERS

The TB62716F is specifically designed for LED and LED DISPLAY constant current drivers.
This constant current output circuits is able to set up external resistor (I_{OUT} = 5~150 mA).
This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.
The devices consist of 16 bit shift register, latch, AND-GATE and Constant Current Drivers.



HSOP36-P-450-0.65

Weight : 1.22 g (Typ.)

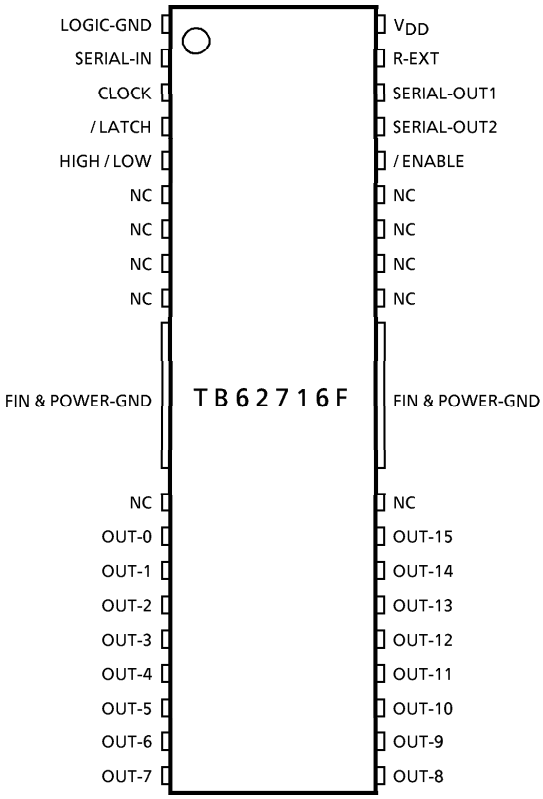
FEATURES

- Constant Current Output : Can set up all output current with one resister for 5 to 150 mA.
- Constant Output Current Matching :

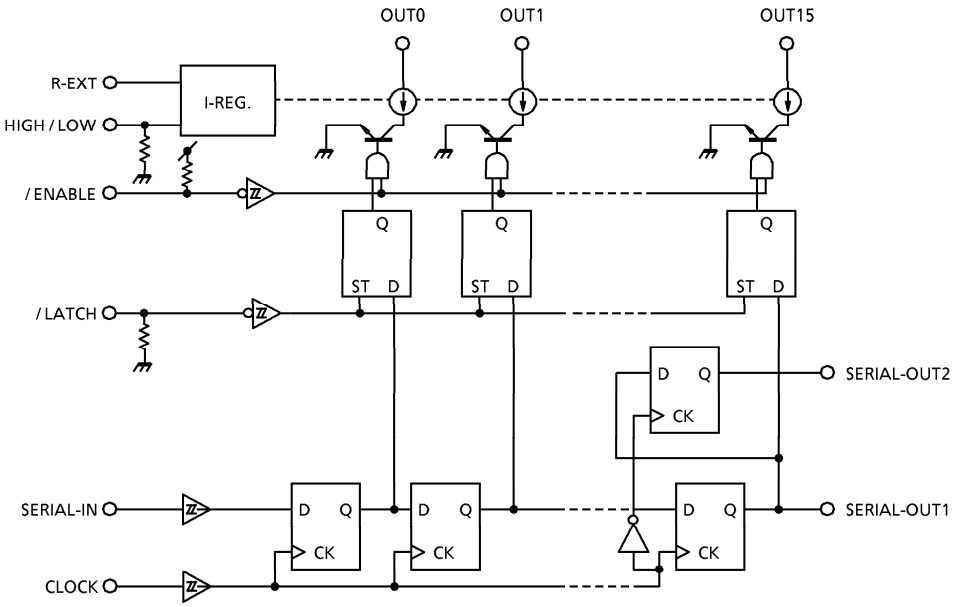
HIGH / LOW	OUTPUT-GND VOLTAGE	CURRENT MATCHING (BIT)	CURRENT MATCHING (LOT)	OUTPUT CURRENT (MAX.)
"L"	≧ 0.7 V	± 6.0%	± 15.0%	2~70 mA
"H"	≧ 1.0 V	± 6.0%	± 15.0%	50~150 mA

- Maximum Clock Frequency : f_{CLK} = 15 MHz (Cascade Connected Operate, T_{opr} = 25°C)
- 5 V C-MOS Compatible Input
- Package : HSOP36-P-375-0.80~0.8mmPitch~

PIN CONNECTION (Top view)



BLOCK DIAGRAM

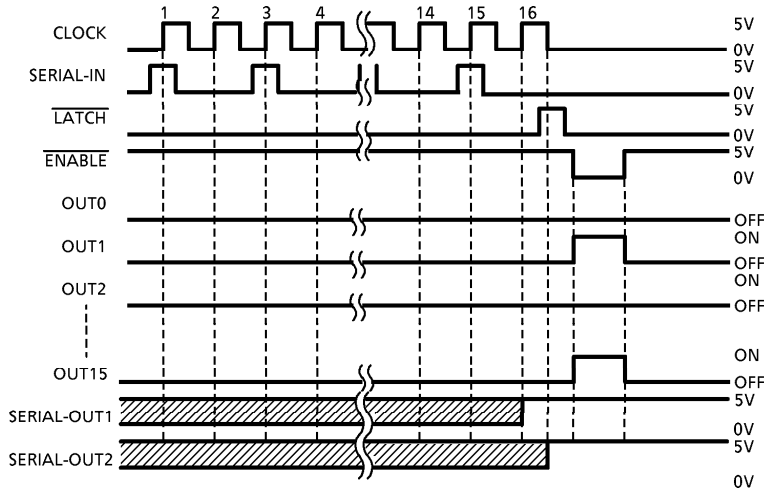


TRUTH TABLE

CLOCK	$\overline{LATCH}$	$\overline{ENABLE}$	SERIAL-IN	OUT0 ··· OUT5 ··· OUT7	SERIAL-OUT
UP	H	L	D_n	D_n ··· D_{n-7} ··· D_{n-15}	D_{n-15}
UP	L	L	D_n+1	No Change	D_{n-14}
UP	H	L	D_n+2	D_n+2 ··· D_{n-5} ··· D_{n-13}	D_{n-13}
DOWN	X	L	D_n+3	D_n+2 ··· D_{n-5} ··· D_{n-13}	D_{n-13}
DOWN	X	H	D_n+3	Off	D_{n-13}

(Note) OUT0~15 = on in case of D_n = H level and OUT0~15 = off in case of D_n = L level.
A resistor is connected with R-EXT and GND accompanied with outside, and it is necessary that a correct power supply voltage is supplied.

TIMING DIAGRAM



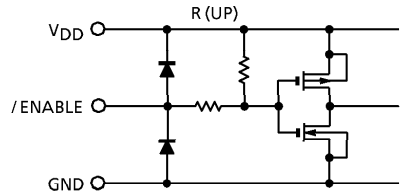
(Note) Latches are level sensitive, not rising edge sensitive and not syncronus CLOCK.
Input of LATCH-terminal to H level, data passes latches, and input to L level, data hold latches.
Input of ENABLE-terminal to H level, all output (OUT0~15) do off.

TERMINAL DISCRIPTION

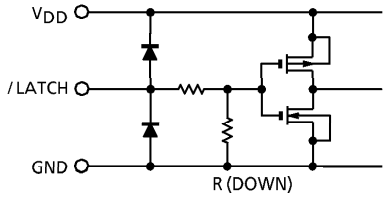
PIN No.	PIN NAME	FUNCTION
5	HIGH / LOW	It is the terminal which does switching for the big current / low current.
FIN	POWER-GND	GND terminal for current output.
1	LOGIC-GND	GND terminal for control logic.
2	SERIAL-IN	Input terminal of a serial-data shift-register.
3	CLOCK	Input terminal of a clock for data shift to up-edge.
4	/ LATCH	Input terminal of a data strobe. Latches passes data with "H" level input of LATCH-terminal, and hold data with "L" level input.
11~18 19~26	OUT0~15	Output terminals.
32	/ ENABLE	Input terminal of output enable. All outputs (OUT0~7) do off with "H" level input of ENABLE-termnal, and do on with "L" level input.
34	SERIAL-OUT	Output terminal of a serial-data for next SERIAL-IN terminal.
35	R-EXT	Input terminal of connects with a resister for to set up all output current.
36	V_{DD}	5 V Supply voltage terminal.

EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

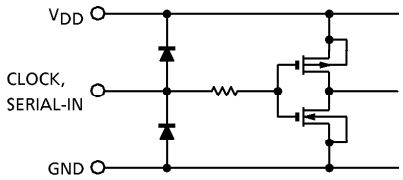
1. ENABLE terminal



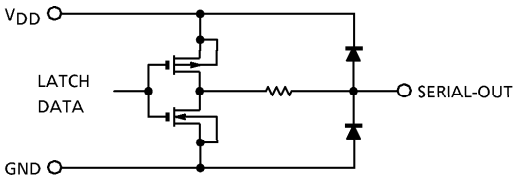
2. LATCH terminal



3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	0~7.0	V
Input Voltage	V_{IN}	−0.4~V_{DD} + 0.4	V
Output Current	I_{OUT}	+150 (HIGH / LOW = "H")	mA / ch
		+ 70 (HIGH / LOW = "L")	
Output Voltage	V_{OUT}	−0.5~17.0	V
Clock Frequency	f_{CLK}	15	MHz
GND Terminal Current	I_{GND}	1200	mA
Power Dissipation	P_{D1}	1.08 (FREE AIR, Ta = 25°C)	W
	P_{D2}	1.92 (ON PCB, Ta = 25°C)	
Thermal Resistance	$R_{th\ (j-a)}$	120 (Free Air) / 65 (On PCB)	°C / W
	$R_{th\ (j-c)}$	12	
Operating Temperature	T_{opr}	−40~+85	°C
Storage Temperature	T_{stg}	−55~+150	°C

(Note) Ambient temperature delated above 25°C in the proportion of 15.4 mW / °C (On PCB)

RECOMMENDED OPERATING CONDITION (Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	—	4.5	5.0	5.5	V
Output Voltage	V_{OUT}	—	—	—	15.0	V
Output Current	I_{OUT1}	DC 1 circuit (HIGH / LOW = "H")	50	—	130	mA
	I_{OUT2}	DC 1 circuit (HIGH / LOW = "L")	2	—	60	
	I_{OH}	SERIAL-OUT1, 2	—	—	−1.0	mA
	I_{OL}	SERIAL-OUT1, 2	—	—	1.0	
Input Voltage	V_{IH}	V_{DD} = 4.5~5.5 V	0.7 V_{DD}	—	V_{DD} + 0.3	V
	V_{IL}		−0.3	—	0.3 V_{DD}	
LATCH Pulse Width	t_{W} / LATCH		100	—	—	ns
CLOCK Pulse Width	t_{W} CLOCK		50	—	—	
ENABLE Pulse Width	t_{W} / ENABLE		1000	—	—	
Set-up Time for DATA	$t_{setup\ (D)}$		60	—	—	
Hold Time for DATA	$t_{hold\ (D)}$		20	—	—	
Set-up Time for LATCH	$t_{setup\ (L)}$		100	—	—	
Hold Time for ENABLE	$t_{hold\ (L)}$		60	—	—	
Clock Frequency	f_{CLK}	Cascade operation	10.0	—	—	MHz
Power Dissipation	P_D	Ta = 85°C (FN-type On PCB)	—	—	1.00	W

ELECTRICAL CHARACTERISTICS (Ta = 25°C unless otherwise noted)

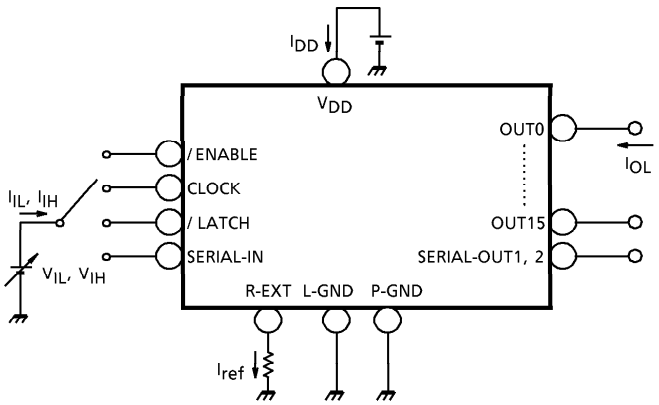
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" level	V_{IH}	1	—		0.7 V_{DD}	—	V_{DD}	V
	"L" level	V_{IL}		—		GND	—	0.3 V_{DD}	
Output Leakage Current		I_{OH}		V_{OH} = 15.0 V		—	—	10	μA
Output Voltage	SERIAL -OUT1, 2	V_{OL}		I_{OL} = + 1.0 mA		—	—	0.4	V
		V_{OH}		I_{OH} = − 1.0 mA		4.6	—	—	
Output Current 1		I_{OL1}		V_{OUT} = 0.7 V	R_{EXT} = 520 Ω, HIGH / LOW = "L"	34.3	40.3	46.8	mA
	Current Skew	ΔI_{OL1}				—	± 1.5	± 6.0	%
Output Current 2		I_{OL2}		V_{OUT} = 1.0 V	R_{EXT} = 160 Ω, HIGH / LOW = "H"	107.1	126.0	144.9	mA
	Current Skew	ΔI_{OL2}				—	± 1.5	± 6.0	%
Supply Voltage Regulation		% / V_{DD}		Ta = − 40~85°C		—	1.5	5.0	% / V
Pull-up Resistor		R_{IN} (up)		—		100	200	400	kΩ
Pull-down Resistor		R_{IN} (down)		—		100	200	400	kΩ
Supply Current	"OFF"	I_{DD} (off) 1		R_{EXT} = OPEN, OUT0~8 = off		—	1.0	2.0	mA
		I_{DD} (off) 2		R_{EXT} = 500 Ω, OUT0~8 = off		7.0	12.0	16.0	
		I_{DD} (off) 3		R_{EXT} = 160 Ω, OUT0~8 = off		13.0	20.0	30.0	
	"ON"	I_{DD} (on) 1		R_{EXT} = 500 Ω, OUT0~8 = on		—	23.1	40.5	
		I_{DD} (on) 2		R_{EXT} = 160 Ω, OUT0~8 = on		—	33.0	62.1	

SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise noted)

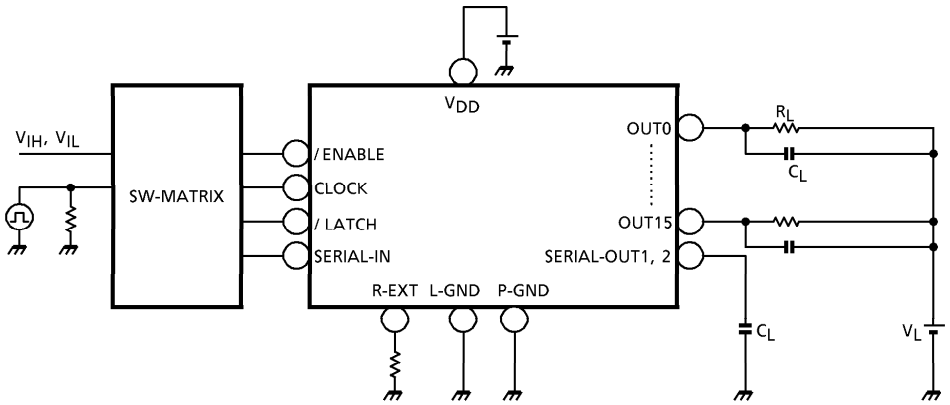
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	CLK-OUTn	t_{pLH}	—	V_{DD} = 5.0 V V_{CE} = 1.0 V V_{IH} = V_{DD} V_{IL} = GND R_{EXT} = 160 Ω, I_{OUT} = 126 mA, V_L = 3.0 V R_L = 32 Ω C_L = 10.5 pF tor : 10% to 90% tof : 90% to 10% t_{pLH} : 50% to 10% t_{pHL} : 50% to 90%	—	500	1000	ns
	LATCH-OUTn				—	500	1000	
	ENABLE-OUTn				—	500	1000	
	CLK-SOUT				—	30	70	
Propagation Delay Time ("H" to "L")	SIN-OUTn	t_{pHL}	—		—	500	1000	ns
	LATCH-OUTn				—	500	1000	
	ENABLE-OUTn				—	500	1000	
	CLK-SOUT				—	30	70	
Pulse Width	CLK	$t_{w\ CLK}$, CLK	—		—	20	30	ns
	LATCH	$t_{w\ LAT}$, LAT	—		—	10	25	ns
Set-up Time for LATCH / SIN	L-H	t_{setup}LAT / SIN	—		—	25	50	ns
	H-L				—	25	50	ns
Hold Time for LATCH / SIN	L-H	t_{hold} LAT / SIN	—		—	0	15	ns
	H-L				—	0	15	ns
Maximum CLOCK Rise Time		t_r	—		—	—	10	μs
Maximum CLOCK Fall Time		t_f	—		—	—	10	
Output Rise Time		t_{or}	—		300	600	1000	ns
Output Fall Time		t_{of}	—		300	600	1000	

TEST CIRCUIT

DC CHARACTERISTIC

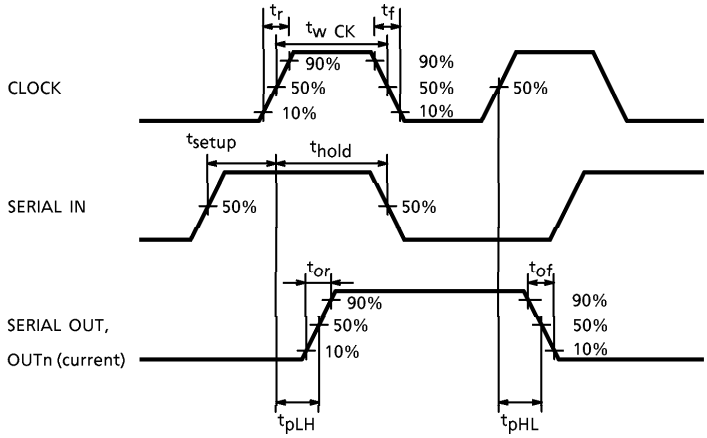


AC CHARACTERISTIC

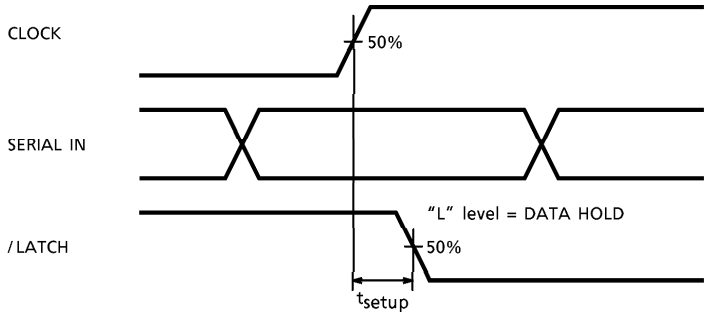


TIMING WAVEFORM

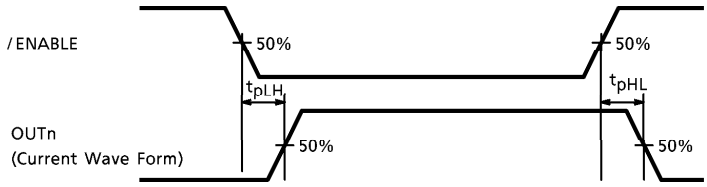
1. CLOCK-SERIAL OUT, OUTn



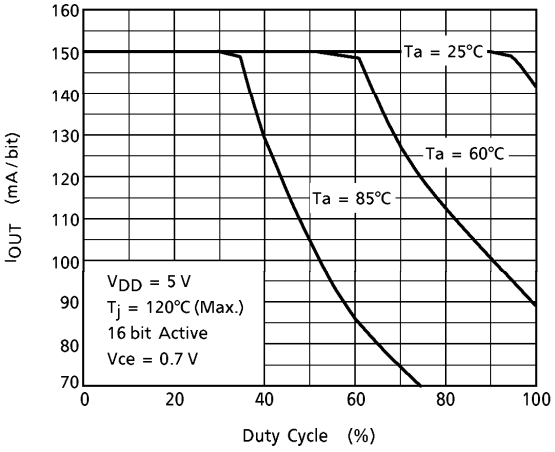
2. CLOCK- / LATCH



3. ENABLE-OUTn



I_{OUT} – Duty Cycle (TB62716F)
HIGH / LOW = "H"



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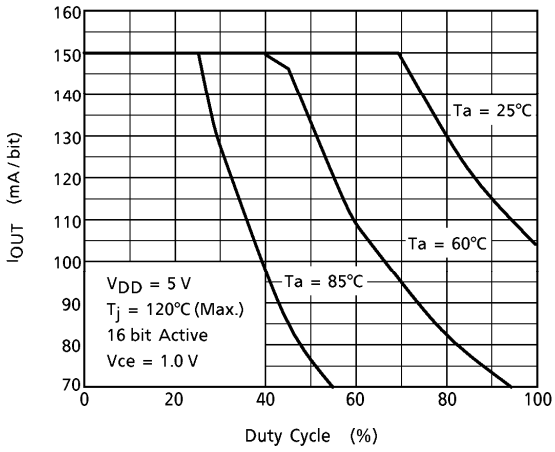
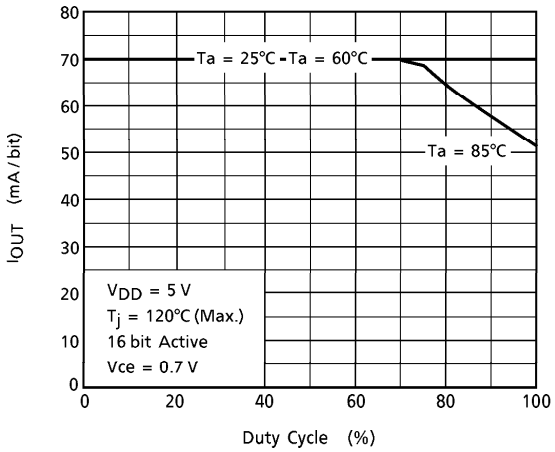
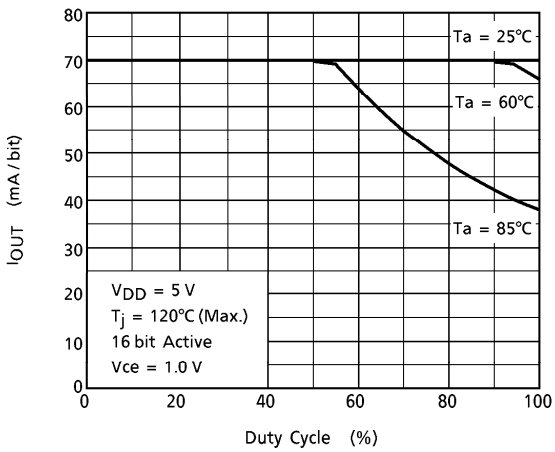
HIGH / LOW = "H"



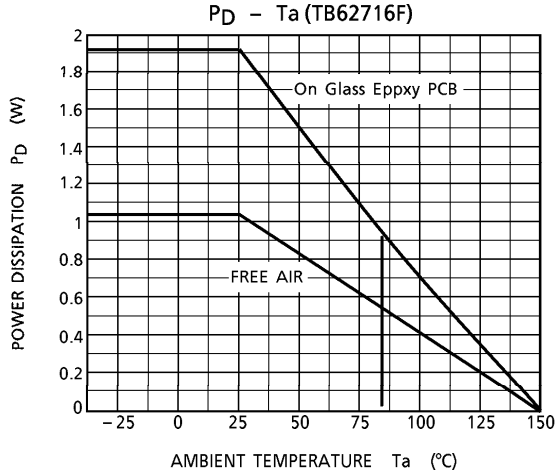
I_{OUT} – Duty Cycle (TB62716F)
HIGH / LOW = "L"



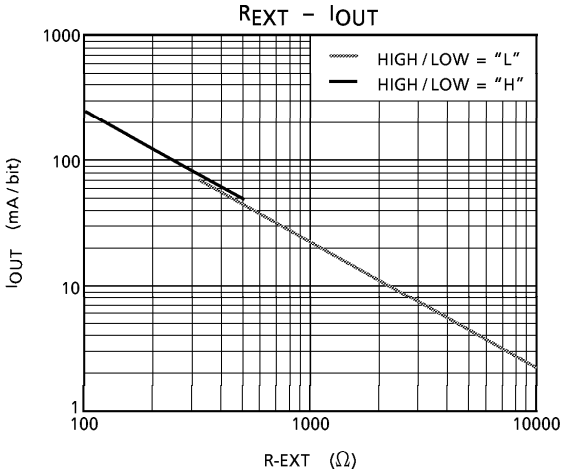
I_{OUT} – Duty Cycle (TB62716F)
HIGH / LOW = "L"

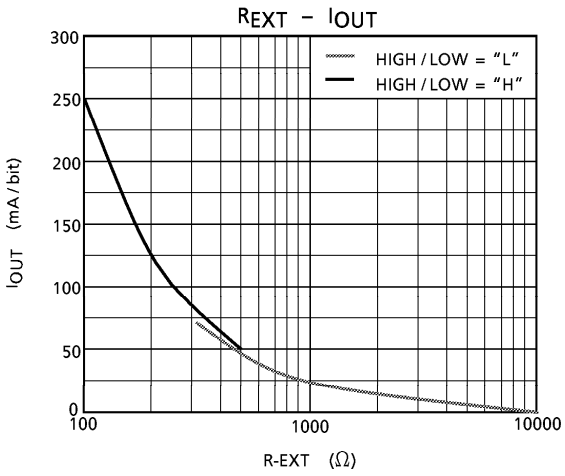


P_D – Ta (TB62716F)



LED DRIVER TB6270X SERIES APPLICATION NOTE





Total supply voltage (V_{LED})

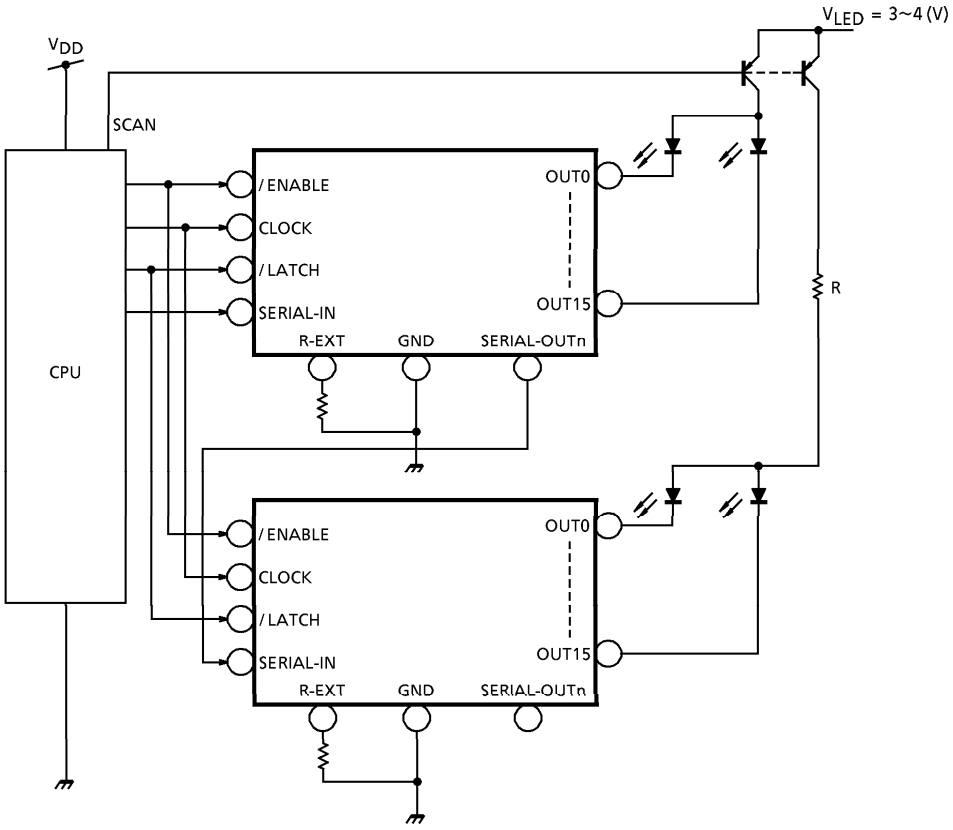
This device can operate 0.7~1.0 V (V_O).
When a higher voltage is input to the device, the excess voltage is consumed inside the device, that leads to power dissipation.
In order to minimize power dissipation and loss, we would like to recommend to set the total supply voltage as shown below,

V_{LED} (total supply voltage) = V_{CE} (T_r V_{sat}) + V_f (LED Forward voltage) + V_O (I_C supply voltage)

When the total supply is too high considering the power dissipation of this device, an additional R can decrease the supply voltage.

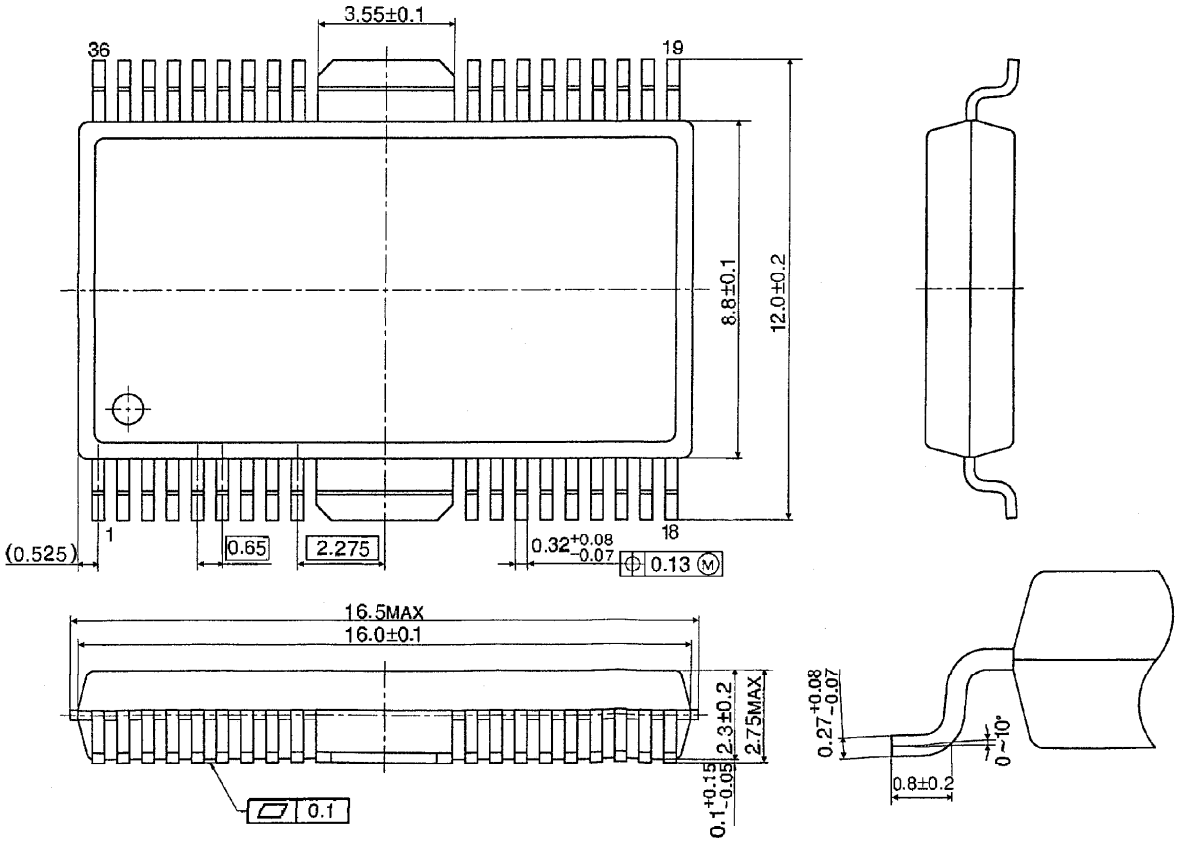
Pattern Layout

This device owns only one ground pin that means signal ground pin and power ground pin are common.
If ground pattern layout contains large inductance and impedance, and the voltage between ground and LATCH, CLOCK terminals exceeds 2.5 V by switching noise in operation, this device may miss-operate.
So we would like you to pay attention pattern layout to minimize inductance.



OUTLINE DRAWING

HSOP36-P-450-0.65 Unit : mm



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