PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

M37735MHLXXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37735MHLXXXHP is a single-chip microcomputer using the 7700 Family core. This single-chip microcomputer has a CPU and a bus interface unit. The CPU is a 16-bit parallel processor that can be an 8-bit parallel processor, and the bus interface unit enhances the memory access efficiency to execute instructions fast. This microcomputer also includes a 32 kHz oscillation circuit, in addition to the ROM, RAM, multiple-function timers, serial I/O, A-D converter, and so on.

Its strong points are the low power dissipation, the low supply voltage and the small package.

FEATURES

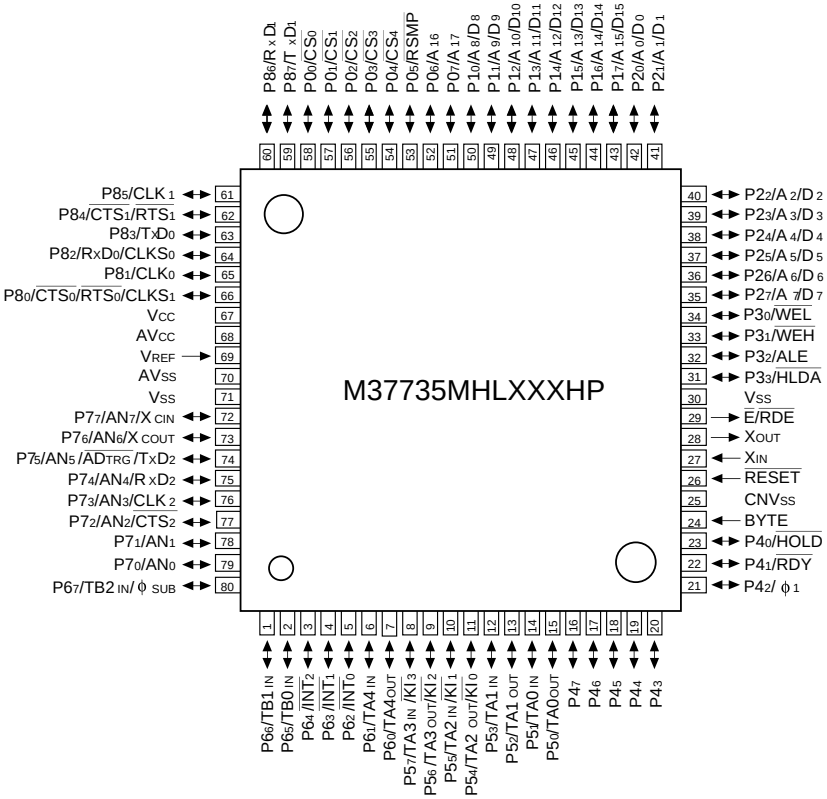
- Number of basic instructions 103
- Memory size ROM ..... 124 Kbytes
  RAM ..... 3968 bytes
- Instruction execution time
  The fastest instruction at 12 MHz frequency ..... 333 ns
- Single power supply ..... 2.7–5.5 V
- Low power dissipation (At 3 V supply voltage, 12 MHz frequency)
  ..... 9 mW (Typ.)
- Interrupts ..... 19 types, 7 levels
- Multiple-function 16-bit timer ..... 5 + 3
- Serial I/O (UART or clock synchronous) 3
- 10-bit A-D converter ..... 8-channel inputs
- 12-bit watchdog timer
- Programmable input/output
  (ports P0, P1, P2, P3, P4, P5, P6, P7, P8) 68
- Clock generating circuit ..... 2 circuits built-in
- Small package ..... 80-pin plastic molded fine-pitch QFP
  (80P6D-A;0.5 mm lead pitch)

APPLICATION

Control devices for general commercial equipment such as office automation, office equipment, personal information equipment, and so on.

Control devices for general industrial equipment such as communication equipment, and so on.

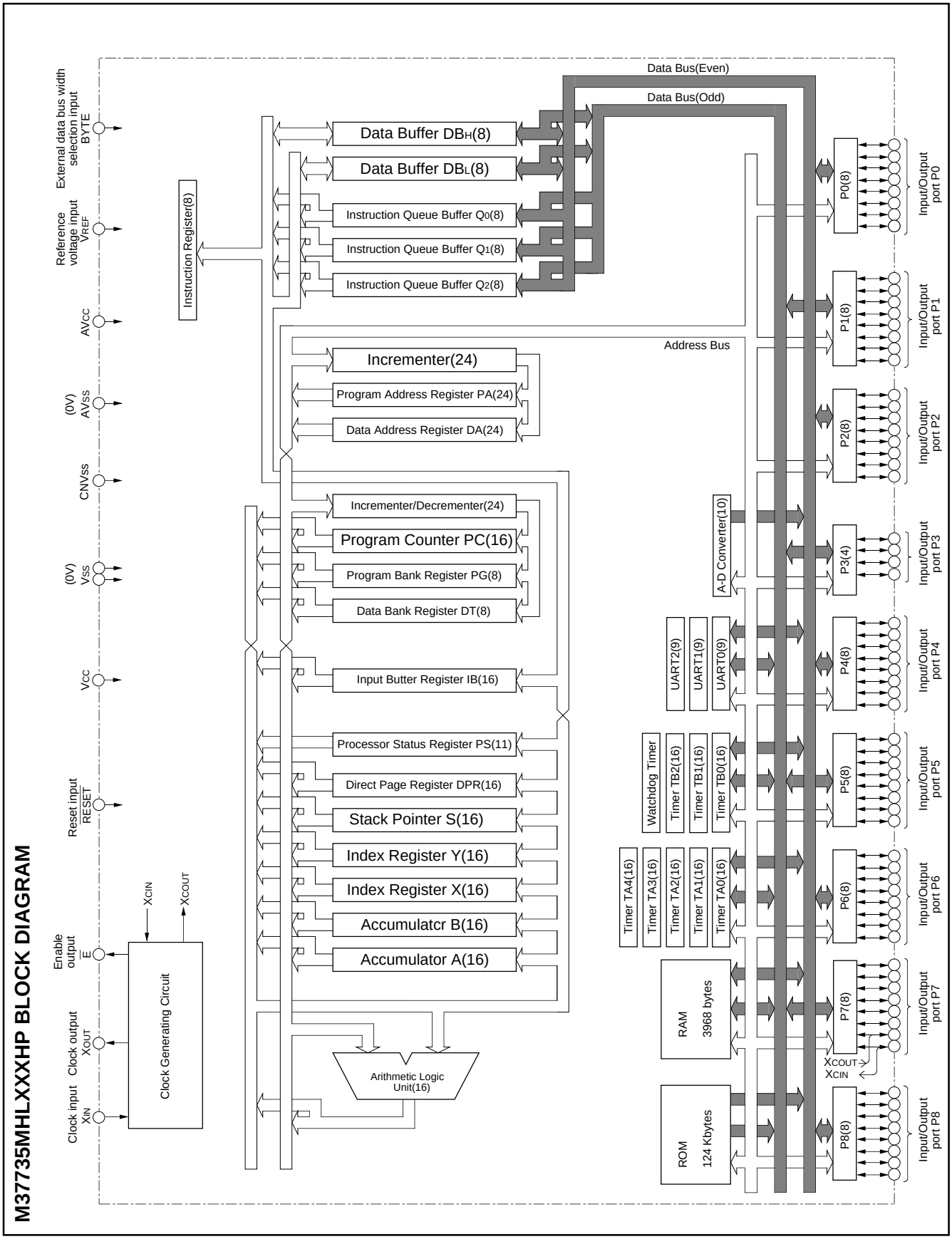
PIN CONFIGURATION (TOP VIEW)



Outline 80P6D-A, 80P6Q-A

MITSUBISHI ELECTRIC

M37735MHLXXXHP BLOCK DIAGRAM



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FUNCTIONS OF M37735MHLXXXHP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		333 ns (the fastest instruction at external clock 12 MHz frequency)
Memory size	ROM	124 Kbytes
	RAM	3968 bytes
Input/Output ports	P0 – P2, P4 – P8	8-bit × 8
	P3	4-bit × 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit × 5
	TB0, TB1, TB2	16-bit × 3
Serial I/O		(UART or clock synchronous serial I/O) × 3
A-D converter		10-bit × 1 (8 channels)
Watchdog timer		12-bit × 1
Interrupts		3 external types, 16 internal types Each interrupt can be set to the priority level (0 – 7.)
Clock generating circuit		2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Supply voltage		2.7 – 5.5 V
Power dissipation		9 mW (at 3 V supply voltage, external clock 12 MHz frequency)
		22.5 mW (at 5 V supply voltage, external clock 12 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 1 Mbytes
Operating temperature range		–40 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		80-pin plastic molded fine-pitch QFP (80P6D-A;0.5 mm lead pitch)

PRELIMINARY
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PIN DESCRIPTION

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source		Apply 2.7 – 5.5 V to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode.
$\overline{RESET}$	Reset input	Input	When "L" level is applied to this pin, the microcomputer enters the reset state.
X_{IN}	Clock input	Input	These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between X_{IN} and X_{OUT}. When an external clock is used, the clock source should be connected to the X_{IN} pin, and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	In the single-chip mode, this pin functions as the enable signal output pin which indicates the access status in the internal bus. In the memory expansion mode or the microprocessor mode, this pin functions as the $\overline{RDE}$ signal output pin.
BYTE	External data bus width selection input	Input	In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input.
AVcc, AVss	Analog power source input		Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
$P0_0$ – $P0_7$	I/O port P0	I/O	In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset. In the memory expansion mode or the microprocessor mode, these pins output $\overline{CS_0}$ – $\overline{CS_4}$, $\overline{RSMP}$ signals, and address (A_{16}, A_{17}).
$P1_0$ – $P1_7$	I/O port P1	I/O	In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data (D_8 – D_{15}) is input/output or an address (A_8 – A_{15}) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address (A_8 – A_{15}) is output.
$P2_0$ – $P2_7$	I/O port P2	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data (D_0 – D_7) is input/output or an address (A_0 – A_7) is output.
$P3_0$ – $P3_3$	I/O port P3	I/O	In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, $\overline{WEL}$, $\overline{WEH}$, ALE, and $\overline{HLDA}$ signals are output.
$P4_0$ – $P4_7$	I/O port P4	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, $P4_0$, $P4_1$, and $P4_2$ become $\overline{HOLD}$ and $\overline{RDY}$ input pins, and clock ϕ_1 output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, $P4_2$ also functions as an I/O port.
$P5_0$ – $P5_7$	I/O port P5	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3 and input pins for key input interrupt input ($\overline{KI_0}$ – $\overline{KI_3}$).
$P6_0$ – $P6_7$	I/O port P6	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input ($\overline{INT_0}$ – $\overline{INT_2}$) and input pins for timers B0 to B2. $P6_7$ also functions as sub-clock ϕ_{SUB} output pin.
$P7_0$ – $P7_7$	I/O port P7	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. $P7_2$ to $P7_5$ also function as I/O pins for UART2. Additionally, $P7_6$ and $P7_7$ have the function as the output pin (X_{COUT}) and the input pin (X_{CIN}) of the sub-clock (32 kHz) oscillation circuit, respectively. When $P7_6$ and $P7_7$ are used as the X_{COUT} and X_{CIN} pins, connect a resonator or an oscillator between the both.
$P8_0$ – $P8_7$	I/O port P8	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1.

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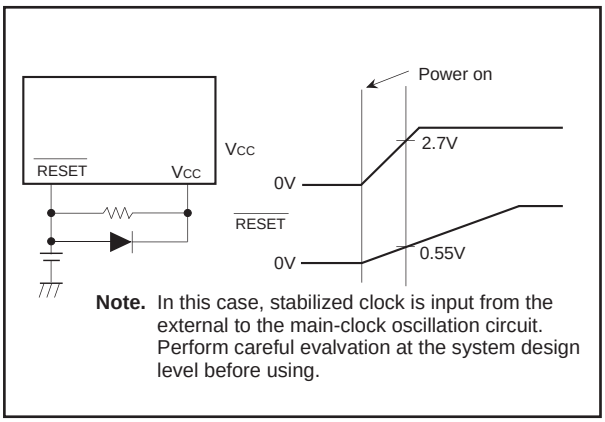
BASIC FUNCTION BLOCKS

The M37735MHLXXXHP has the same functions as the M37735MHBXXXFP except for the package and the reset circuit. Refer to the section on the M37735MHBXXXFP.

RESET CIRCUIT

The microcomputer is released from the reset state when the $\overline{\text{RESET}}$ pin is returned to "H" level after holding it at "L" level with the power source voltage at 2.7 – 5.5 V. Program execution starts at the address formed by setting address A_{23} – A_{16} to 00_{16}, A_{15} – A_8 to the contents of address $FFFF_{16}$, and A_7 – A_0 to the contents of address $FFFE_{16}$.
Figure 1 shows an example of a reset circuit. When the stabilized clock is input from the external to the main-clock oscillation circuit, the reset input voltage must be 0.55 V or less when the power source voltage reaches 2.7 V. When a resonator/oscillator is connected to the main-clock oscillation circuit, change the reset input voltage from "L" to "H" after the main-clock oscillation is fully stabilized.
The status of the internal registers during reset is the same as the M37735MHBXXXFP's.



Note. In this case, stabilized clock is input from the external to the main-clock oscillation circuit. Perform careful evalvation at the system design level before using.

Fig. 1 Example of a reset circuit

ADDRESSING MODES

The M37735MHLXXXHP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details.

MACHINE INSTRUCTION LIST

The M37735MHLXXXHP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.

DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.
(1) M37735MHLXXXHP mask ROM order confirmation form
(2) 80P6D, 80P6Q mark specification form
(3) ROM data (EPROM 3 sets)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Power source voltage		–0.3 to +7	V
AVcc	Analog power source voltage		–0.3 to +7	V
V_I	Input voltage $\overline{RESET}$, CNVss, BYTE		–0.3 to +12	V
V_I	Input voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, V_{REF}, X_{IN}		–0.3 to Vcc + 0.3	V
V_O	Output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, X_{OUT}, $\overline{E}$		–0.3 to Vcc + 0.3	V
P_d	Power dissipation	Ta = 25 °C	200	mW
T_{opr}	Operating temperature		–40 to +85	°C
T_{stg}	Storage temperature		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (Vcc = 2.7 – 5.5 V, Ta = –40 to +85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
Vcc	Power source voltage	f(X_{IN}) : Operating	2.7		5.5	V
		f(X_{IN}) : Stopped, f(X_{CIN}) = 32.768 kHz	2.7		5.5	
AVcc	Analog power source voltage			Vcc		V
Vss	Power source voltage			0		V
AVss	Analog power source voltage			0		V
V_{IH}	High-level input voltage $P0_0$ – $P0_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, X_{CIN} (Note 3)		0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in single-chip mode)		0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in memory expansion mode and microprocessor mode)		0.5 Vcc		Vcc	V
V_{IL}	Low-level input voltage $P0_0$ – $P0_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, X_{CIN} (Note 3)		0		0.2Vcc	V
V_{IL}	Low-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in single-chip mode)		0		0.2Vcc	V
V_{IL}	Low-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in memory expansion mode and microprocessor mode)		0		0.16Vcc	V
$I_{OH(peak)}$	High-level peak output current $P0_0$ – $P0_7$, $P1_0$– $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$				–10	mA
$I_{OH(avg)}$	High-level average output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$				–5	mA
$I_{OL(peak)}$	Low-level peak output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_3$, $P5_4$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$				10	mA
$I_{OL(peak)}$	Low-level peak output current $P4_4$ – $P4_7$, $P5_0$ – $P5_3$				16	mA
$I_{OL(avg)}$	Low-level average output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_3$, $P5_4$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$				5	mA
$I_{OL(avg)}$	Low-level average output current $P4_4$ – $P4_7$, $P5_0$ – $P5_3$				12	mA
f(X_{IN})	Main-clock oscillation frequency (Note 4)				12	MHz
f(X_{CIN})	Sub-clock oscillation frequency			32.768	50	kHz

Notes 1. Average output current is the average value of a 100 ms interval.

2. The sum of $I_{OL(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of $I_{OH(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of $I_{OL(peak)}$ for ports P4, P5, P6, and P7 must be 100 mA or less, and the sum of $I_{OH(peak)}$ for ports P4, P5, P6, and P7 must be 80 mA or less.

3. Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = "1".

4. The maximum value of f(X_{IN}) = 6 MHz when the main clock division selection bit = "1".

PRELIMINARY
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ELECTRICAL CHARACTERISTICS (Vcc = 5 V, Vss = 0 V, Ta = –40 to +85 °C, f(XIN) = 12 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
VOH	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87	VCC = 5 V, IOH = –10 mA		3			V
		VCC = 3 V, IOH = –1 mA		2.5			
VOH	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	VCC = 5 V, IOH = –400 µA		4.7			V
VOH	High-level output voltage P30 – P32	VCC = 5 V, IOH = –10 mA		3.1			V
		VCC = 5 V, IOH = –400 µA		4.8			
		VCC = 3 V, IOH = –1 mA		2.6			
VOH	High-level output voltage $\overline{E}$	VCC = 5 V, IOH = –10 mA		3.4			V
		VCC = 5 V, IOH = –400 µA		4.8			
		VCC = 3 V, IOH = –1 mA		2.6			
VOL	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87	VCC = 5 V, IOL = 10 mA				2	V
		VCC = 3 V, IOL = 1 mA				0.5	
VOL	Low-level output voltage P44 – P47, P50 – P53	VCC = 5 V, IOL = 16 mA				1.8	V
		VCC = 3 V, IOL = 10 mA				1.5	
VOL	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	VCC = 5 V, IOL = 2 mA				0.45	V
VOL	Low-level output voltage P30 – P32	VCC = 5 V, IOL = 10 mA				1.9	V
		VCC = 5 V, IOL = 2 mA				0.43	
		VCC = 3 V, IOL = 1 mA				0.4	
VOL	Low-level output voltage $\overline{E}$	VCC = 5 V, IOL = 10 mA				1.6	V
		VCC = 5 V, IOL = 2 mA				0.4	
		VCC = 3 V, IOL = 1 mA				0.4	
VT+ – VT–	Hysteresis $\overline{HOLD}$, $\overline{RDY}$, TA0IN – TA4IN, TB0IN – TB2IN, $\overline{INT0}$ – $\overline{INT2}$, $\overline{ADTRG}$, $\overline{CTS0}$, $\overline{CTS1}$, $\overline{CTS2}$, CLK0, CLK1, CLK2, $\overline{KI0}$ – $\overline{KI3}$	VCC = 5 V		0.4		1	V
		VCC = 3 V		0.1		0.7	
VT+ – VT–	Hysteresis $\overline{RESET}$	VCC = 5 V		0.2		0.5	V
		VCC = 3 V		0.1		0.4	
VT+ – VT–	Hysteresis XIN	VCC = 5 V		0.1		0.4	V
		VCC = 3 V		0.06		0.26	
VT+ – VT–	Hysteresis XCIN (When external clock is input)	VCC = 5 V		0.1		0.4	V
		VCC = 3 V		0.06		0.26	
IIH	High-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, XIN, $\overline{RESET}$, CNVss, BYTE	VCC = 5 V, VI = 5 V				5	µA
		VCC = 3 V, VI = 3 V				4	
IIL	Low-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P53, P60, P61, P65 – P67, P70 – P77, P80 – P87, XIN, $\overline{RESET}$, CNVss, BYTE	VCC = 5 V, VI = 0 V				–5	µA
		VCC = 3 V, VI = 0 V				–4	
IIL	Low-level input current P54 – P57, P62 – P64	VI = 0 V, without a pull-up transistor	VCC = 5 V			–5	µA
			VCC = 3 V			–4	
		VI = 0 V, with a pull-up transistor	VCC = 5 V	–0.25	–0.5	–1.0	mA
			VCC = 3 V	–0.08	–0.18	–0.35	
VRAM	RAM hold voltage	When clock is stopped.		2			V

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, V_{SS} = 0 V, Ta = –40 to +85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	When single-chip mode, output pins are open, and other pins are V_{SS}.	V_{CC} = 5 V, $f(X_{IN})$ = 12 MHz (square waveform), ($f(f_2)$ = 6 MHz), $f(X_{CIN})$ = 32.768 kHz, in operating (Note 1)		4.5	9	mA
			V_{CC} = 3 V, $f(X_{IN})$ = 12 MHz (square waveform), ($f(f_2)$ = 6 MHz), $f(X_{CIN})$ = 32.768 kHz, in operating (Note 1)		3	6	mA
			V_{CC} = 3 V, $f(X_{IN})$ = 12 MHz (square waveform), ($f(f_2)$ = 0.75 MHz), $f(X_{CIN})$: Stopped, in operating		0.4	0.8	mA
			V_{CC} = 3 V, $f(X_{IN})$ = 12 MHz (square waveform), $f(X_{CIN})$ = 32.768 kHz, when a WIT instruction is executed (Note 2)		6	12	µA
			V_{CC} = 3 V, $f(X_{IN})$: Stopped, $f(X_{CIN})$ = 32.768 kHz, in operating (Note 3)		30	60	µA
			V_{CC} = 3 V, $f(X_{IN})$: Stopped, $f(X_{CIN})$ = 32.768 kHz, when a WIT instruction is executed (Note 4)		3	6	µA
			Ta = 25 °C, when clock is stopped			1	µA
			Ta = 85 °C, when clock is stopped			20	µA

Notes 1. This applies when the main clock external input selection bit = “1”, the main clock division selection bit = “0”, and the signal output stop bit = “1”.

2. This applies when the main clock external input selection bit = “1” and the system clock stop bit at wait state = “1”.

3. This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.

4. This applies when the X_{COUT} drivability selection bit = “0” and the system clock stop bit at wait state = “1”.

A–D CONVERTER CHARACTERISTICS

(V_{CC} = AV_{CC} = 5 V, V_{SS} = AV_{SS} = 0 V, Ta = –40 to +85 °C, $f(X_{IN})$ = 12 MHz, unless otherwise noted (Note))

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V_{REF} = V_{CC}			10	Bits
—	Absolute accuracy	V_{REF} = V_{CC}			± 3	LSB
R_{LADDER}	Ladder resistance	V_{REF} = V_{CC}	10		25	kΩ
t_{CONV}	Conversion time		19.6			µs
V_{REF}	Reference voltage		2.7		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

Note. This applies when the main clock division selection bit = “0” and $f(f_2)$ = 6 MHz.

TIMING REQUIREMENTS (V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, Ta = –40 to +85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted (Note 1))

Notes 1. This applies when the main clock division selection bit = "0" and f(f_2) = 6 MHz.

2. Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time (Note 1)	83		ns
$t_{w(H)}$	External clock input high-level pulse width (Note 2)	33		ns
$t_{w(L)}$	External clock input low-level pulse width (Note 2)	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

Notes 1. When the main clock division selection bit = "1", the minimum value of t_c = 166 ns.

2. When the main clock division selection bit = "1", values of $t_{w(H)}$ / t_c and $t_{w(L)}$ / t_c must be set to values from 0.45 through 0.55.

Single-chip mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(P0D–E)}$	Port P0 input setup time	200		ns
$t_{su(P1D–E)}$	Port P1 input setup time	200		ns
$t_{su(P2D–E)}$	Port P2 input setup time	200		ns
$t_{su(P3D–E)}$	Port P3 input setup time	200		ns
$t_{su(P4D–E)}$	Port P4 input setup time	200		ns
$t_{su(P5D–E)}$	Port P5 input setup time	200		ns
$t_{su(P6D–E)}$	Port P6 input setup time	200		ns
$t_{su(P7D–E)}$	Port P7 input setup time	200		ns
$t_{su(P8D–E)}$	Port P8 input setup time	200		ns
$t_{h(E–P0D)}$	Port P0 input hold time	0		ns
$t_{h(E–P1D)}$	Port P1 input hold time	0		ns
$t_{h(E–P2D)}$	Port P2 input hold time	0		ns
$t_{h(E–P3D)}$	Port P3 input hold time	0		ns
$t_{h(E–P4D)}$	Port P4 input hold time	0		ns
$t_{h(E–P5D)}$	Port P5 input hold time	0		ns
$t_{h(E–P6D)}$	Port P6 input hold time	0		ns
$t_{h(E–P7D)}$	Port P7 input hold time	0		ns
$t_{h(E–P8D)}$	Port P8 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(D–RDE)}$	Data input setup time	50		ns
$t_{su(RDY–\phi 1)}$	$\overline{RDY}$ input setup time	80		ns
$t_{su(HOLD–\phi 1)}$	$\overline{HOLD}$ input setup time	80		ns
$t_{h(RDE–D)}$	Data input hold time	0		ns
$t_{h(\phi 1–RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(\phi 1–HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	250		ns
$t_{w(TAH)}$	TAiIN input high-level pulse width	125		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width	125		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time (Note)	666		ns
$t_{w(TAH)}$	TAiIN input high-level pulse width (Note)	333		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width (Note)	333		ns

Note. Limits change depending on f(X_{IN}). Refer to “DATA FORMULAS”.

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time (Note)	666		ns
$t_{w(TAH)}$	TAiIN input high-level pulse width	166		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width	166		ns

Note. Limits change depending on f(X_{IN}). Refer to “DATA FORMULAS”.

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high-level pulse width	166		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width	166		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	3333		ns
$t_{w(UPH)}$	TAiOUT input high-level pulse width	1666		ns
$t_{w(UPL)}$	TAiOUT input low-level pulse width	1666		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	666		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	666		ns

Timer A input (Two-phase pulse input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAjIN input cycle time	2000		ns
$t_{su(TAjIN-TAjOUT)}$	TAjIN input setup time	500		ns
$t_{su(TAjOUT-TAjIN)}$	TAjOUT input setup time	500		ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (one edge count)	250		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (one edge count)	125		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (one edge count)	125		ns
$t_{c(TB)}$	TBi_{IN} input cycle time (both edges count)	500		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (both edges count)	250		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (both edges count)	250		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (Note)	666		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (Note)	333		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to “DATA FORMULAS”.

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (Note)	666		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (Note)	333		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to “DATA FORMULAS”.

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ input cycle time (minimum allowable trigger)	1333		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ input low-level pulse width	166		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK_i input cycle time	333		ns
$t_{w(CKH)}$	CLK_i input high-level pulse width	166		ns
$t_{w(CKL)}$	CLK_i input low-level pulse width	166		ns
$t_{d(C-Q)}$	TxD_i output delay time		100	ns
$t_{h(C-Q)}$	TxD_i hold time	0		ns
$t_{su(D-C)}$	RxD_i input setup time	65		ns
$t_{h(C-D)}$	RxD_i input hold time	75		ns

External interrupt $\overline{INT_i}$ input, key input interrupt $\overline{KI_i}$ input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT_i}$ input high-level pulse width	250		ns
$t_{w(INL)}$	$\overline{INT_i}$ input low-level pulse width	250		ns
$t_{w(KIL)}$	$\overline{KI_i}$ input low-level pulse width	250		ns

DATA FORMULAS

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer B input (In pulse period measurement mode or pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Note. $f(f_2)$ represents the clock f_2 frequency.
For the relation to the main clock and sub clock, refer to Table 10 in data sheet “M37735MHBXXXFP”.

SWITCHING CHARACTERISTICS

(V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, Ta = –40 to +85°C, f(X_{IN}) = 12 MHz, unless otherwise noted (Note))

Single-chip mode

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(E-P0Q)}$	Port P0 data output delay time	Fig. 2		300	ns
$t_{d(E-P1Q)}$	Port P1 data output delay time			300	ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			300	ns
$t_{d(E-P3Q)}$	Port P3 data output delay time			300	ns
$t_{d(E-P4Q)}$	Port P4 data output delay time			300	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time			300	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time			300	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time			300	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time			300	ns

Note. This applies when the main clock division selection bit = "0" and f(f_2) = 6 MHz.

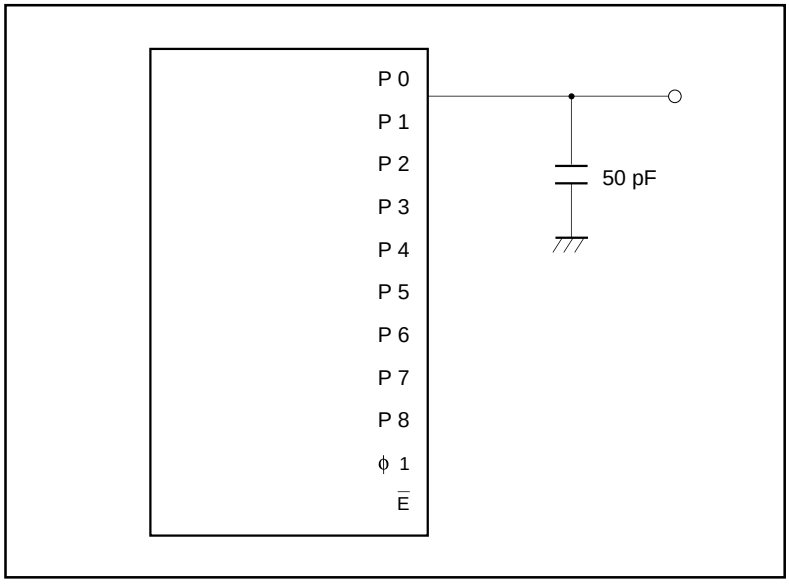


Fig. 2 Measuring circuit for ports P0 – P8 and ϕ_1

Memory expansion mode and microprocessor mode

(V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, Ta = –40 to +85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted (Note 1))

Symbol	Parameter	(Note 2) Wait mode	Test conditions	Limits Min.	Limits Max.	Unit
$t_{d(CS–WE)}$ $t_{d(CS–RDE)}$	Chip-select output delay time	No wait Wait 1	Fig. 2	20		ns
		Wait 0		182		ns
$t_{h(WE–CS)}$ $t_{h(RDE–CS)}$	Chip-select hold time			4		ns
$t_{d(An–WE)}$ $t_{d(An–RDE)}$	Address output delay time	No wait Wait 1		20		ns
		Wait 0		182		ns
$t_{d(A–WE)}$ $t_{d(A–RDE)}$	Address output delay time	No wait Wait 1		20		ns
		Wait 0		162		ns
$t_{h(WE–An)}$ $t_{h(RDE–An)}$	Address hold time			40		ns
$t_{w(ALE)}$	ALE pulse width	No wait Wait 1		40		ns
		Wait 0		123		ns
$t_{su(A–ALE)}$	Address output setup time	No wait Wait 1		10		ns
		Wait 0		93		ns
$t_{h(ALE–A)}$	Address hold time	No wait Wait 1		9		ns
		Wait 0		40		ns
$t_{d(ALE–WE)}$ $t_{d(ALE–RDE)}$	ALE output delay time	No wait Wait 1		4		ns
		Wait 0		40		ns
$t_{d(WE–DQ)}$	Data output delay time				90	ns
$t_{h(WE–DQ)}$	Data hold time			40		ns
$t_{w(WE)}$	$\overline{WEL}$/$\overline{WEH}$ pulse width	No wait		131		ns
		Wait 1 Wait 0		298		ns
$t_{pxz(RDE–DZ)}$	Floating start delay time				10	ns
$t_{pzx(RDE–DZ)}$	Floating release delay time			53		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width	No wait		128		ns
		Wait 1 Wait 0		295		ns
$t_{d(RSMP–WE)}$ $t_{d(RSMP–RDE)}$	$\overline{RSMP}$ output delay time			25		ns
$t_{h(\phi 1–RSMP)}$	$\overline{RSMP}$ hold time			0		ns
$t_{d(WE–\phi 1)}$ $t_{d(RDE–\phi 1)}$	$\phi 1$ output delay time			0	30	ns
$t_{d(\phi 1–HLDA)}$	$\overline{HLDA}$ output delay time				120	ns

Notes 1. This applies when the main clock division selection bit = “0” and f(f_2) = 6 MHz.

2. No wait : Wait bit = “1”.
Wait 1 : The external memory area is accessed with wait bit = “0” and wait selection bit = “1”.
Wait 0 : The external memory area is accessed with wait bit = “0” and wait selection bit = “0”.

Bus timing data formulas (V_{CC} = 2.7 – 5.5V, V_{SS} = 0 V, Ta = –40 to +85 °C, f(X_{IN}) = 12 MHz (Max.), unless otherwise noted (Note1))

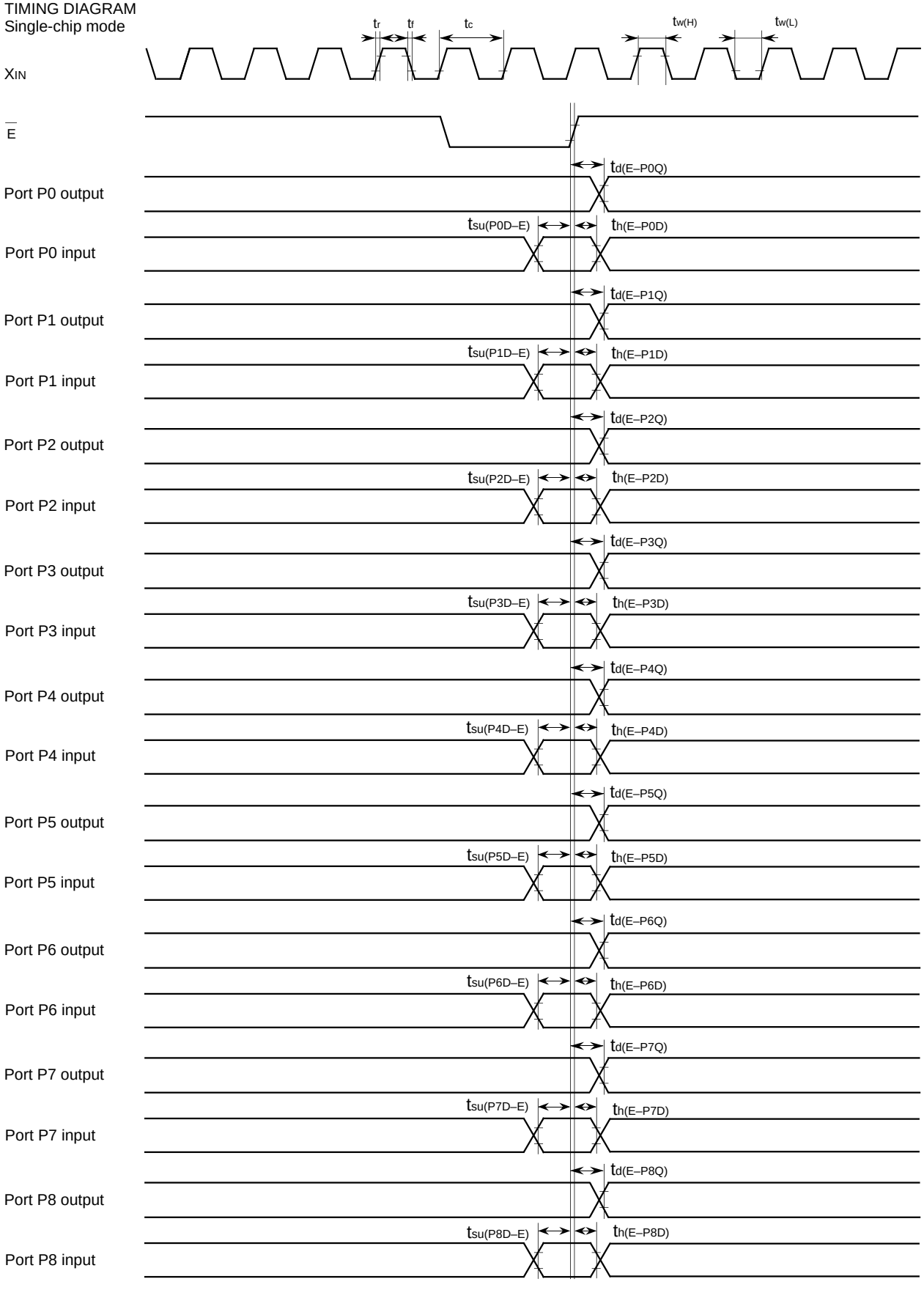
Symbol	Parameter	Wait mode	Limits Min.	Limits Max.	Unit
$t_{d(CS–WE)}$ $t_{d(CS–RDE)}$	Chip-select output delay time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 68$		ns
$t_{h(WE–CS)}$ $t_{h(RDE–CS)}$	Chip-select hold time		4		ns
$t_{d(An–WE)}$ $t_{d(An–RDE)}$	Address output delay time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 68$		ns
$t_{d(A–WE)}$ $t_{d(A–RDE)}$	Address output delay time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 88$		ns
$t_{h(WE–An)}$ $t_{h(RDE–An)}$	Address hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{w(ALE)}$	ALE pulse width	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{su(A–ALE)}$	Address output setup time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 73$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 73$		ns
$t_{h(ALE–A)}$	Address hold time	No wait Wait 1	9		ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{d(ALE–WE)}$ $t_{d(ALE–RDE)}$	ALE output delay time	No wait Wait 1	4		ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{d(WE–DQ)}$	Data output delay time			90	ns
$t_{h(WE–DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{w(WE)}$	$\overline{WEL}$/$\overline{WEH}$ pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
		Wait 1 Wait 0	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
$t_{pxz(RDE–DZ)}$	Floating start delay time			10	ns
$t_{pzx(RDE–DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 38$		ns
		Wait 1 Wait 0	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 38$		ns
$t_{d(RSMP–WE)}$ $t_{d(RSMP–RDE)}$	$\overline{RSMP}$ output delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 58$		ns
$t_{h(\phi 1–RSMP)}$	$\overline{RSMP}$ hold time		0		ns
$t_{d(WE–\phi 1)}$ $t_{d(RDE–\phi 1)}$	$\phi 1$ output delay time		0	30	ns

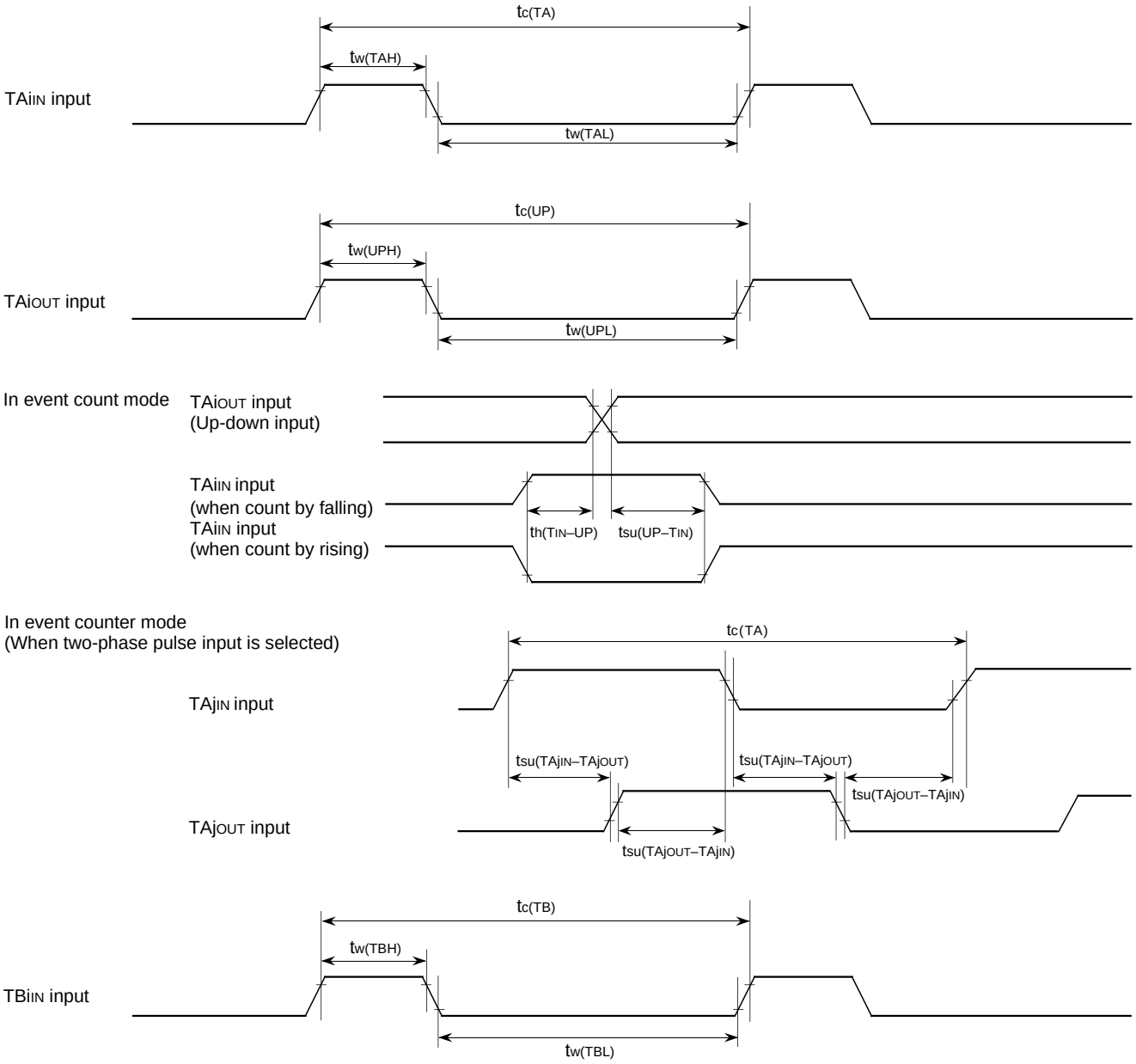
Notes 1. This applies when the main clock division selection bit = “0”.

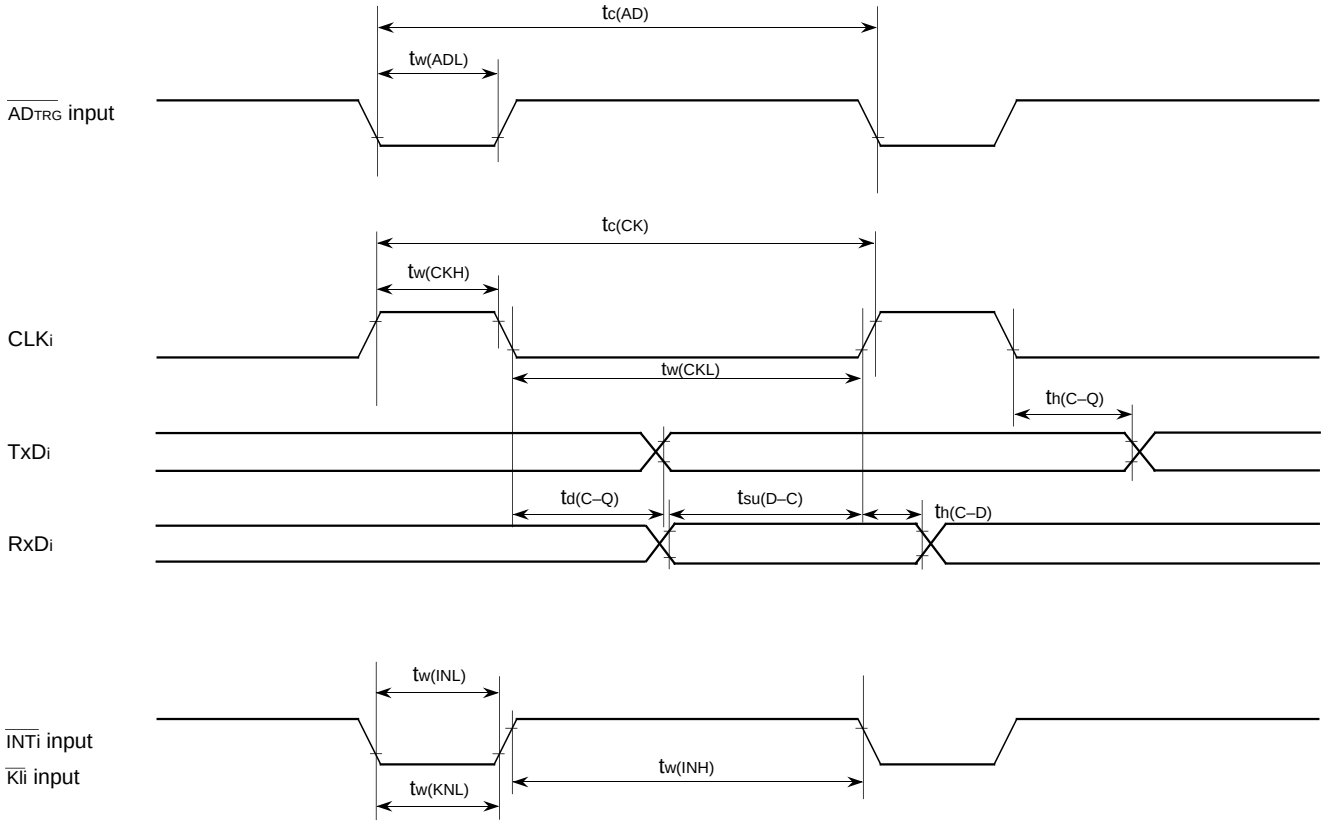
2. f(f_2) represents the clock f_2 frequency.
For the relation to the main clock and sub clock, refer to Table 10 in data sheet “M37735MHBXXXFP”.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

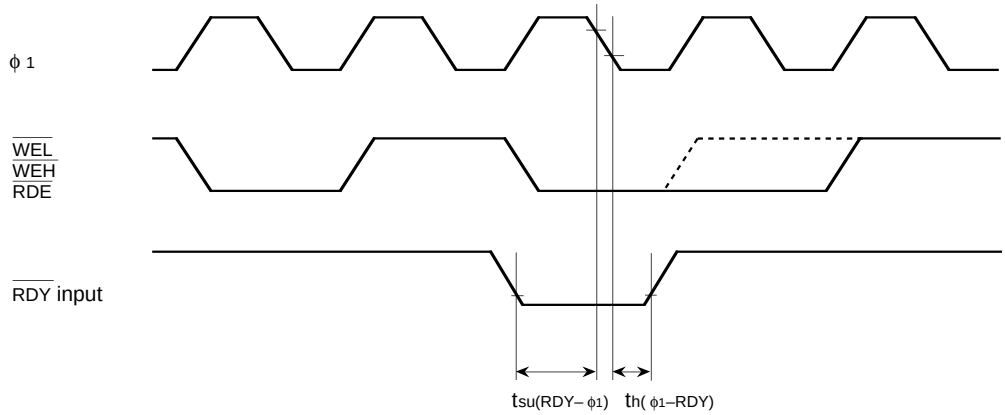
TIMING DIAGRAM
Single-chip mode



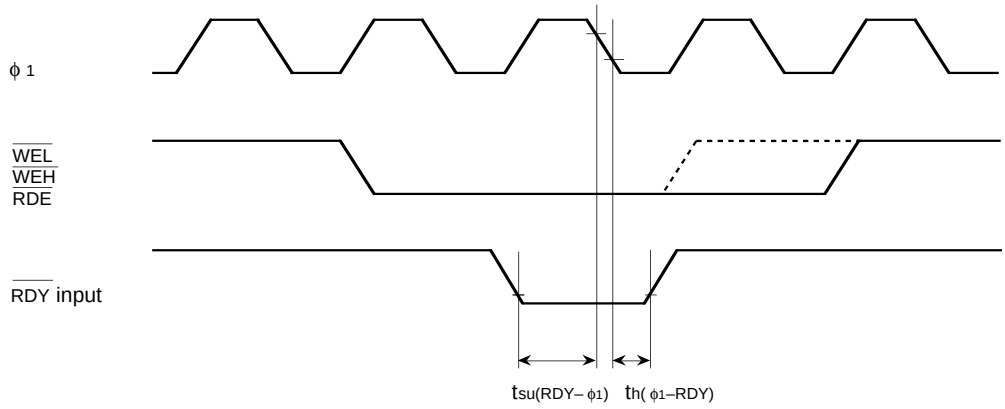

tc(TA)
tw(TAH)
TAiIN input
tw(TAL)
tc(UP)
tw(UPH)
TAiOUT input
tw(UPL)
In event count mode
TAiOUT input
(Up-down input)
TAiIN input
(when count by falling)
TAiIN input
(when count by rising)
th(TIN–UP)
tsu(UP–TIN)
In event counter mode
(When two-phase pulse input is selected)
tc(TA)
TAjIN input
tsu(TAjIN–TAjOUT)
tsu(TAjIN–TAjOUT)
tsu(TAjOUT–TAjIN)
TAjOUT input
tsu(TAjOUT–TAjIN)
tc(TB)
tw(TBH)
TBiIN input
tw(TBL)


tc(AD)
tw(ADL)
ADTRG input
tc(CK)
tw(CKH)
CLKi
tw(CKL)
th(C–Q)
TxDi
td(C–Q)
tsu(D–C)
th(C–D)
RxDi
tw(INL)
INTi input
tw(INH)
KIi input
tw(KNL)

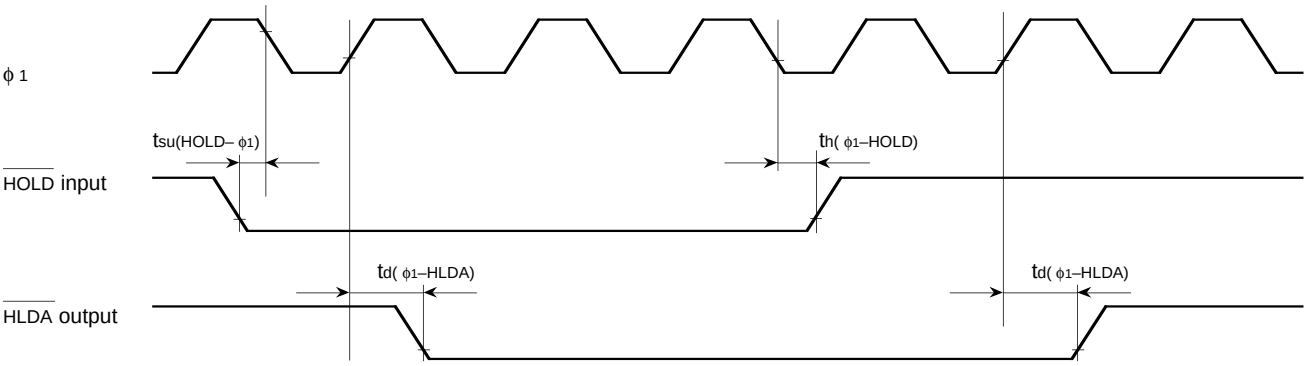
Memory expansion and microprocessor mode
(When wait bit = “1”)



(When wait bit = “0”)

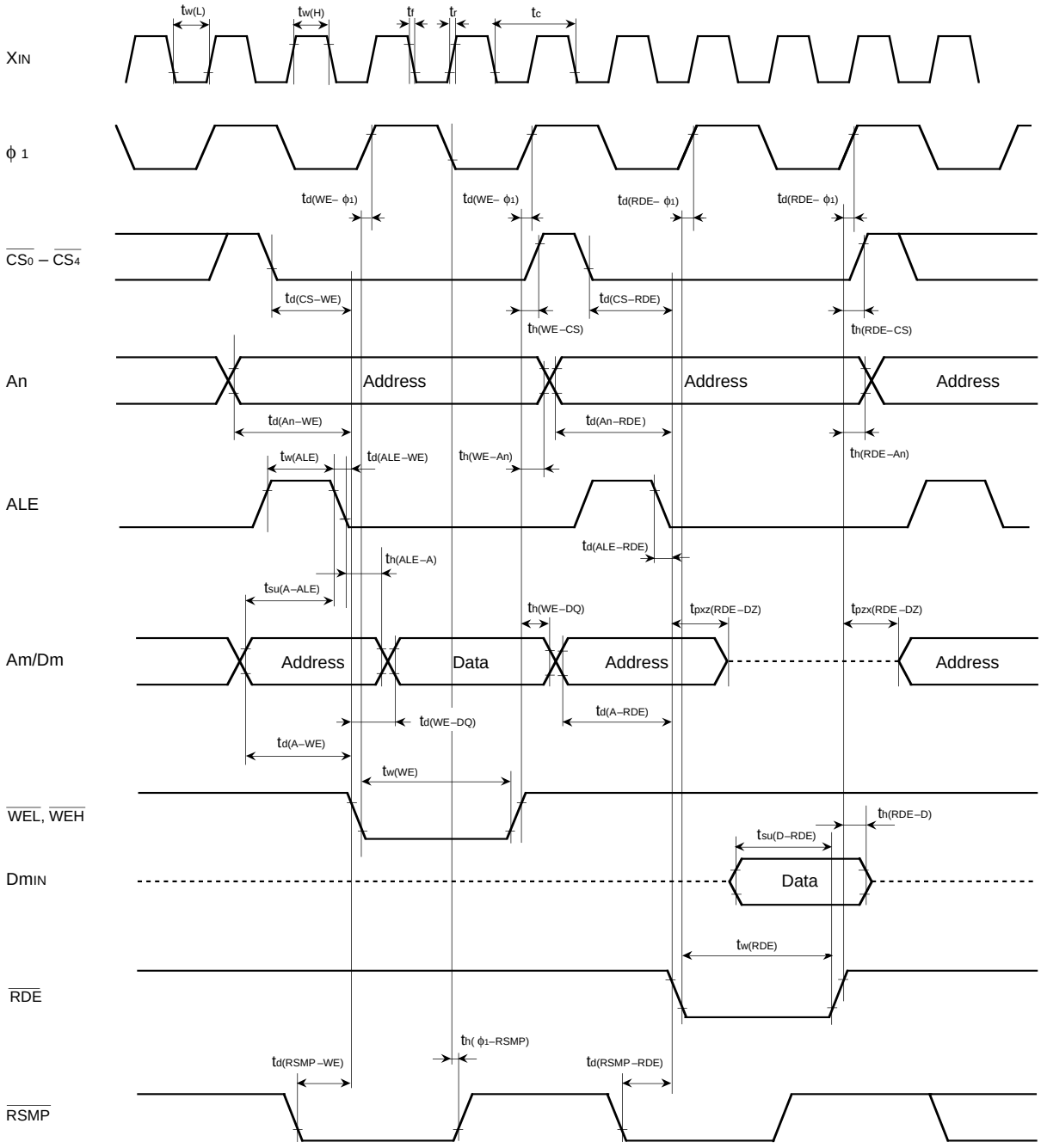


(When wait bit = “1” or “0” in common)



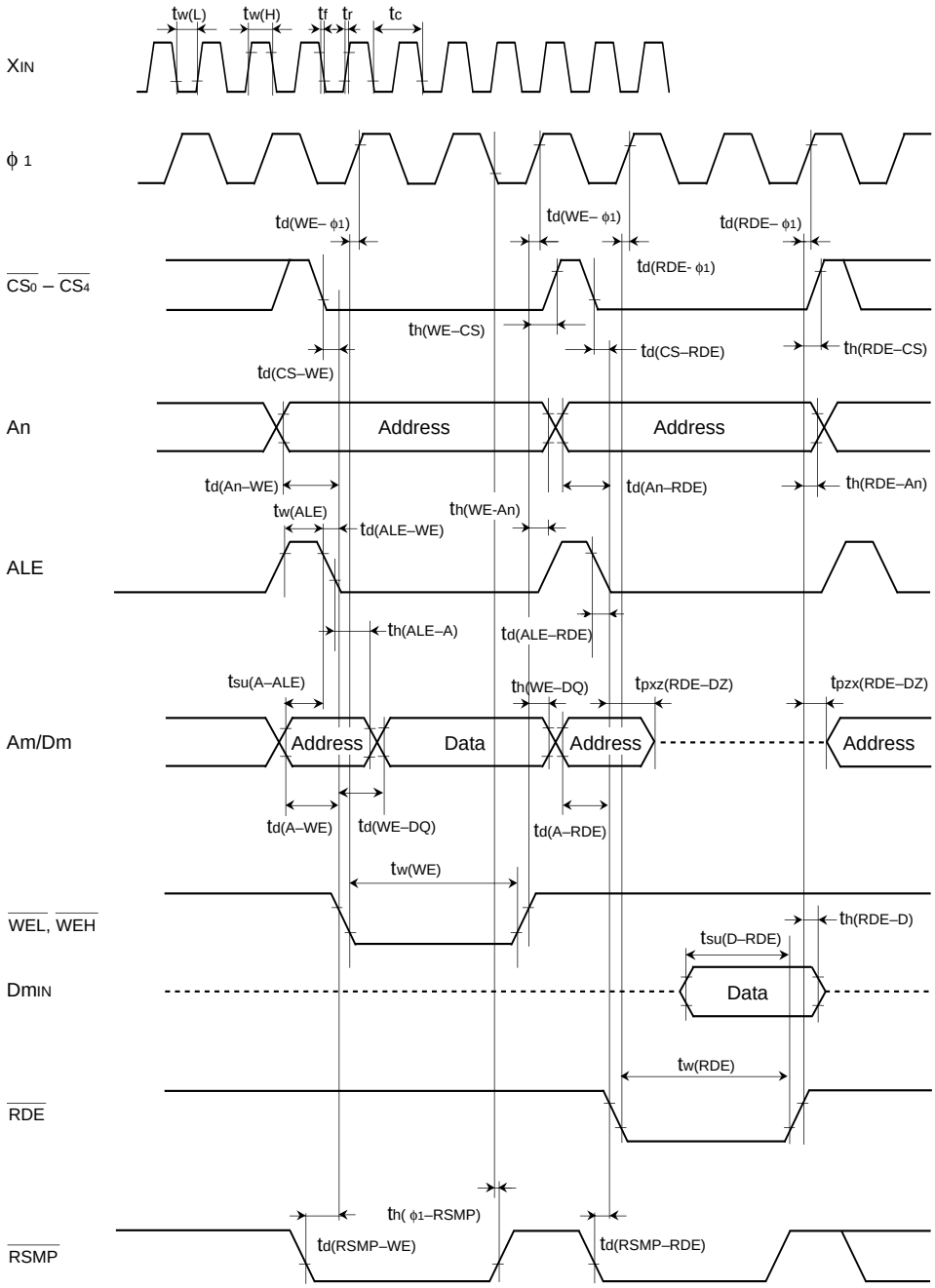
Test conditions
- V_{CC} = 2.7 – 5.5 V
- Input timing voltage : V_{IL} = 0.2V_{CC}, V_{IH} = 0.8V_{CC}
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

Memory expansion and microprocessor mode
(No wait : When wait bit = "1")



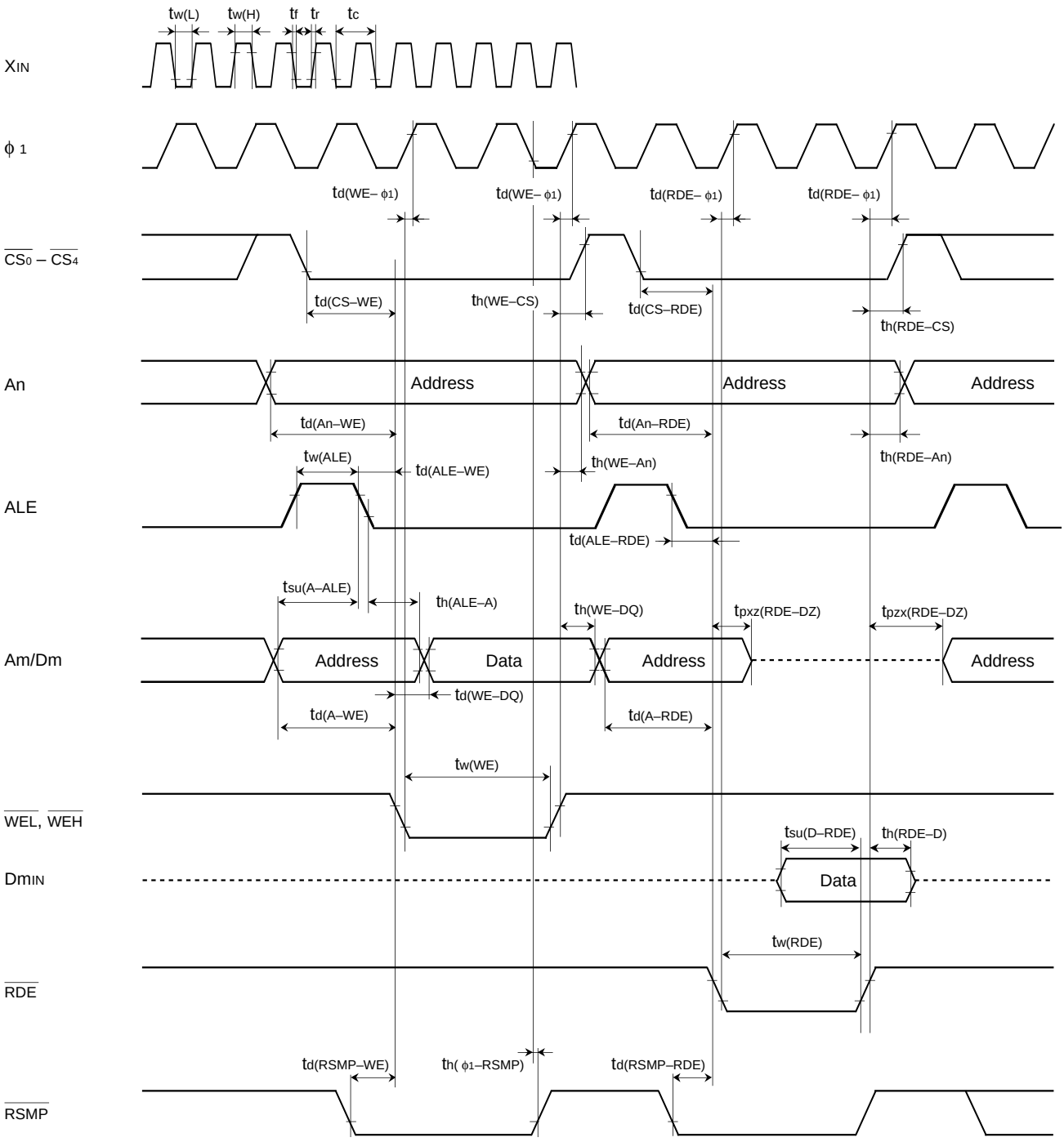
Test condition
- Vcc = 2.7 – 5.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input Dm_{IN} : V_{IL} = 0.16 Vcc, V_{IH} = 0.5 Vcc

Memory expansion and microprocessor mode
(Wait 1 : The external area is accessed when wait bit = “0” and wait selection bit = “1”.)



Test condition
- Vcc = 2.7 – 5.5 V
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V
- Data input DmIN : VIL = 0.16 Vcc, VIH = 0.5 Vcc

Memory expansion and microprocessor mode
(Wait 0 : The external memory are is accessed when wait bit = “0” and wait selection bit = “0”.)



Test conditions
- Vcc = 2.7 – 5.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input Dm_{IN} : V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}

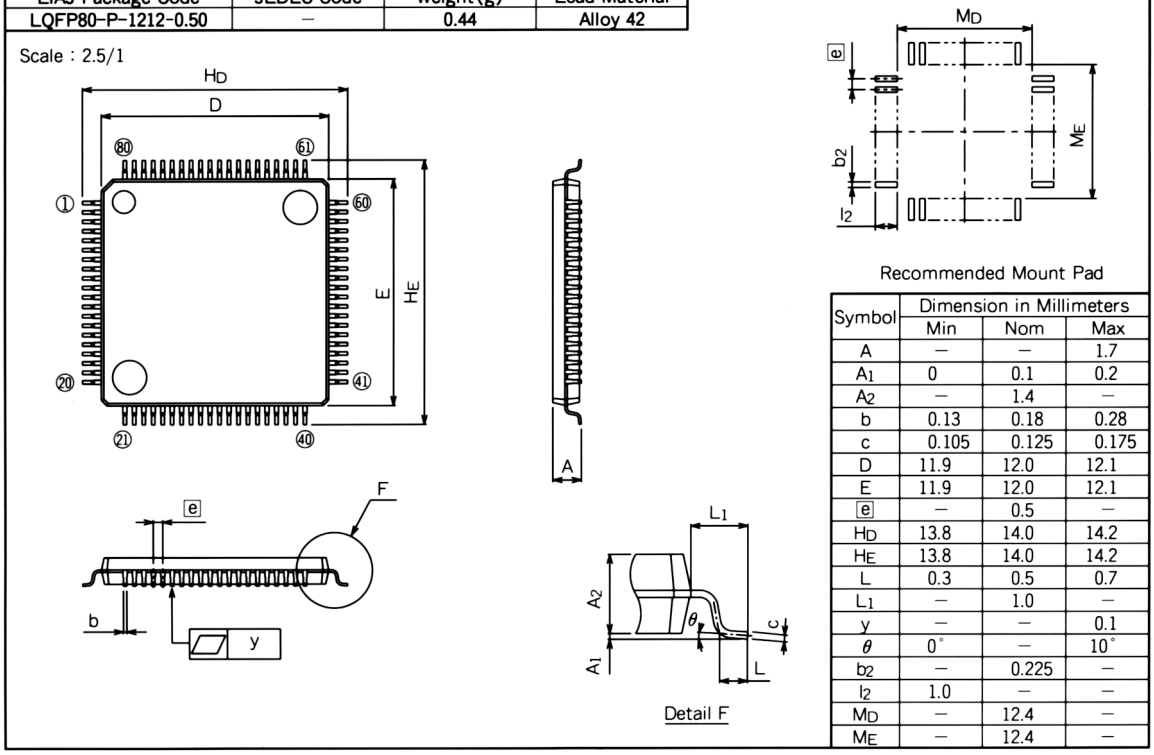
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

PACKAGE OUTLINE

80P6D−A — Plastic 80pin 12×12mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1212-0.50	—	0.44	Alloy 42

Scale : 2.5/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A_1	0	0.1	0.2
A_2	—	1.4	—
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	—	0.5	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
L	0.3	0.5	0.7
L_1	—	1.0	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.225	—
l_2	1.0	—	—
M_D	—	12.4	—
M_E	—	12.4	—

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ–SH00–43B<68A0>

Mask ROM number	

Receipt	Date:	
	Section head signature	Supervisor signature

7700 FAMILY MASK ROM ORDER CONFIRMATION FORM
SINGLE-CHIP 16-BIT MICROCOMPUTER
M37735MHLXXXHP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked ※

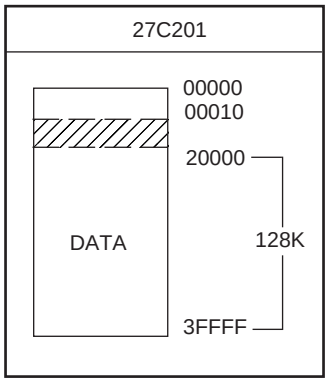
※	Customer	Company name	TEL ( )	Issuance signatures	Responsible officer	Supervisor
		Date issued	Date:			

※1. Confirmation

Specify the name of the product being ordered.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based on this data.
We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data.
Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM Type :



(1) Set "FF16" in the shaded area.
(2) Address 016 to 1016 are the area for storing the data on model designation and options.This area must be written with the data shown below.
Details for option data are given next in the section describing the STP instruction option.
Address and data are written in hexadecimal notation.

Address		Address		Address
4D	0	4C	8	Option data 10
33	1	FF	9	
37	2	FF	A	
37	3	FF	B	
33	4	FF	C	
35	5	FF	D	
4D	6	FF	E	
48	7	FF	F	

※2. STP instruction option

One of the following sets of data should be written to the option data address (1016) of the EPROM you have ordered.
Check @ in the appropriate box.

☐ STP instruction enable 0116 Address 1016
☐ STP instruction disable 0016 Address 1016

※3. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered fill out the appropriate 80P6D Mark Specification Form (for M37735MHLXXXHP) and attach to the Mask ROM Order Confirmation Form.

※4. Comments

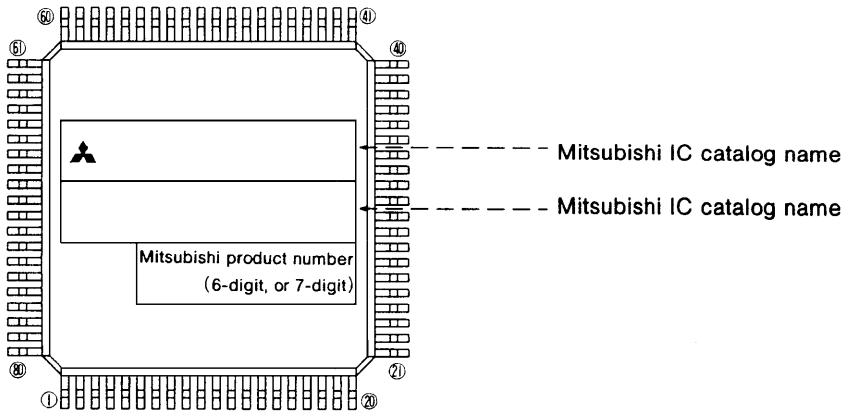
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

80P6S (80-PIN QFP) MARK SPECIFICATION FORM
80P6D (80-PIN Fine-pitch QFP)

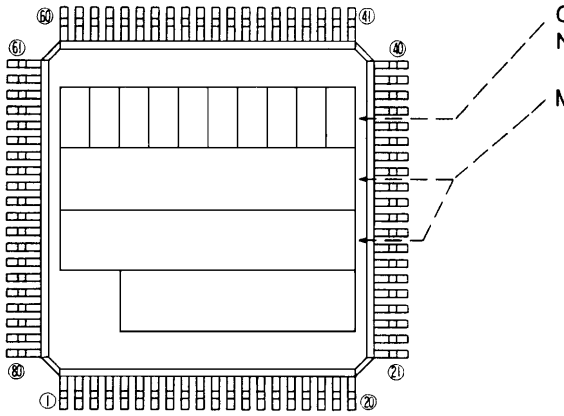
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi IC Catalog Name

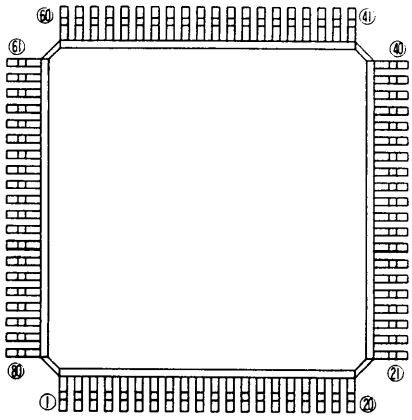


Notes1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 10 alphanumeric characters for capital letters, hyphens, commas, periods and so on.
4 : If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required ☐

5 : The allocation of Mitsubishi IC catalog name and Mitsubishi product number is different on the package owing to the number of Mitsubishi IC catalog name's characters, and the requiring Mitsubishi logo or not.

C. Special Mark Required



Notes1 : If special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated technically as close as possible. Mitsubishi product number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked for sorting the products.
2 : If special character fonts (e.g., customer's trade mark logo) must be used in Special Mark, check the box below.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special character fonts required ☐

PRELIMINARY
Notice: This is not a final specification.
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M37735MHLXXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

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- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

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Specifications subject to change without notice.

MITSUBISHI ELECTRIC

REVISION DESCRIPTION LIST	M37735MHLXXXHP Datasheet

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• MASK ROM ORDER CONFIRMATION FORM
• MARK SPECIFICATION FORM</td><td>980421</td></tr>
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Right column
Line 2</td><td>The M37735MHLXXXHP has 28 powerful addressing modes. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for the details of each addressing mode.

MACHINE INSTRUCTION LIST
The M37735MHLXXXHP has 103 machine instructions. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for details.</td><td>The M37735MHLXXXHP has 28 powerful addressing modes. Refer to the “7700 Family Software Manual” for the details.

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<tr><td></td><td>Line 10</td><td>(2) 80P6D mark specification form</td><td>(2) 80P6D, 80P6Q mark specification form</td><td></td></tr>
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Memory expansion mode and microprocessor mode</td><td colspan="2">Previous Version
<table><tr><th rowspan="2">Symbol</th><th rowspan="2">Parameter</th><th colspan="2">Limits</th><th rowspan="2">Unit</th></tr><tr><th>Min.</th><th>Max.</th></tr><tr><td>tsu(D–RDE)</td><td>Data input setup time</td><td>80</td><td></td><td>ns</td></tr></table>Revised Version
<table><tr><th rowspan="2">Symbol</th><th rowspan="2">Parameter</th><th colspan="2">Limits</th><th rowspan="2">Unit</th></tr><tr><th>Min.</th><th>Max.</th></tr><tr><td>tsu(D–RDE)</td><td>Data input setup time</td><td>50</td><td></td><td>ns</td></tr></table></td><td></td></tr>
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