FAIRCHILD

SEMICONDUCTOR®

Si6953DQ

Dual 20V P-Channel PowerTrench® MOSFET

General Description

This P-Channel MOSFET is a rugged gate version of Fairchild's Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V – 20V).

Applications

- Load switch
- Battery protection
- DC/DC conversion
- Power management

Features

- −1.9 A, −20 V, $R_{DS(ON)}$ = 170 mΩ @ V_{GS} = −10 V.
  $R_{DS(ON)}$ = 320 mΩ @ V_{GS} = −4.5V.

- Extended V_{GSS} range (±20V) for battery applications

- Low gate charge

- High performance trench technology for extremely low $R_{DS(ON)}$

- Low profile TSSOP-8 package

TSSOP-8

Pin 1

G2
S2
S2
D2
G1
S1
S1
D1
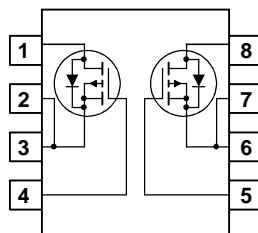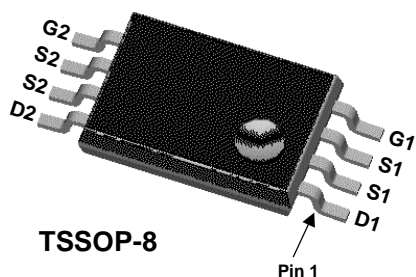
Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		−20	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1)	−1.9	A
	– Pulsed		−15	
P_D	Power Dissipation for Single Operation	(Note 1a)	1.0	W
		(Note 1b)	0.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Thermal Characteristic

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	100	°C/W
		(Note 1b)	125	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
6953	Si6953DQ	13''	12mm	2500 units

Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = -250$ µA	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250$ µA, Referenced to 25°C		-22		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -20$ V, $V_{GS} = 0$ V			-1	µA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = -20$ V, $V_{DS} = 0$ V			-100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = 20$ V, $V_{DS} = 0$ V			100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250$ µA	-1	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250$ µA, Referenced to 25°C		4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10$ V, $I_D = -1.9$ A $V_{GS} = -4.5$ V, $I_D = -1.3$ A $V_{GS} = -10$ V, $I_D = -1.9$ A, $T_J=125°C$		96 151 134	170 320 254	mΩ
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -10$ V, $V_{DS} = -5$ V	-10			A
g_{FS}	Forward Transconductance	$V_{DS} = -15$ V, $I_D = -1.9$ A		4		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -10$ V, $V_{GS} = 0$ V, f = 1.0 MHz		218		pF
C_{oss}	Output Capacitance			65		pF
C_{rss}	Reverse Transfer Capacitance			31		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -10$V, $I_D = -1$ A, $V_{GS} = -10$ V, $R_{GEN} = 6$ Ω		6	20	ns
t_r	Turn–On Rise Time			15	25	ns
$t_{d(off)}$	Turn–Off Delay Time			12	30	ns
t_f	Turn–Off Fall Time			1.5	15	ns
t_{rr}	Reverse Recovery Time	$V_{GS} = 0$ V, $I_F = 1.5$ A, $dI_F/dt = 100A/µs$		11	70	ns
Q_g	Total Gate Charge	$V_{DS} = -10$V, $I_D = -1.9$ A, $V_{GS} = -10$ V		4	10	nC
Q_{gs}	Gate–Source Charge			0.9		nC
Q_{gd}	Gate–Drain Charge			0.7		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				-1.25	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = -1.25$ A (Note 2)		-0.8	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$ is 100°C/W (steady state) when mounted on a 1 inch² copper pad on FR-4.
b) $R_{\theta JA}$ is 125°C/W (steady state) when mounted on a minimum copper pad on FR-4.

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

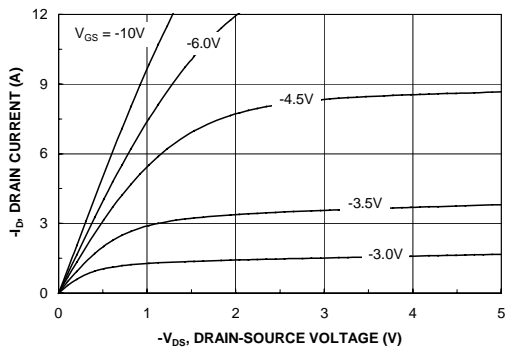## Typical Characteristics

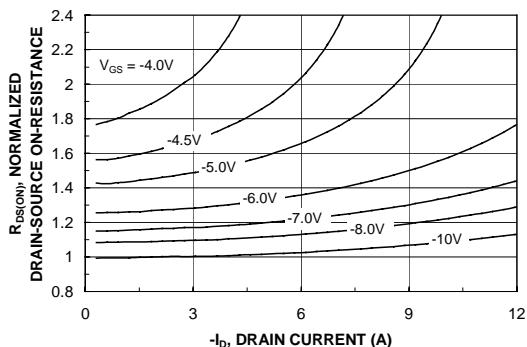Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with
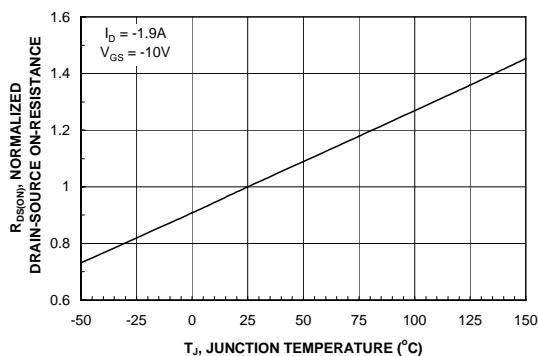Drain Current and Gate Voltage.

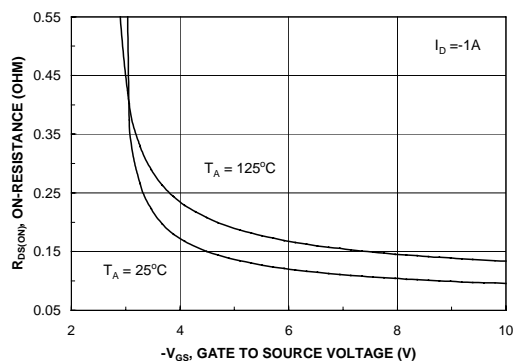Figure 3. On-Resistance Variation with
Temperature.

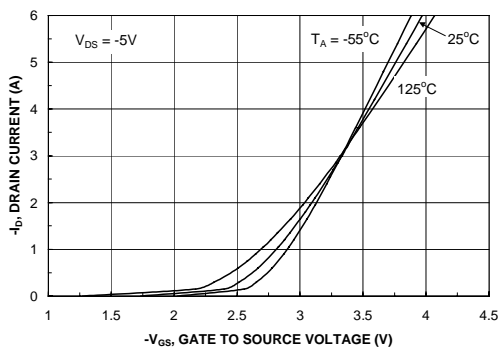Figure 4. On-Resistance Variation with
Gate-to-Source Voltage.
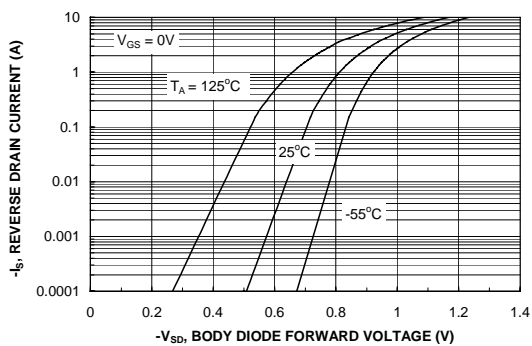

Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation
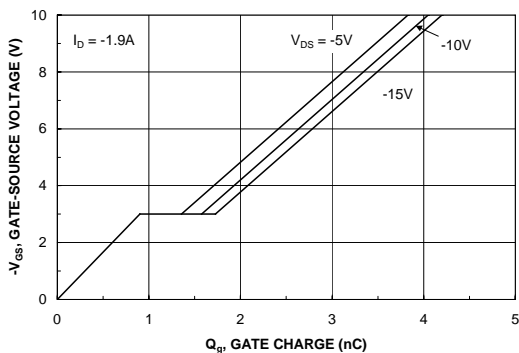with Source Current and Temperature.

Typical Characteristics
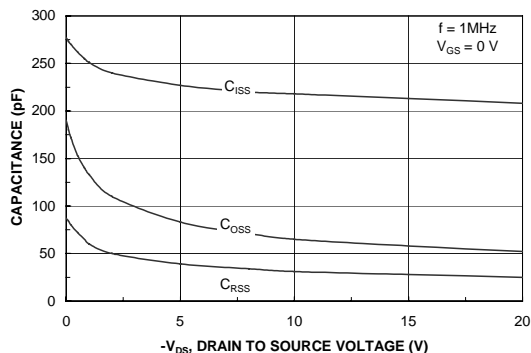
Figure 7. Gate Charge Characteristics.
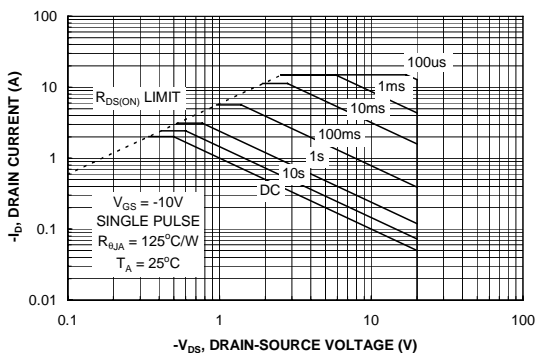
Figure 8. Capacitance Characteristics.

Figure 9. Maximum Safe Operating Area.
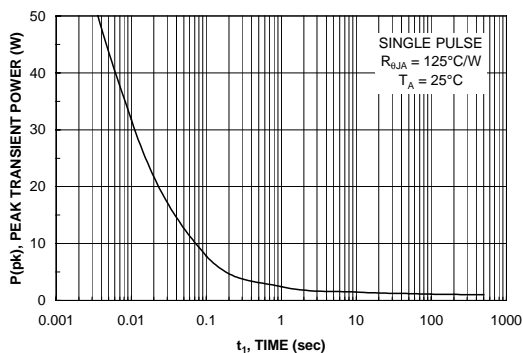
Figure 10. Single Pulse Maximum Power Dissipation.

In Figure 11:

$$R_{\theta JA}(t) = r(t) * R_{\theta JA}$$
$$R_{\theta JA} = 125 \text{ °C/W}$$
$$T_J - T_A = P * R_{\theta JA}(t)$$
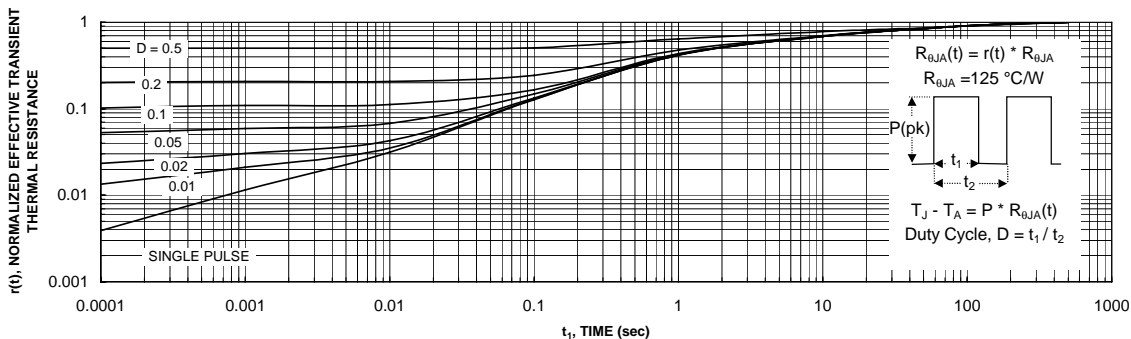$$\text{Duty Cycle, } D = t_1 / t_2$$

Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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