

CCD Vertical Clock Driver

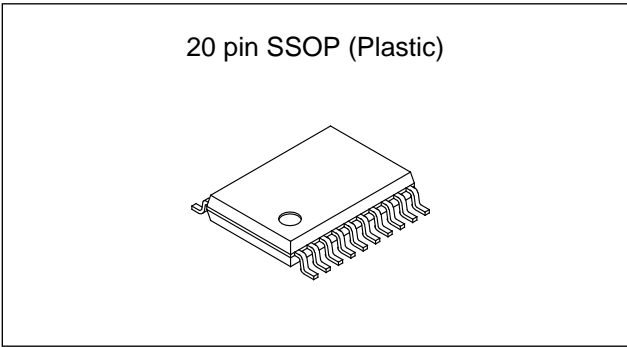
Description

The CXD1267AN is a vertical clock driver for CCD image sensors. This IC is the successor of the CXD1250N with attractive features.

Power consumption is reduced approximately 30% for the CXD1267AN version.

Features

- 1) Substrate voltage (V_{sub}) generator is built-in.
 - Variable V_{sub} in the range of 4.0V to 18.5V.
 - Reduction of peripheral parts saves space.
- 2) Only two power supplies (+15V and -8.5V) are needed.
- 3) 3.3V clock interface is acceptable.
- 4) 20-pin SSOP package is used.
- 5) Low power consumption
 - 90mW (CXD1267N)
 - 62mW (CXD1267AN)
 - approximately 30% reduction



Applications

CCD cameras

Structure

CMOS

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

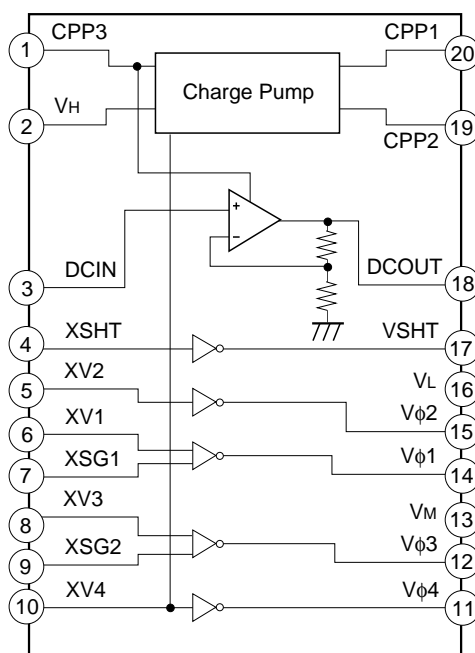
• Supply voltage	V_L	0 to -10	V
• Supply voltage	V_H	$V_L - 0.3$ to $2V_L + 35$	V
• Supply voltage	V_M	$V_L - 0.3$ to 3.0	V
• Input voltage	V_i	$V_L - 0.3$ to $V_H + 0.3$	V
• Output voltage (V_2, V_4)	MV_ϕ	$V_L - 0.3$ to $V_M + 0.3$	V
• Output voltage (V_1, V_3)	HV_ϕ	$V_L - 0.3$ to $V_H + 0.3$	V
• Output voltage (V_{SHT})	HHV_ϕ	$V_L - 0.3$ to $V_H + 0.3$	V
• Operational amplifier output current	I_{DCOUT}	± 5	mA
• Operating temperature	T_{opr}	-25 to +85	$^\circ\text{C}$
• Storage temperature	T_{stg}	-40 to +125	$^\circ\text{C}$

Recommended Operating Conditions

• Supply voltage	V_H	14.5 to 15.5	V
• Supply voltage	V_M	0	V
• Supply voltage	V_L	-6.0 to -9.0	V
• Input voltage (except for pin 3)	V_i	0 to 6.0	V
• Operational amplifier input voltage	V_{IOP}	1.0 to 4.5	V
• Operating temperature	T_{opr}	-20 to +75	$^\circ\text{C}$

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Block Diagram and Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	I/O	Description
1	CPP3	O	Charge pump
2	VH	—	Power supply (15V)
3	DCIN	I	Operational amplifier input
4	XSHT	I	Output control (VSHT)
5	XV2	I	Output control (Vφ2)
6	XV1	I	Output control (Vφ1)
7	XSG1	I	Output control (Vφ1)
8	XV3	I	Output control (Vφ3)
9	XSG2	I	Output control (Vφ3)
10	XV4	I	Output control (Vφ4)
11	Vφ4	O	High-voltage output (2 levels: VM, VL)
12	Vφ3	O	High-voltage output (3 levels: VH, VM, VL)
13	VM	—	GND
14	Vφ1	O	High-voltage output (3 levels: VH, VM, VL)
15	Vφ2	O	High-voltage output (2 levels: VM, VL)
16	VL	—	Power supply (-8.5V)
17	VSHT	O	High-voltage output (2 levels: VH, VL)
18	DCOUT	O	Operational amplifier output
19	CPP2	—	Charge pump
20	CPP1	—	Charge pump

Truth Table

Input				Output		
XV1, 3	XSG1, 2	XV2, 4	XSHT	V ϕ 1, 3	V ϕ 2, 4	VSHT
L	L	X	X	V _H	X	X
H	L	X	X	Z	X	X
L	H	X	X	V _M	X	X
H	H	X	X	V _L	X	X
X	X	L	X	X	V _M	X
X	X	H	X	X	V _L	X
X	X	X	L	X	X	V _H
X	X	X	H	X	X	V _L

X: Don't care
Z: High impedance

Electrical Characteristics

DC Characteristics

(Unless otherwise specified, Ta = 25°C, V_H = 15V, V_M = GND, V_L = -8.5V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V _{IH}		2.3	—	—	V
Low level input voltage	V _{IL}		—	—	1.3	V
High level output voltage	V _{OH}	I _O = -20 μ A	14.9	15.0	—	V
Middle level output voltage	V _{OM1}	I _O = 20 μ A	—	0.0	0.1	V
Middle level output voltage	V _{OM2}	I _O = -20 μ A	-0.1	0.0	—	V
Low level output voltage	V _{OL}	I _O = 20 μ A	—	-8.5	-8.4	V
Charge pump output voltage	V _{CPP3}	-1 \leq I _{CPP3} \leq 0mA I _{DCOUT} = 0mA, Ta = -20 to 75°C V _{IOP} = 4.5V	20	—	—	V
Input current	I _I	V _I = V _L to 5V	-1.0	0.0	1.0	μ A
Operating supply current	I _H	*1	—	1.4	2.0	mA
Operating supply current	I _L	*1	-6.0	-5.0	—	mA
Output current	I _{OL}	V ϕ 1 to 4 = -8.0V	25	—	—	mA
Output current	I _{OM1}	V ϕ 1 to 4 = -0.5V	—	—	-10	mA
Output current	I _{OM2}	V ϕ 1, 3 = 0.5V	9	—	—	mA
Output current	I _{OH}	V ϕ 1, 3 = 14.5V	—	—	-12	mA
Output current	I _{OSL}	VSHT = -8.0V	12	—	—	mA
Output current	I _{OSH}	VSHT = 14.5V	—	—	-7	mA
Operational amplifier gain	G	I _{DCOUT} = -200/+100 μ A	—	\times 4.40	—	
Gain error	Δ G	Ta = -20 to 75°C*2 I _{DCOUT} = -200/+100 μ A V _{IOP} = 1.0 to 4.5V	-3	—	+3	%

*1 See Measurement Circuit. Shutter speed: 1/10000.

*2 See Operational Amplifier Gain Characteristic.

Note) Current directions: + indicates the direction flowing to IC; - indicates the direction flowing from IC

Switching Characteristics

 $(V_H = 15V, V_M = GND, V_L = -8.5V)$

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time	T _{PLM}	*1	30	50	75	ns
Propagation delay time	T _{PMH}	*1	30	50	75	ns
Propagation delay time	T _{PLH}	*1	30	50	75	ns
Propagation delay time	T _{PML}	*1	50	80	120	ns
Propagation delay time	T _{PHM}	*1	50	80	120	ns
Propagation delay time	T _{PHL}	*1	50	80	120	ns
Rise time	T _{TLM}	$V_L \rightarrow V_M$ *1	360	600	900	ns
Rise time	T _{TMH}	$V_M \rightarrow V_H$ *1	330	550	770	ns
Rise time	T _{TLH}	$V_L \rightarrow V_H$ *1	30	50	75	ns
Fall time	T _{TML}	$V_M \rightarrow V_L$ *1	180	300	500	ns
Fall time	T _{THM}	$V_H \rightarrow V_M$ *1	330	550	770	ns
Fall time	T _{THL}	$V_H \rightarrow V_L$ *1	24	40	60	ns
Charge pump boosting time	T _C	*2	—	—	10	ms
Output noise voltage	V _{CLH}	*3	—	—	0.5	V
Output noise voltage	V _{CLL}	*3	—	—	0.5	V
Output noise voltage	V _{CMH}	*3	—	—	0.5	V
Output noise voltage	V _{CML}	*3	—	—	0.5	V

*1 See Response of Voltage Pulse.

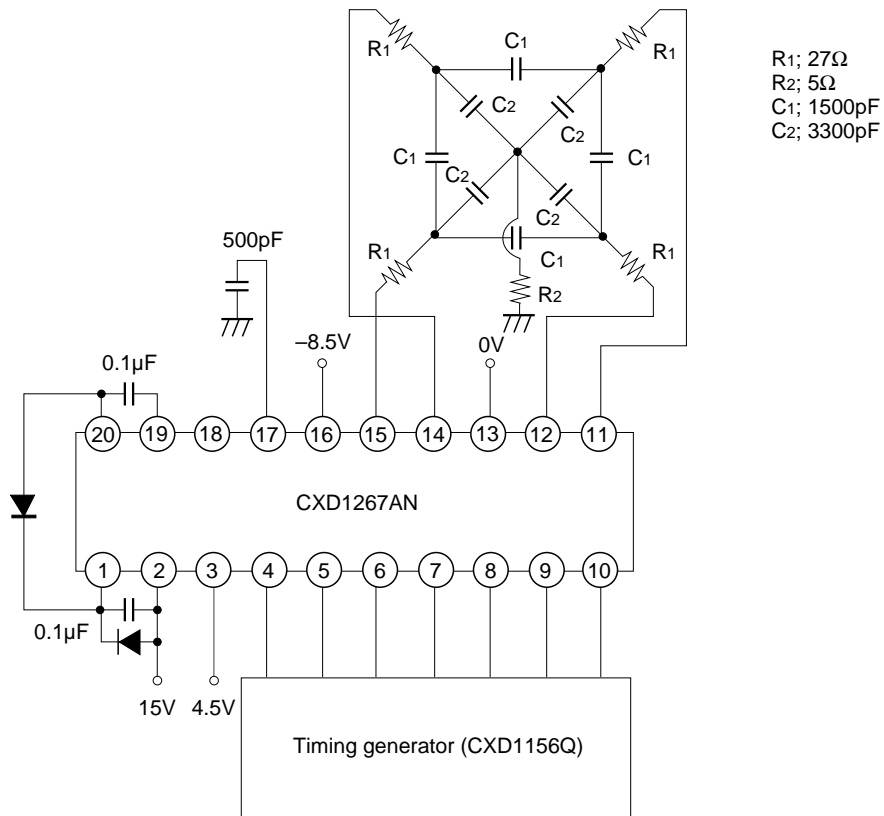
*2 CP1 = 0.1 μ F, CP2 = 0.1 μ F, V_{CPP3} = 20V; boosting time after all power supplies rose.

*3 See Noise on a Waveform.

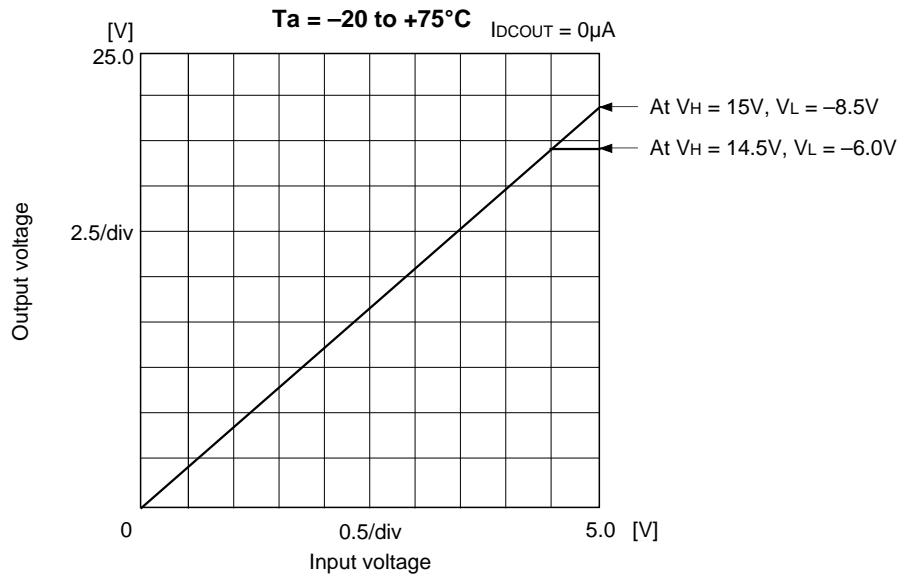
Note) Each item is evaluated by Measurement Circuit.**Notes on Operation** (See Application Circuit.)

1. Be sure to protect against static electricity because this IC is MOS structure.
2. A bypass capacitor is connected between each power supply (V_H , V_L) and GND.
3. To prevent latch-up, use a capacitor of 0.1 μ F (CP1, CP2) for charge pump.
Insert a silicon diode (D2) between CPP3 and CPP1.
4. In order to protect CCD image sensor, pre-clamp is requested prior to clamp by DCOU_T.

Measurement Circuit



Operational Amplifier Gain Characteristics

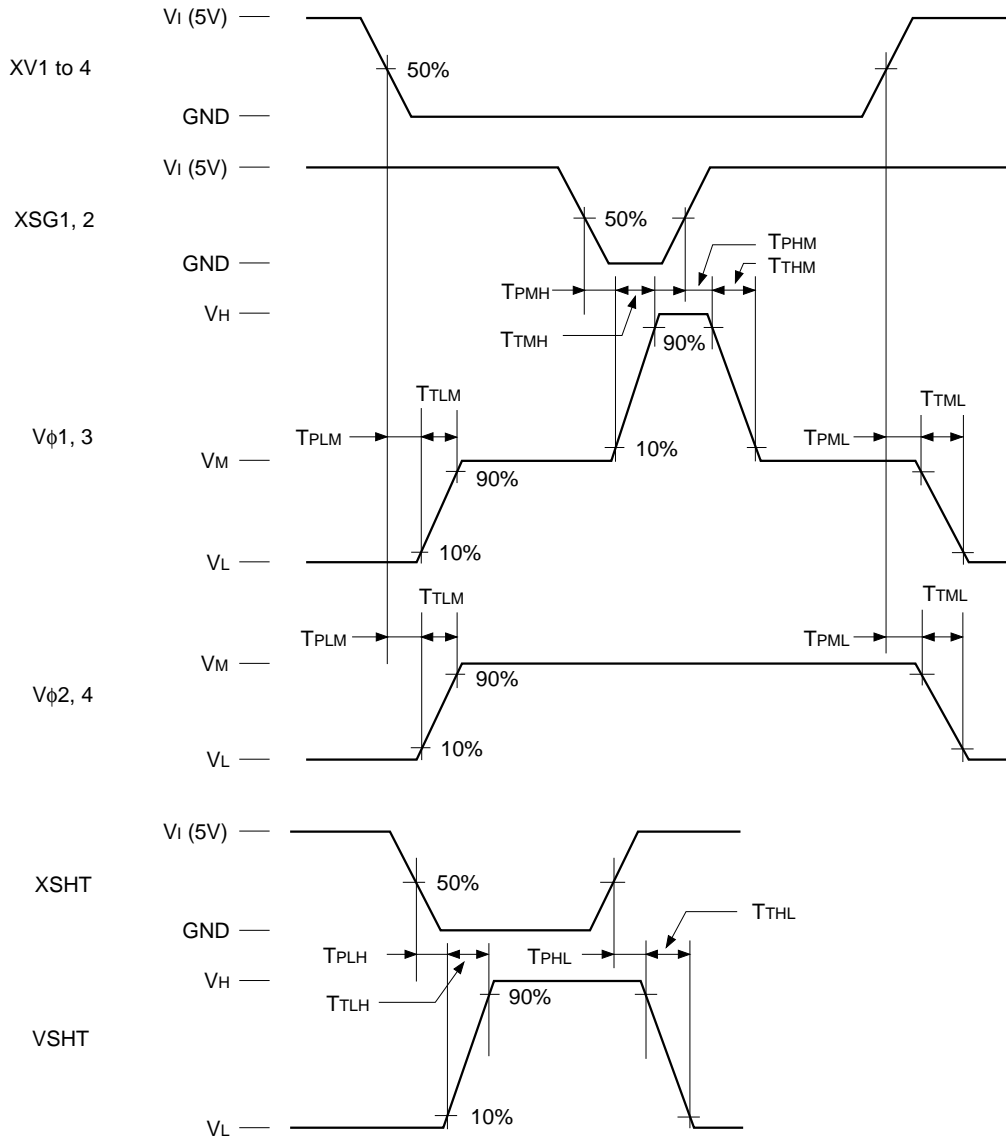


Note) Operating amplifier maximum output voltage is restricted as shown in the formula below depending on supply voltage setting of V_H and V_L .

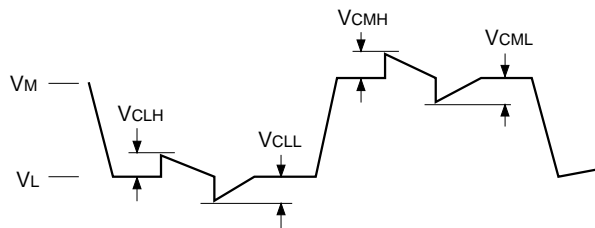
$$\text{Maximum output voltage } V_{\text{DCOUT}}(\text{max}) \approx V_H + |V_L| - 0.8\text{V}$$

For instance, when $V_H = 14.5\text{V}$ and $V_L = -6.0\text{V}$, output voltage is saturated at approximately 19.7V as shown above figure.

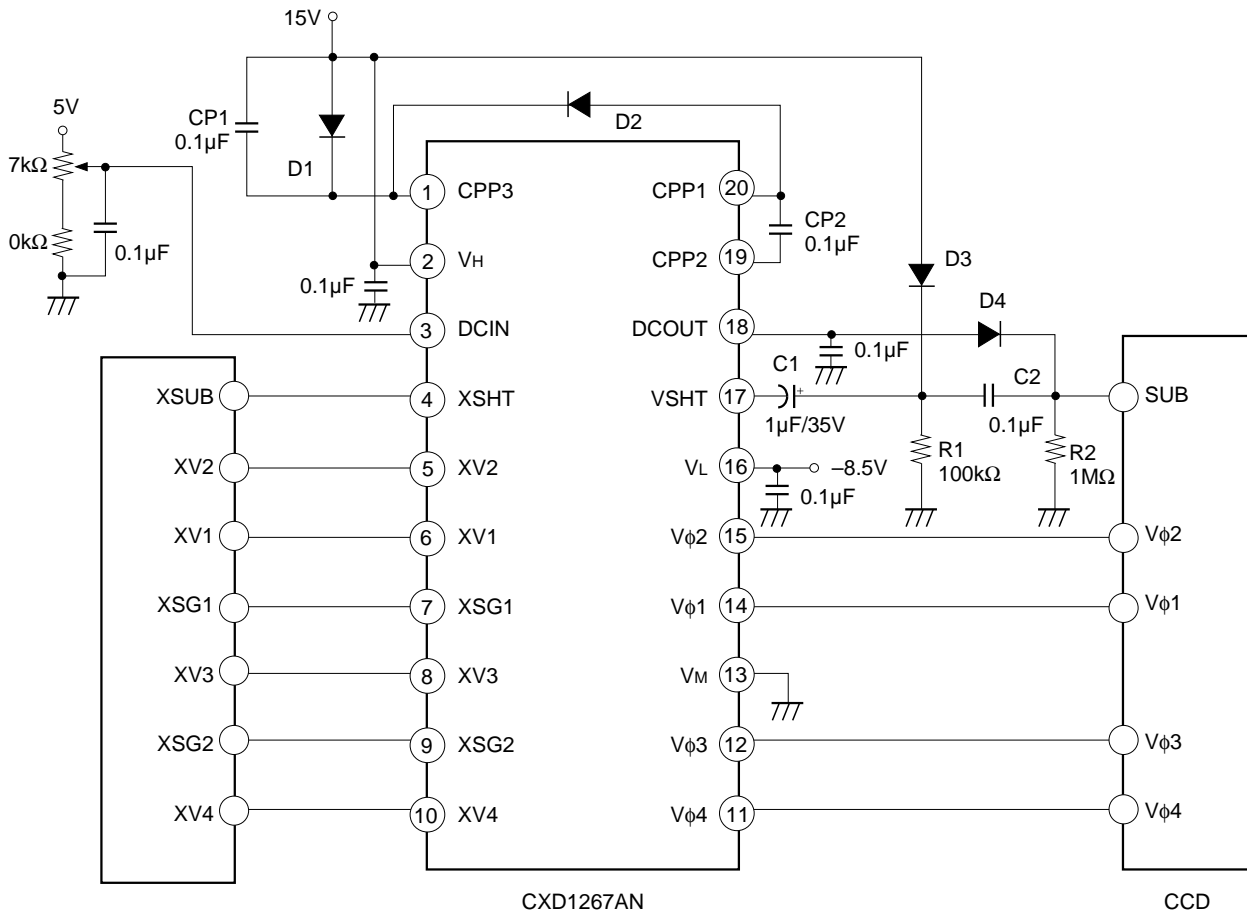
Response of Voltage Pulse



Noise on a Waveform



Application Circuit

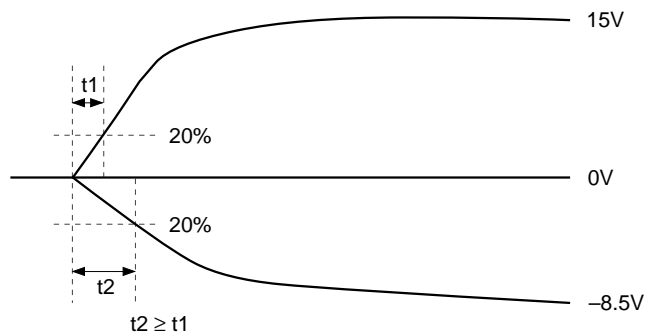


* A peripheral circuit can be simplified by CCD image sensor.

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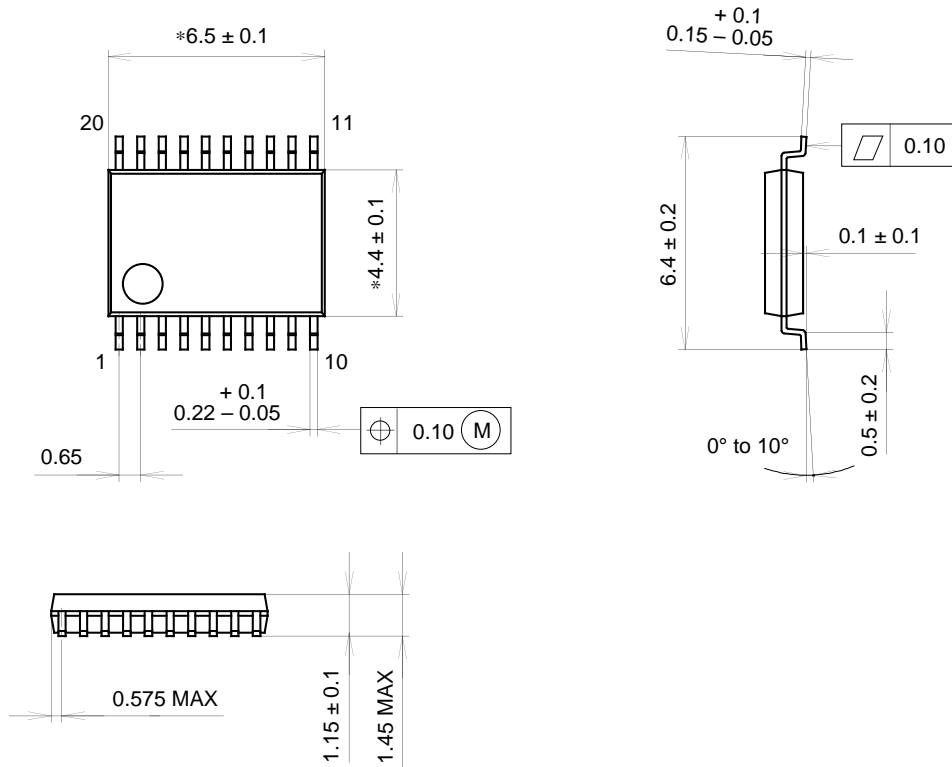
Note with power-on sequence

To protect CCD image sensor, rise two power supplies as follows.



Package Outline Unit: mm

20PIN SSOP (Plastic)



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	SSOP-20P-L071
EIAJ CODE	SSOP020-P-0044-AN
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	Cu ALLOY
PACKAGE WEIGHT	0.1g