SONY

CXP853P40A

CMOS 8-bit Single-chip Microcomputer

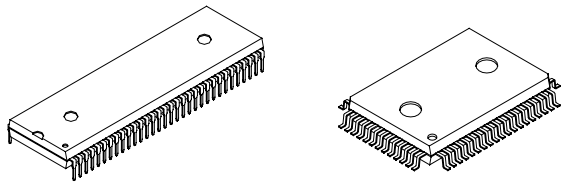
Description

The CXP853P40A are a highly integrated microcomputers composed of a 8-bit CPU, PROM, RAM, and I/O ports. These chips feature many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time-base timer, vector interrupt, on-screen display function, I²C bus interface, PWM generator, remote control receiver, HSYNC counter, power supply frequency counter, and watchdog timer.

Also, this IC provides power-on reset and sleep functions. The designers have ensured low power consumption for these powerful microcomputers.

The CXP853P40A is the one-chip PROM version of the CXP85340A with on-chip mask ROM, providing the function of being able to write directly into the program. Furthermore, because of the OSD character ROM can also be written directly into, it is suitable for evaluation use during system development and for small quantity production.

64 pin SDIP (Plastic) 64 pin QFP (Plastic)



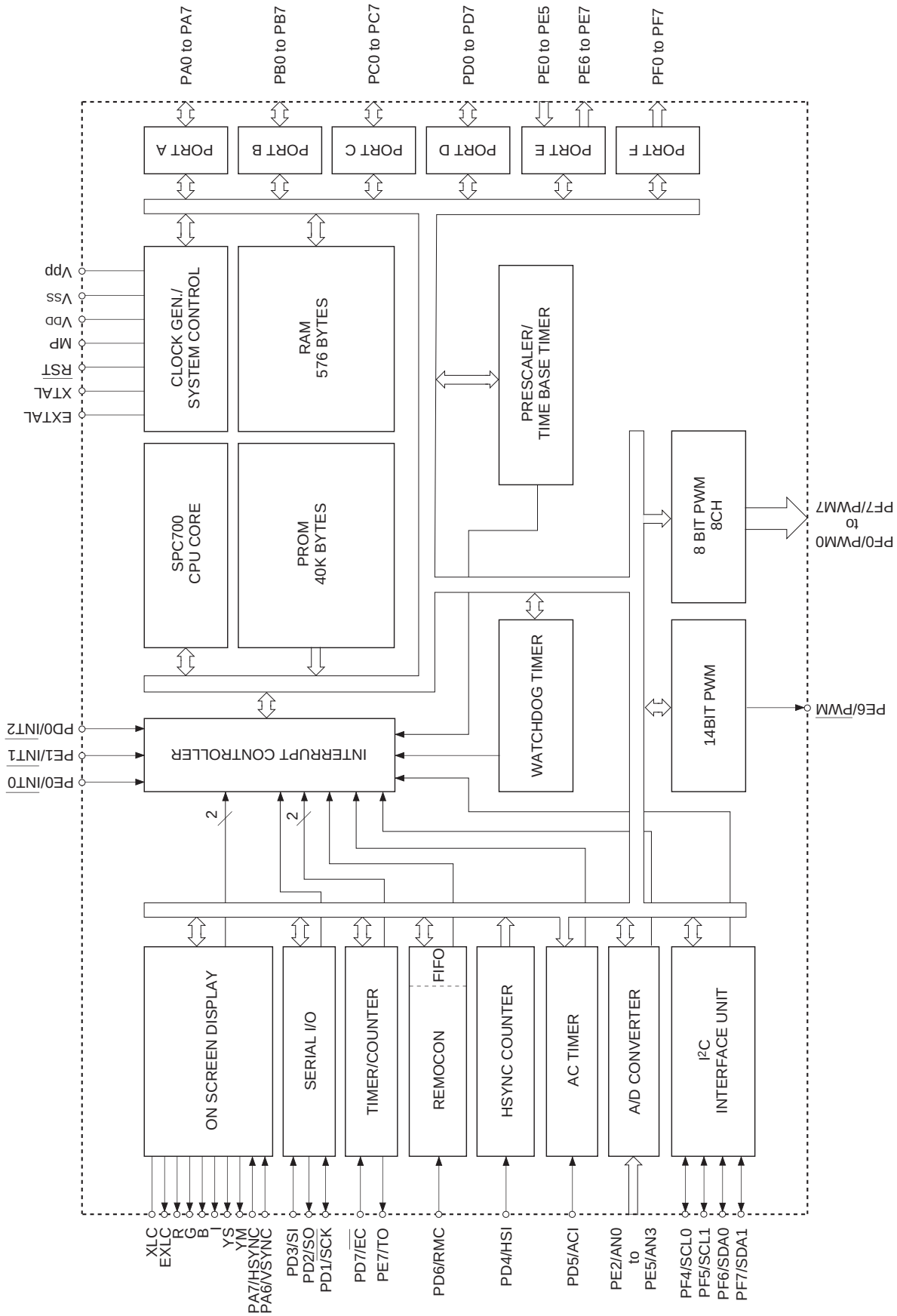
in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.

Features

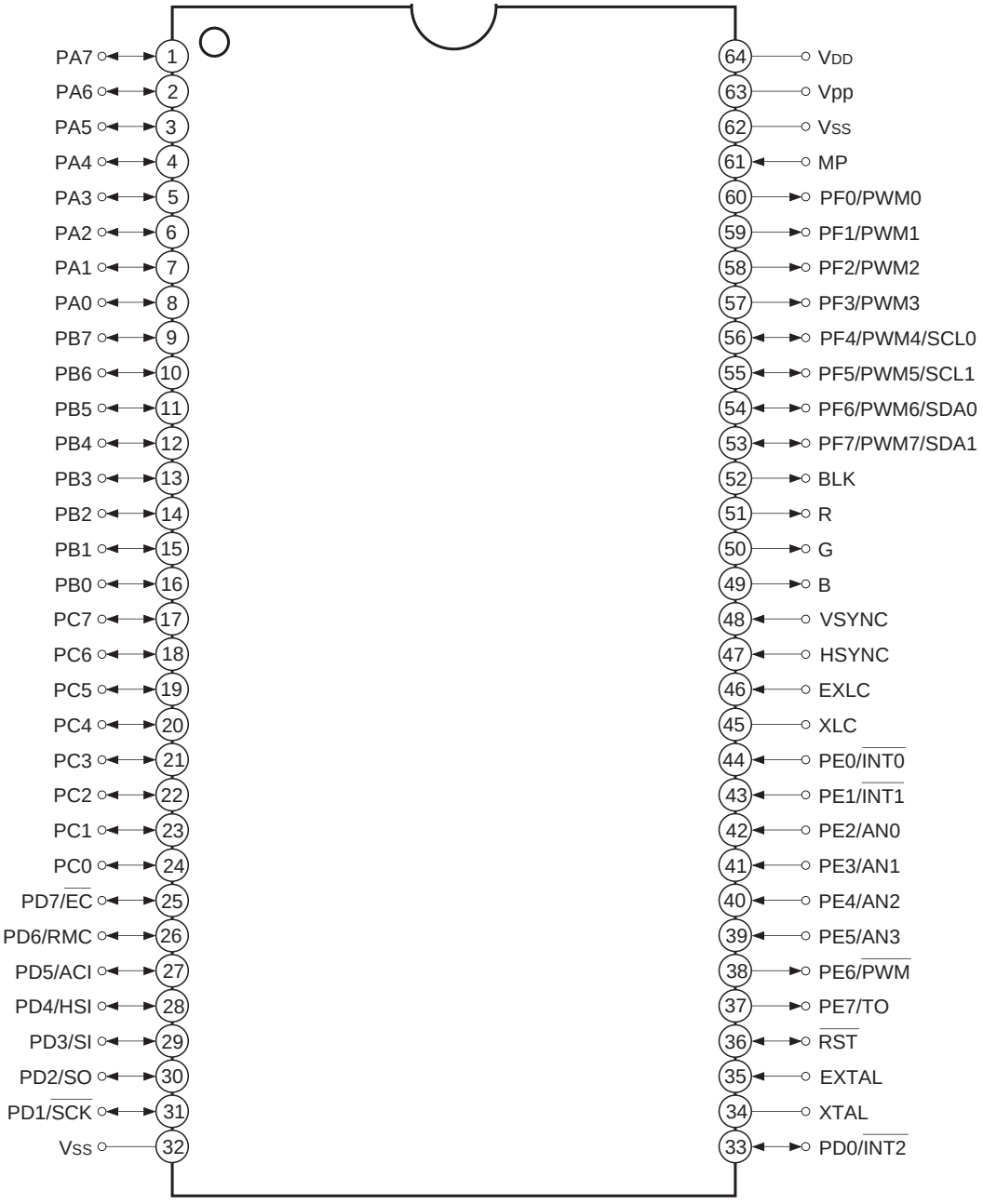
- A wide instruction set (213 instructions) which covers various of data
  - — 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle 1µs/4MHz (4MHz verison)
  0.5µs/8MHz (8MHz verison)
- Incorporated PROM capacity 40K bytes (For program)
  6.75K bytes (For OSD)
- Incorporated RAM capacity 576 bytes
- Peripheral funcitons
  - — On-screen display function 12 × 18 dots, 256 types, 15 colors, 12 lines of 21 characters
    Black frame output half blanking, shadow, background color on full screen/half blanking
    Double scanning mode supported, jitter elimination circuit
  - — I²C bus interface
  - — PWM output 14 bits, 1 channel
    8 bits, 8 channels
  - — Remote control receiver circuit 8-bit pulse measuring counter, 6-stage FIFO
  - — A/D converter 8-bit, 4 channels, successive approximation system
    (conversion time of 40µs/4MHz, 8MHz)
  - — HSYNC counter
  - — Power supply frequency counter
  - — Watchdog timer
  - — Serial I/O 8-bit synchronized
  - — Timer 8-bit timer, 8-bit timer/counter, 19-bit time-base timer
- Interruption 14 factors, 14 vectors, multiple interrupt possible
- Standby mode Sleep
- Package 64-pin plastic SDIP/QFP

E93Z19A7Z-PS

Block Diagram

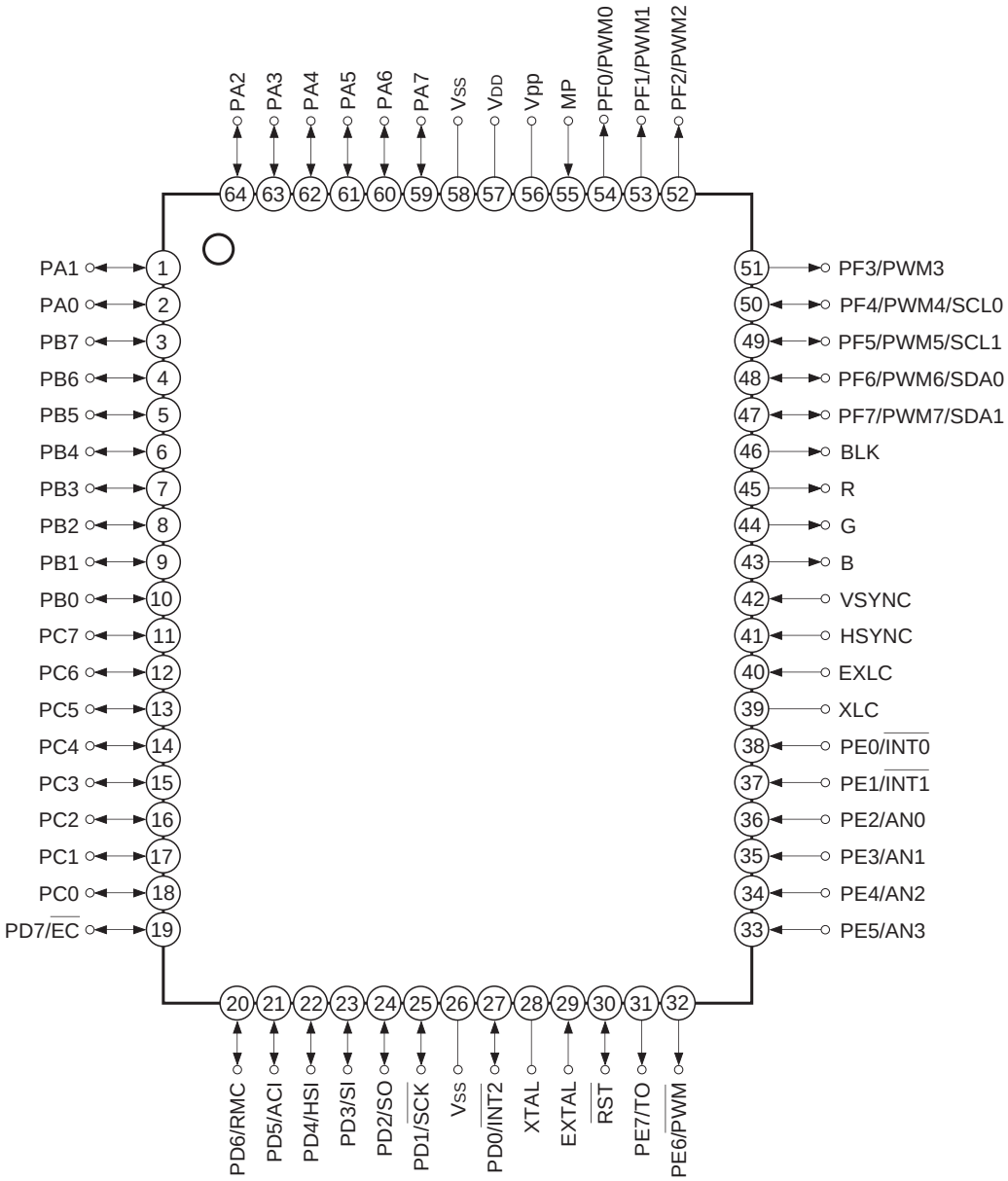


Pin Assignment 1 (Top View) 64 pin SDIP Package



Note) 1. Vpp (Pin 63) is always connected to V_{DD}.
2. Vss (Pins 32 and 62) are both connected to GND.
3. MP (Pin 61) is always connected to GND.

Pin Assignment 2 (Top View) 64 pin QFP Package



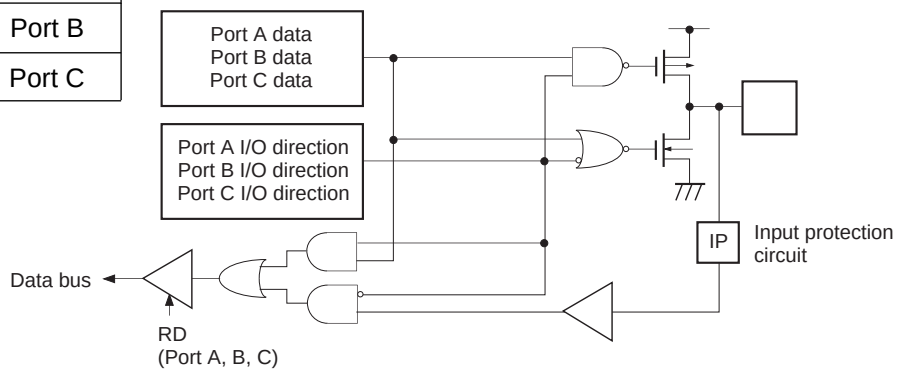
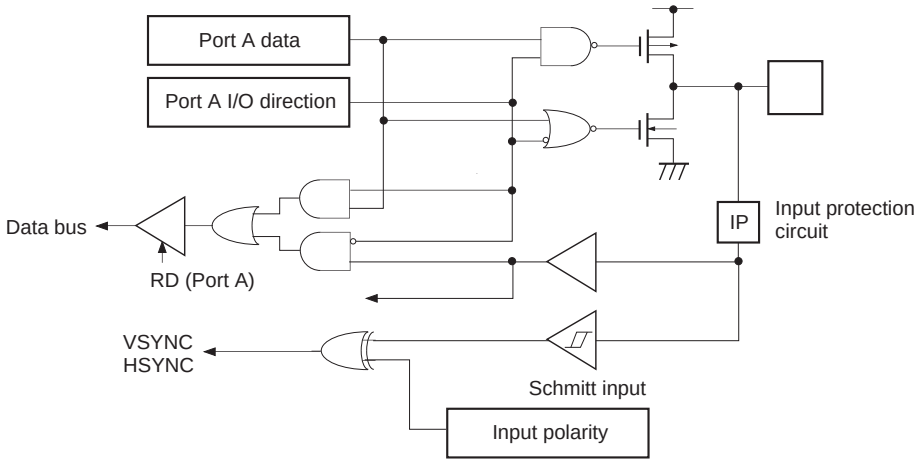
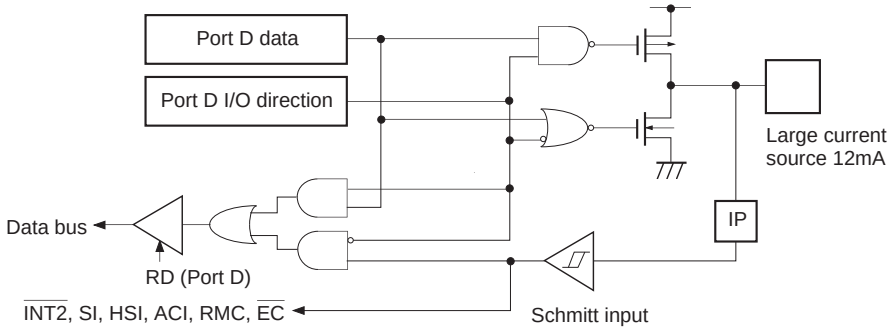
Note) 1. Vpp (Pin 56) is always connected to V_{DD}.
2. Vss (Pins 26 and 58) are both connected to GND.
3. MP (Pin 55) is always connected to GND.

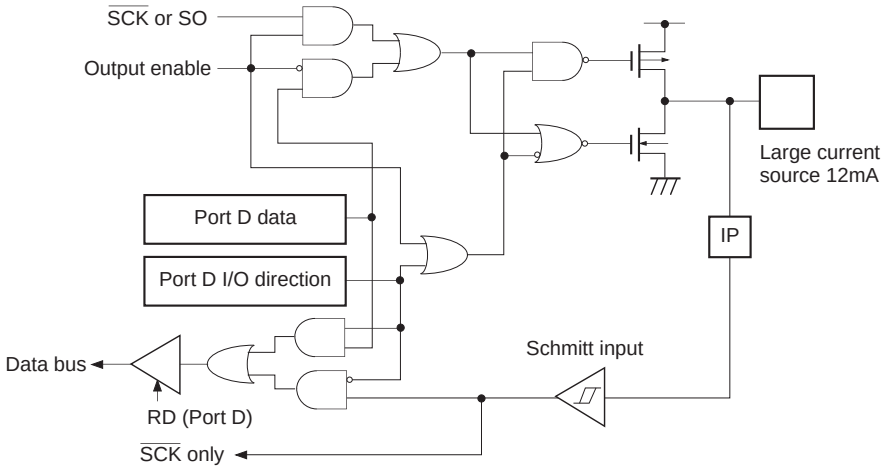
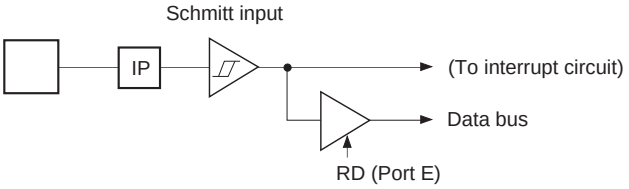
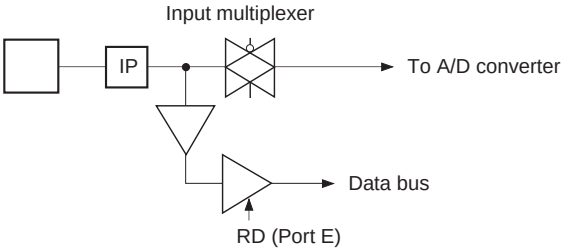
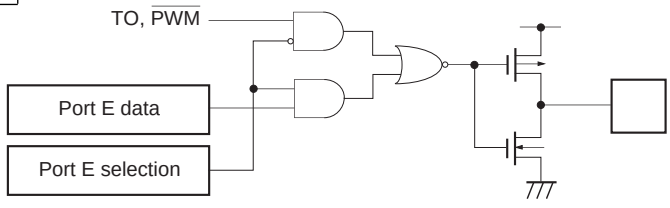
Pin Description

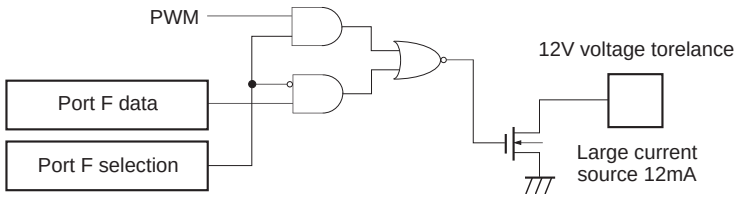
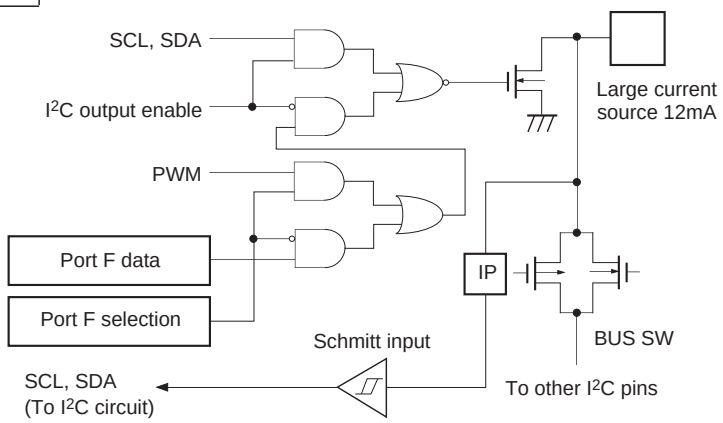
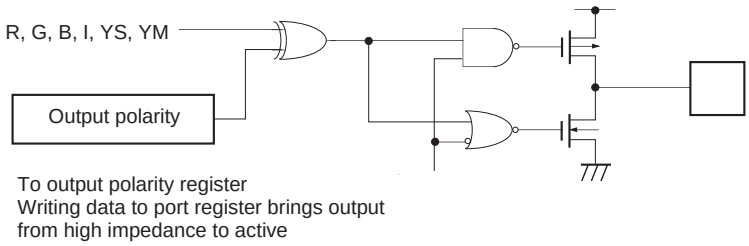
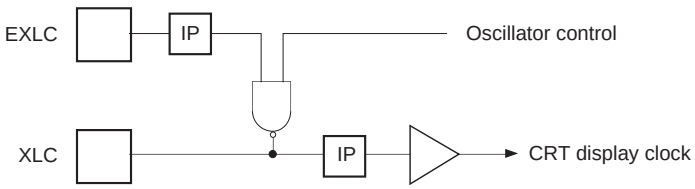
Symbol	I/O	Description	
PA0 to PA5	I/O	(Port A) Single bit selectable 8-bit I/O port. (8 pins)	
PA6/VSYNC	I/O/Input		CRT display vertical synchronization signal input pin.
PA7/HSYNC	I/O/Input		CRT display horizontal synchronization signal input pin.
PB0 to PB7	I/O	(Port B) Single bit selectable 8-bit I/O port. (8 pins)	
PC0 to PC7	I/O	(Port C) Single bit selectable 8-bit I/O port. (8 pins)	
PD0/$\overline{\text{INT2}}$	I/O/Input	(Port D) Single bit selectable 8-bit I/Oport. 12mA sink current drive possible. (8 pins)	Input pin for external interrupt request. Active on falling edge.
PD1/$\overline{\text{SCK}}$	I/O/I/O		Serial clock I/O pin.
PD2/SO	I/O/Output		Serial data output pin.
PD3/SI	I/O/Input		Serial data input pin.
PD4/HSI	I/O/Input		HSYNC counter input pin.
PD5/ACI	I/O/Input		Power supply frequency counter input pin.
PD6/RMC	I/O/Input		Remote control receiver circuit input pin.
PD7/$\overline{\text{EC}}$	I/O/Input		External event timer/counter input pin.
PE0/$\overline{\text{INT0}}$ PE1/$\overline{\text{INT1}}$	Input/Input	(Port E) 8-bit port, lower 6 bits for input, upper 2 bits for output. (8 pins)	Input pin for external interrupt request. Active on falling edge. (2 pins)
PE2/AN0 to PE5/AN3	Input/Input		Analog input pin for A/D converter. (4 pins)
PE6/$\overline{\text{PWM}}$	Output/Output		14-bit PWM output pin. (CMOS output)
PE7/TO	Output/Output		Square wave output for timer 1. (50% duty cycle)
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port with large current (12mA) N-ch open drain output. Lower 4 bits middle voltage tolerance (12V), upper 4 bits 5V suppression. (8 pins)	8-bit PWM output pin. (8 pins)
PF4/PWM4/ SCL0 PF5/PWM5/ SCL1	Output/Output/ I/O		I^2C bus interface transfer clock I/O pin.
PF6/PWM6/ SDA0 PF7/PWM7/ SDA1	Output/Output/ I/O		I^2C bus interface transfer data I/O pin.
R, G, B, I, YS, YM	Output	CRT display 6-bit output pin.	

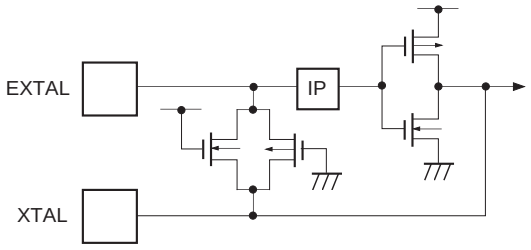
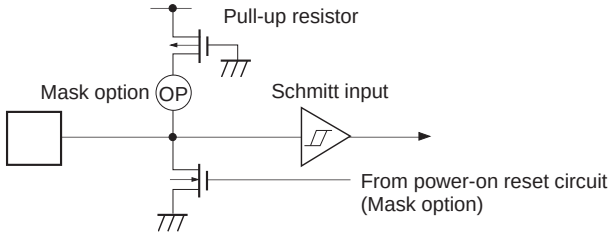
Symbol	I/O	Description
EXLC	Input	CRT display clock oscillator I/O pin. Oscillator frequency is determined by external L, C circuit.
XLC	Output	
EXTAL	Input	System clock oscillator crystal connection pin. When using an external clock, input to EXTAL pin and leave XTAL pin open.
XTAL	Output	
$\overline{RST}$	I/O	"L" level active system reset. This pin also acts as an I/O pin during power up. While internal power-on reset function is talking place a "L" level is output. (Mask option)
MP	Input	Test mode input pin. Must be connected to GND.
V_{DD}		Positive supply voltage pin.
Vpp		Positive power supply pin for incorporated PROM writing. Connect to V_{DD} for normal operation.
Vss		GND. Both Vss pins should be connected to common GND.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0 to PA5 PB0 to PB7 PC0 to PC7 22 pins	Port A Port B Port C 	Hi-Z
PA6/VSYNC PA7/HSYNC 2 pins	Port A 	Hi-Z
PD0/$\overline{\text{INT2}}$ PD3/SI PD4/HSI PD5/ACI PD6/$\overline{\text{RMC}}$ PD7/$\overline{\text{EC}}$ 6 pins	Port D 	Hi-Z

Pin	Circuit format	When reset
PD1/$\overline{\text{SCK}}$ PD2/SO 2 pins	Port D 	Hi-Z
PE0/$\overline{\text{INT0}}$ PE1/$\overline{\text{INT1}}$ 2 pins	Port E 	Hi-Z
PE2/AN0 to PE5/AN3 4 pins	Port E 	Hi-Z
PE6/$\overline{\text{PWM}}$ PE7/TO 2 pins	Port E 	High level

Pin	Circuit format	When reset
PF0/PWM0 to PF3/PWM3 4 pins	Port F 	Hi-Z
PF4/PWM4/ SCL0 PF5/PWM5/ SCL1 PF6/PWM6/ SDA0 PF7/PWM7/ SDA1 4 pins	Port F 	Hi-Z
R G B I YS YM 6 pins		Hi-Z
EXLC XLC 2 pins		Oscillation halted

Pin	Circuit format	When reset
EXTAL XTAL 2 pins		Oscillation
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13.0	V	Incorporated PROM
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
Medium voltage tolerance output voltage	V_{OUTP}	–0.3 to +15.0	V	Pins PF0 to PF3
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total of all output pins
Low level output current	I_{OL}	15	mA	Excludes large current output
	I_{OLC}	20	mA	Large current output*2
Low level total output current	$\sum I_{OL}$	130	mA	Total of all output pins
Operating temperature	Topr	–10 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	1000	mW	SDIP
		600	mW	QFP

*1 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*2 The large current drivetransistor for the PD and PF ports is a N-ch transistor.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed range during operation
		3.5	5.5	V	Guaranteed range for low speed data*1
		2.5	5.5	V	Guaranteed data hold operation range during stop
	Vpp	Vpp = V_{DD}		V	*5
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	I^2C Schmitt input included*2
	V_{IHS}	0.8V_{DD}	V_{DD}	V	CMOS Schmitt input*3
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin*4
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	I^2C Schmitt input included*2
	V_{ILS}	0	0.2V_{DD}	V	CMOS Schmitt input*3
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*4
Operating temperature	Topr	–10	+75	°C	

*1 Rating for 1/16 frequency mode and sleep mode.

*2 Normal input port (All pins of PA, PB, PC, PE2 to PE5), PF4 to PF7 pins.

*3 Includes PD0/$\overline{INT2}$, PD1/$\overline{SCK}$, PD2, PD3/SI, PD4/HSI, PD5/ACI, PD6/RMC, PD7/$\overline{EC}$, PE0/$\overline{INT0}$, PE1/$\overline{INT1}$, HSYNC, VSYNC, $\overline{RST}$ pins.

*4 It specifies only when the external clock is input.

*5 Vpp and V_{DD} should be set to the same voltage.

Electrical Characteristics

DC Characteristics

(Ta = –10 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE6, PE7, R, G, B, I, YS, YM	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}	PA to PD, PE6, PE7, R, G, B, I, YS, YM, PF0 to PF3, $\overline{RST}$	V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PF	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	V_{DD} = 4.5V, I_{OL} = 3.0mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 4.0mA			0.6	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{IHL}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{ILR}	$\overline{RST}$	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PE, HSYNC, VSYNC, R, G, B, I, YS, YM	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Open drain output leakage current (N-ch Tr off case)	I_{LOH}	PF0 to PF3	V_{DD} = 5.5V, V_{OH} = 12.0V			50	µA
		PF4 to PF7	V_{DD} = 5.5V, V_{OH} = 5.5V			10	µA
I^2C bus switch connection impedance (output Tr off case)	R_{BS}	SCL0: SCL1 SDA0: SDA1	V_{DD} = 4.5V V_{SCL0} = V_{SCL1} = 2.25V V_{SDA0} = V_{SDA1} = 2.25V			120	Ω
Supply current	I_{DD}	V_{DD}*1	Operating mode (1/2, 1/4 clock rate) 4MHz, 8MHz crystal oscillator (C_1 = C_2 = 22pF) All output pins open		11*2	30*2	mA
					17*3	40*3	
	I_{DDSL}		Sleep mode		0.6*2	3*2	mA
					0.8*3	3*3	
	I_{DDST}		Stop mode*4	—	—	—	µA
Input capacitance	C_{IN}	Pins other than V_{DD} and Vss	1MHz clock 0V other than the measure pins		10	20	pF

*1 Rating applies only if OSD oscillator is halted.

*2 Oscillator clock 4MHz version

*3 Oscillator clock 8MHz version

*4 This device does not enter the stop mode.

AC Characteristics

(1) Clock timing

(Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	3.5*2	4.5	MHz
				7*3	9	
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	100*2		ns
				50*3		
System clock rise and fall times	t_{CR}, t_{CF}	EXTAL	Fig 1, Fig 2 External clock drive		200	ns
Event counter input clock pulse widtth	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	tsys + 50*1		ns
Event counter input clock rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3		20	ms

*1 tsys indicates one of three values according to the contents of the clock control register (address : 00FE$_H$) upper 2 bits (CPU clock selection)
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

*2 Oscillator clock 4MHz version

*3 Oscillator clock 8MHz version

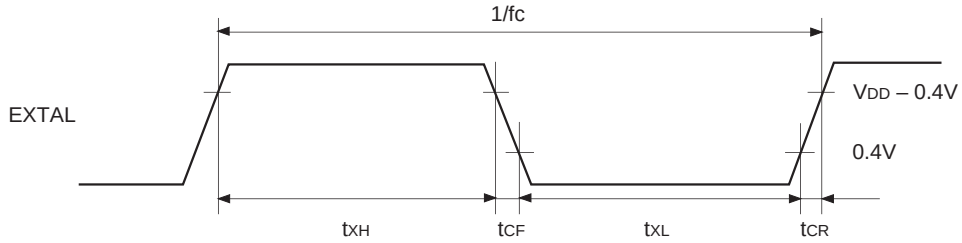


Fig. 1. Clock timing

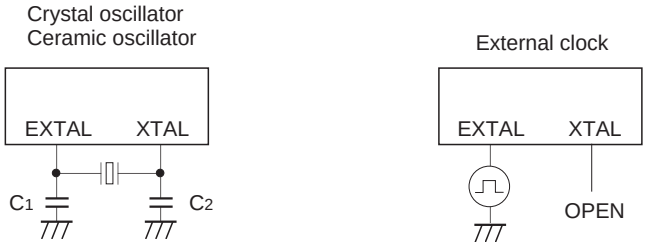


Fig. 2. Clock applied condition

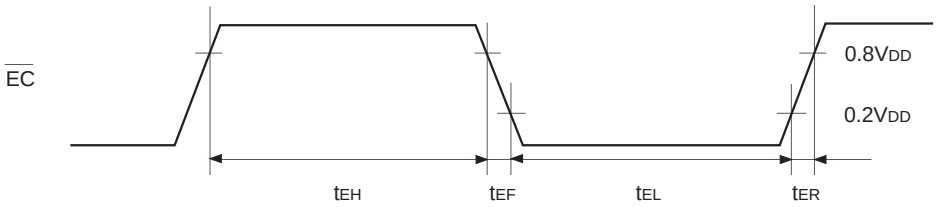


Fig. 3. Event count clock timing

(2) Serial transfer (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK}$	Input mode	1000		ns
			Output mode	8000/fc'*1		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK}$	$\overline{SCK}$ input mode			ns
			$\overline{SCK}$ output mode	400		ns
SI input setup time (referenced to $\overline{SCK}$ ↑)	t_{SIK}	SI	$\overline{SCK}$ input mode	4000/fc' – 50*1		ns
			$\overline{SCK}$ output mode	100		ns
SI input hold time (referenced to $\overline{SCK}$ ↑)	t_{KSI}	SI	$\overline{SCK}$ input mode	200		ns
			$\overline{SCK}$ output mode	200		ns
$\overline{SCK}$ ↓ → SO delay time	t_{KSO}	SO	$\overline{SCK}$ input mode	100	200	ns
			$\overline{SCK}$ output mode		100	ns

Note) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

*1 The value of fc' varies as shown below depending on the specification of oscillation clock option.
4MHz version ... fc' = fc
8MHz version ... fc' = fc/2

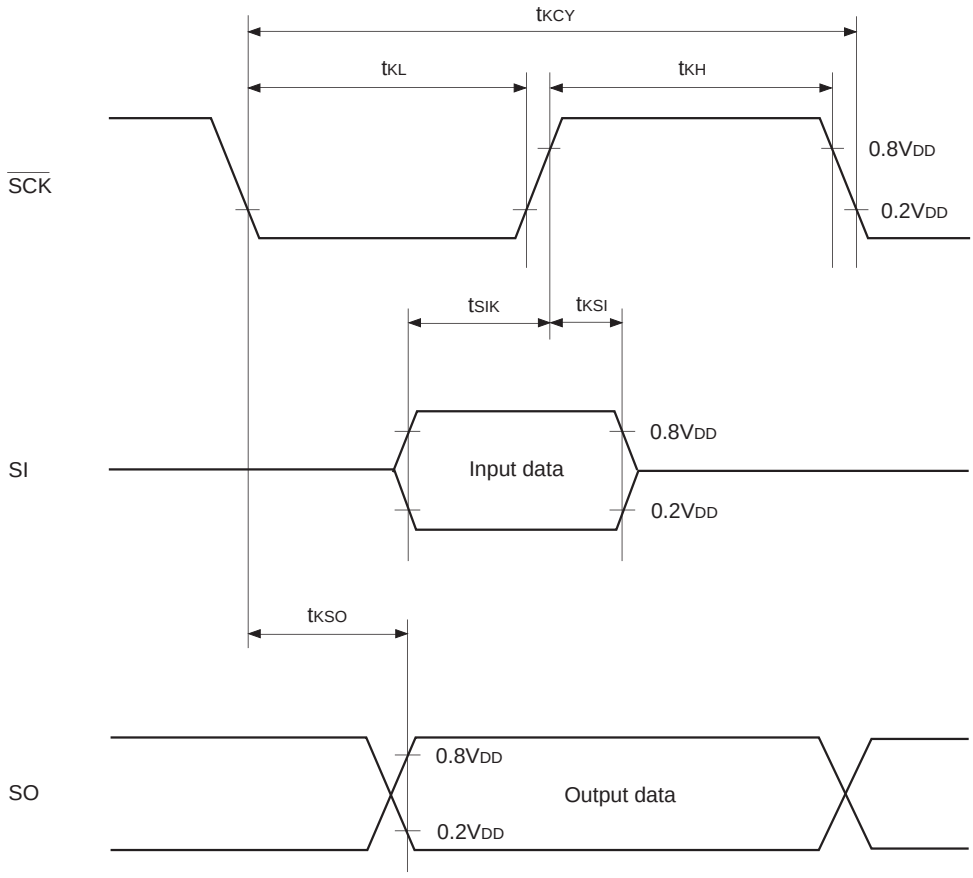


Fig. 4. Serial transfer timing

(3) Interrupt, Reset input (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interrupt High and Low level widths	t_{IH} t_{IL}	$\overline{INT0}$ to $\overline{INT2}$		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		8/fc' *1		µs

*1 The value of fc' varies as shown below depending on the specification of oscillation clock option.
4MHz version ... fc' = fc
8MHz version ... fc' = fc/2

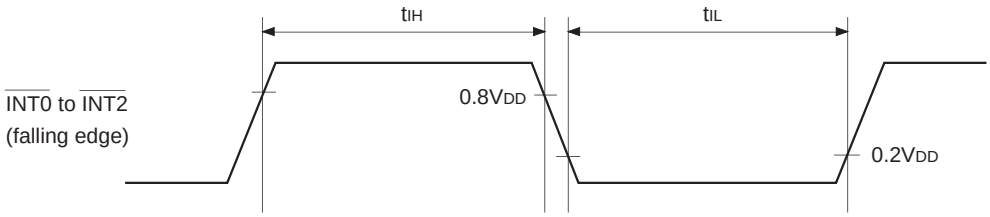


Fig. 5. Interrupt input timing

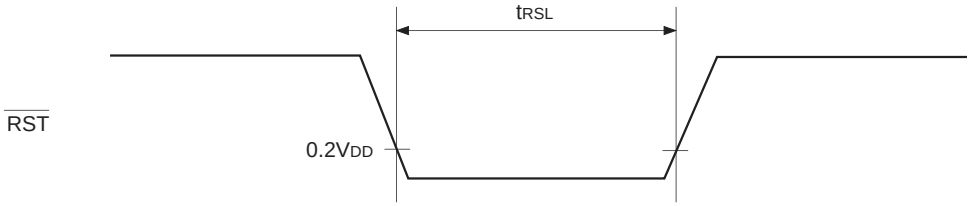
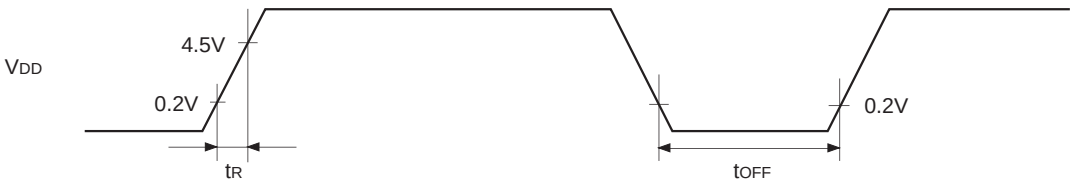


Fig. 6. $\overline{RST}$ input timing

(4) Power-on reset

Power-on reset (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rise time	t_R	V_{DD}	Power-on reset	0.05	50	ms
Power supply cutt-off time	t_{OFF}		Repeated power-on reset	1		ms

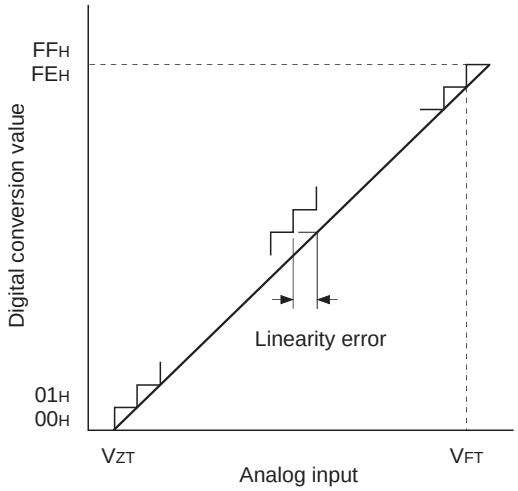


The power supply should rise smoothly.

Fig. 7. Power-on reset

(5) A/D converter characteristics (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = 5.0V Vss = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–10	70	150	mV
Full-scale transition voltage	V_{FT}*2			4930	5050	5120	mV
Conversion time	t_{CONV}			160/fc' *3			µs
Sampling time	t_{SAMP}			12/fc' *3			µs
Analog input voltage	V_{IAN}	AN0 to AN3		0		V_{DD}	V



*1 V_{ZT}: Digital conversion values change between $00_H \longleftrightarrow 01_H$.

*2 V_{FT}: Digital conversion values change between $FE_H \longleftrightarrow FF_H$.

*3 The value of fc' varies as shown below depending on the specification of oscillation clock option.
4MHz version ... fc' = fc
8MHz version ... fc' = fc/2

Fig. 8. Definitions for A/D converter terms

(6) I²C bus timing (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f_{SLC}	SCL		0	100	kHz
Bus free time before starting transfer	t_{BUF}	SDA, SCL		4.7		µs
Hold time for starting transfer	$t_{HD;\,STA}$	SDA, SCL		4.0		µs
Clock Low level width	t_{LOW}	SCL		4.7		µs
Clock High level width	t_{HIGH}	SCL		4.0		µs
Setup time for repetitive transfers	$t_{SU;\,STA}$	SDA, SCL		4.7		µs
Data hold time	$t_{HD;\,DAT}$	SDA, SCL		0*1		µs
Data setup time	$t_{SU;\,DAT}$	SDA, SCL		250		ns
SDA, SCL rise time	t_R	SDA, SCL			1	µs
SDA, SCL fall time	t_F	SDA, SCL			300	ns
Setup time for transfer completion	$t_{SU;\,STO}$	SDA, SCL		4.7		µs

*1 Since for part of data hold time SCL rise time (max: 300ns) is not considered , allow at least 300ns.

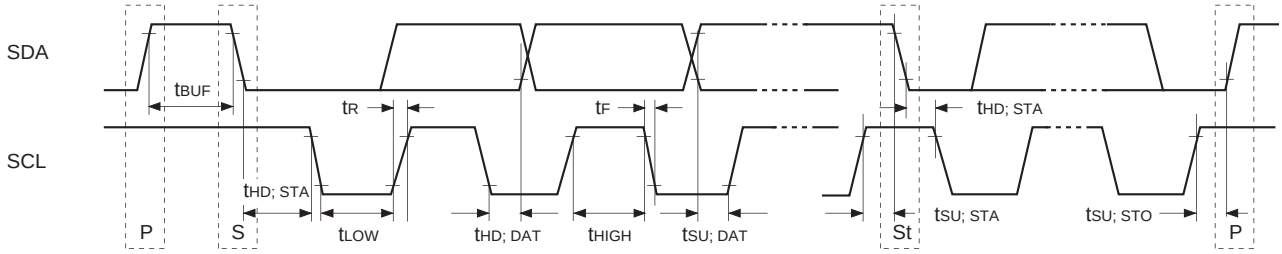


Fig. 9. I²C bus transfer data timing

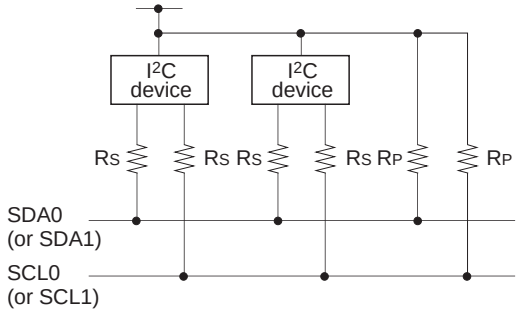


Fig. 10. I²C device recommended circuit

- A pull-up resistor (R_P) must be connected to SDA0 (or SDA1), and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be used to reduce spike noise caused by CRT flashover.

(7) OSD (On Screen Display) timing (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condiiton	Shadow Existent		Shadow Non-existent		Unit
				Min.	Max.	Min.	Max.	
OSD clock frequency	f_{OSC}	EXLC XLC	Fig. 12	4	7*1	4	11*1	MHz
					14*2		16*2	
HSYNC pulse width	t_{HWD}	HSYNC	Fig. 11	1.2		1.2		µs
HSYNC afterwrite rise and fall times	t_{HCG}	HSYNC	Fig. 11		200		200	ns
VSYNC afterwrite rise and fall times	t_{VCG}	VSYNC	Fig. 11		1.0		1.0	µs

*1 Oscillator clock 4MHz version

*2 Oscillator clock 8MHz version

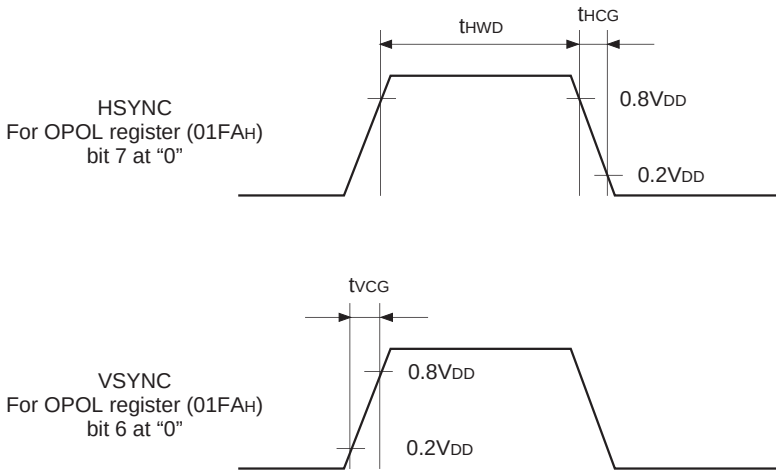


Fig. 11. OSD timing

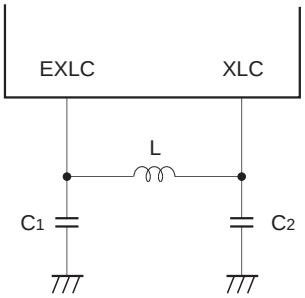


Fig. 12. LC oscillator circuit connection

Supplement

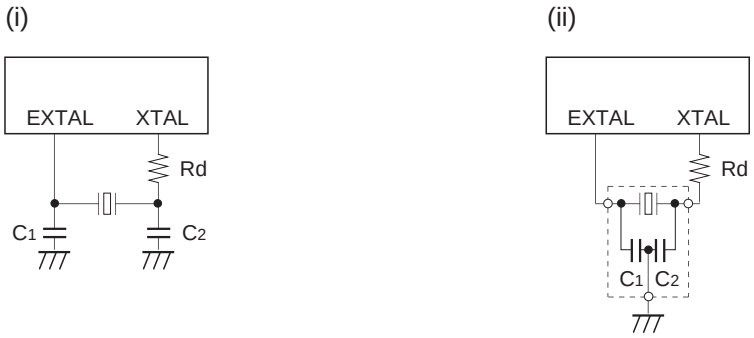


Fig. 13. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit Example
MURATA MFG CO., LTD.	CSA4.00MG	4.00	30	30	0	(i)
	CSA4.19MG	4.19				
	CSA8.00MTZ	8.00				
	CST4.00MGW*	4.00				(ii)
	CST4.19MGW*	4.19				
	CST8.00MTW*	8.00				
RIVER ELETEC CORPORATION	HC-49/U03	4.00	12	12	0	(i)
		4.19				
		8.00				
KINSEKI LTD.	HC-49/U(-S)	4.00	27	27	0	(i)
		4.19				
		8.00				

* Indicates types with on-chip grounding capacitors (C_1 and C_2).

Product List

Option item	Mask	CXP853P40AS-2-□□□ CXP853P40AQ-2-□□□	CXP853P40AS-3-□□□ CXP853P40AQ-3-□□□
Package	64-pin plastic SDIP/QFP	64-pin plastic SDIP/QFP	64-pin plastic SDIP/QFP
PROM capacitance	24K/32K/40K bytes	PROM 40K bytes	PROM 40K bytes
Reset pin pull-up resistor	Existent/Non-existent	Existent	Existent
Power-on reset circuit	Existent/Non-existent	Existent	Existent
Font data	User specified	User specified (PROM)*1	User specified (PROM)*1
Oscillator clock	4MHz/8MHz	4MHz	8MHz

*1 The font data for the one-time PROM version is operated in the same way as the program writing.

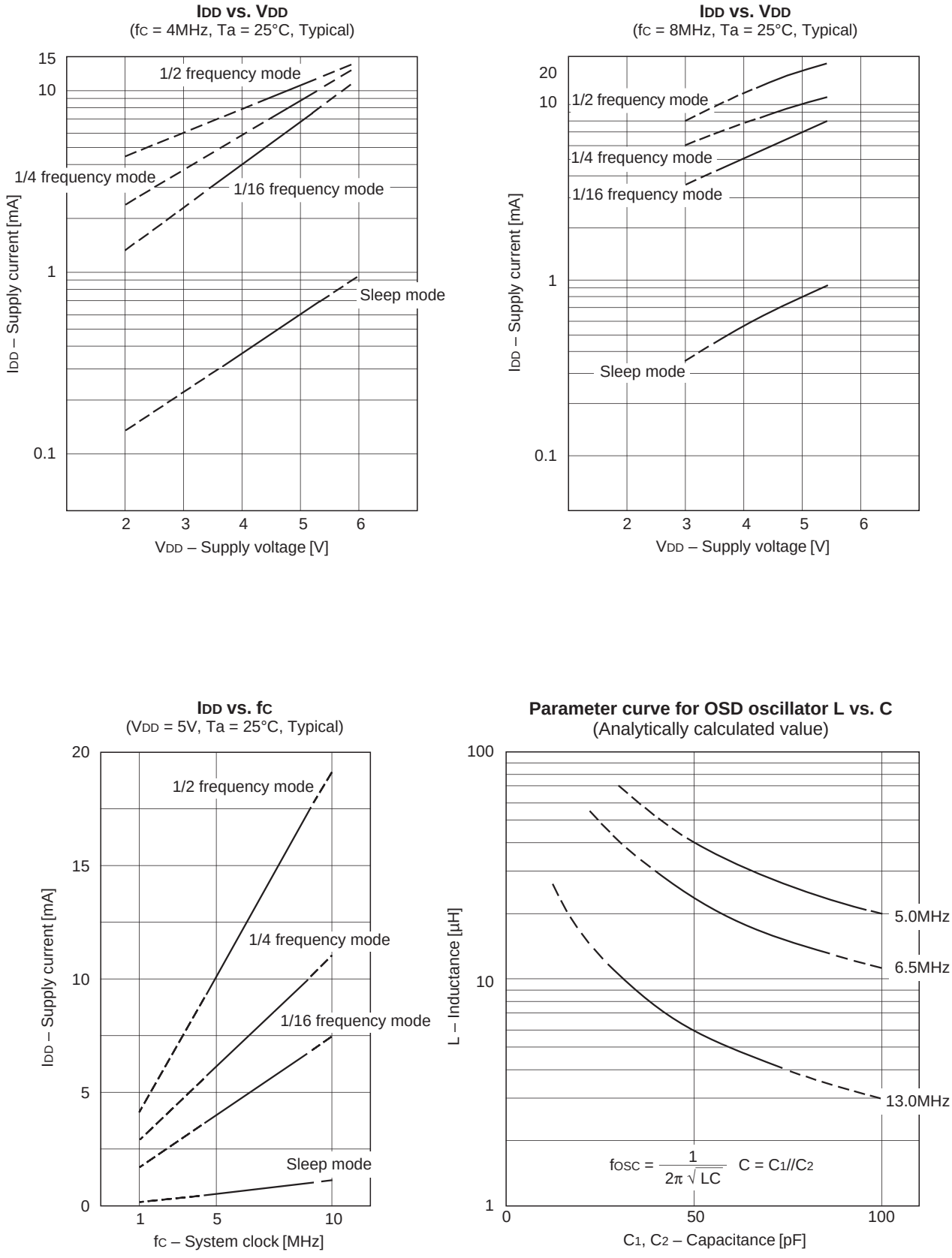
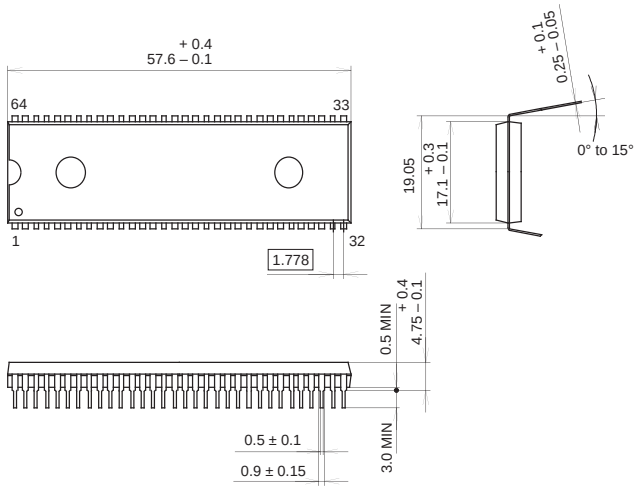


Fig. 14. Characteristic curves

Package Outline Unit: mm

64PIN SDIP (PLASTIC)

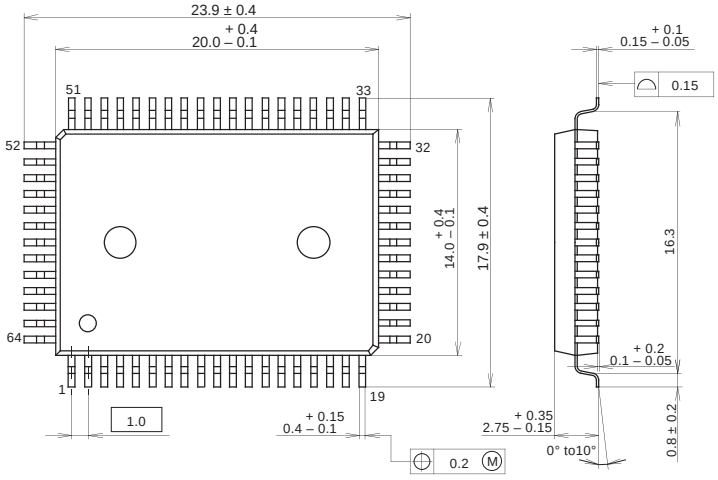


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	SDIP064-P-0750
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	8.6g

64PIN QFP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	QFP064-P-1420
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g