DATA SHEET

SEE THE LAST 2 PAGES OF THIS DATA SHEET FOR A LIST OF ERRATA RELATED TO THIS PART.

P87C51MB2/P87C51MC2

80C51 8-bit microcontroller family with extended memory

64KB/96KB OTP with 2KB/3KB RAM

Preliminary specification

2001 Apr 06

Philips Semiconductors

PHILIPS

GENERAL DESCRIPTION

The P87C51Mx2 represents the first microcontroller based on Philips Semiconductors' new 51MX core. The P87C51MC2 features 96 Kbytes of OTP program memory and 3 Kbytes of data SRAM, while the P87C51MB2 has 64 Kbytes of OTP and 2 Kbytes of RAM. In addition, both devices are equipped with a Programmable Counter Array (PCA), a watchdog timer that can be configured to different time ranges through SFR bits, as well as two enhanced UARTs or one enhanced UART and an SPI.

Philips Semiconductors' 51MX (Memory eXtension) core is an accelerated 80C51 architecture that executes instructions at twice the rate of standard 80C51 devices. The linear address range of the 51MX has been expanded to support up to 8 Mbytes of program memory and 8Mbytes of data memory. It retains full program code compatibility to enable design engineers to re-use 80C51 development tools, eliminating the need to move to a new, unfamiliar architecture. The 51MX core also retains 80C51 bus compatibility to allow for the continued use of 80C51-interfaced peripherals and Application Specific Integrated Circuits (ASICs).

The P87C51Mx2 provides greater functionality, increased performance and overall lower system cost. By offering an embedded memory solution combined with the enhancements to manage the memory extension, the P87C51Mx2 eliminates the need for software work-arounds. The increased program memory enables design engineers to develop more complex programs in a high-level language like C, for example, without struggling to contain the program within the traditional 64 Kbytes of program memory. These enhancements also greatly improve C Language efficiency for code size below 64 Kbytes.

The 51MX core is described in more details in the 51MX Architecture Reference.

KEY FEATURES

- Extended features of the 51MX Core:
  - 23-bit program memory space and 23-bit data memory space - linear program and data address range expanded to support up to 8 Mbytes each
  - Program counter expanded to 23 bits
  - Stack pointer extended to 16 bits enabling stack space beyond the 80C51 limitation
  - New 23-bit extended data pointer and two 24-bit universal pointers greatly improve C compiler code efficiency in using pointers to access variables in different spaces.
- 100% binary compatibility with the classic 80C51 so that existing code is completely reusable
- Up to 24 MHz CPU clock with 6 clock cycles per machine cycle
- 96 Kbytes or 64 Kbytes of on-chip OTP
- 3 Kbytes or 2 Kbytes of on-chip RAM
- Programmable Counter Array (PCA)
- Two full-duplex enhanced UARTs
- Industry-standard Serial Peripheral Interface (SPI)

KEY BENEFITS

- Increases program/data address range to 8 Mbytes each
- Enhances performance and efficiency for C programs
- Fully 80C51-compatible microcontroller
- Provides seamless and compelling upgrade path from classic 80C51
- Preserves 80C51 code base, investment/knowledge, and peripherals & ASICs
- Supported by 80C51 development and programming tools (Keil, Nohau, BP Micro, etc.)
- The P87C51Mx2 makes it possible to develop applications at a lower cost and with a reduced time-to-market

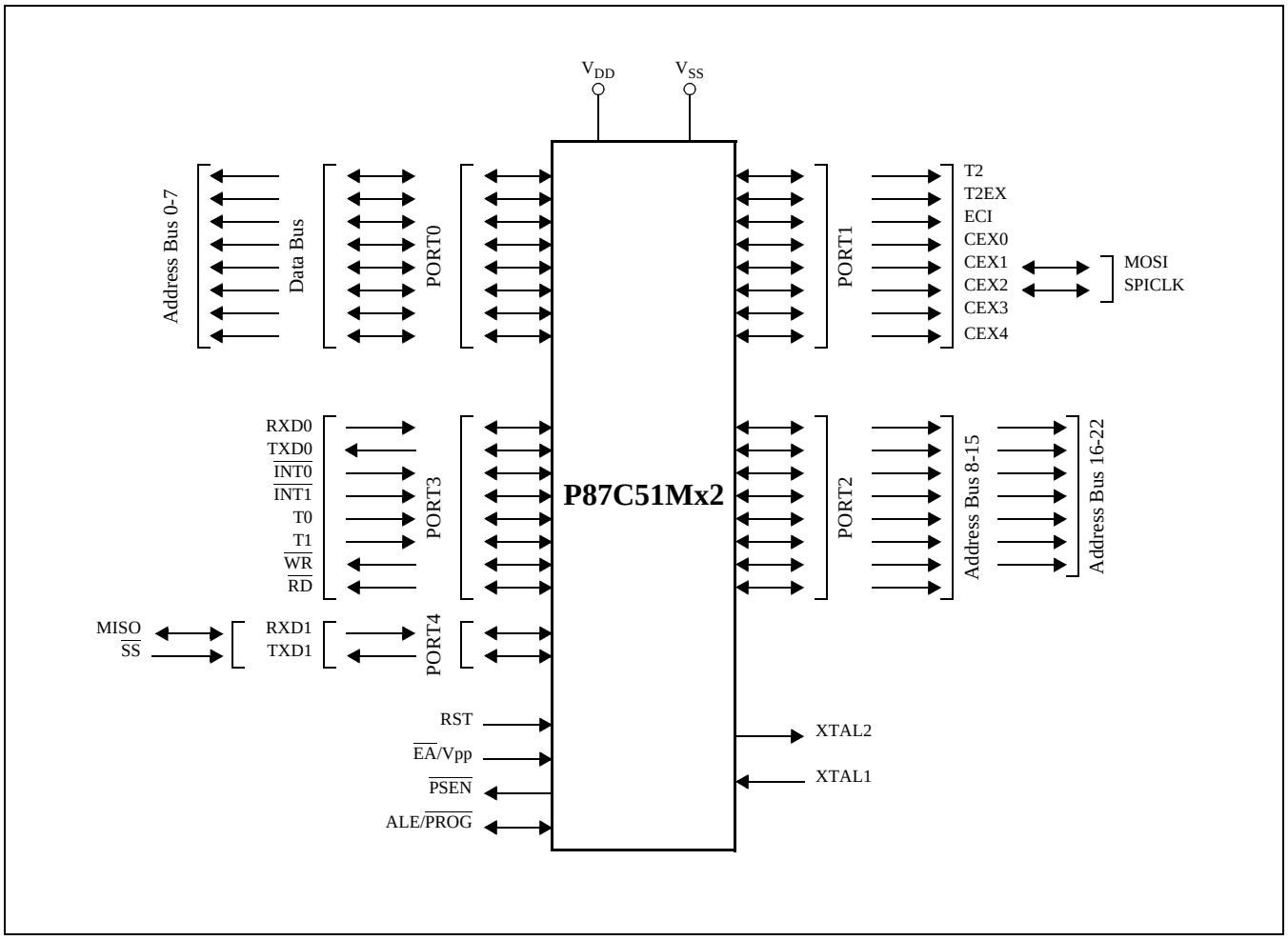
COMPLETE FEATURES

- Fully static
- Up to 24 MHz CPU clock with 6 clock cycles per machine cycle
- 96 Kbytes or 64 Kbytes of on-chip OTP
- 3 Kbytes or 2 Kbytes of on-chip RAM
- 23-bit program memory space and 23-bit data memory space
- Four-level interrupt priority
- 34 I/O lines (5 ports)
- Three Timers: Timer0, Timer1 and Timer2
- Two full-duplex enhanced UARTs with baud rate generator
- Framing error detection
- Automatic address recognition
- Supports industry-standard Serial Peripheral Interface (SPI) with a baud rate up to 6 Mbits/sec
- Power control modes
- Clock can be stopped and resumed
- Idle mode
- Power down mode
- Second DPTR register
- Asynchronous port reset
- Programmable Counter Array (PCA) (compatible with 8xC51Rx+) with five Capture/Compare modules
- Low EMI (inhibit ALE)
- Watchdog timer with programmable prescaler for different time ranges (compatible with 8xC66x with added prescaler)

ORDERING INFORMATION

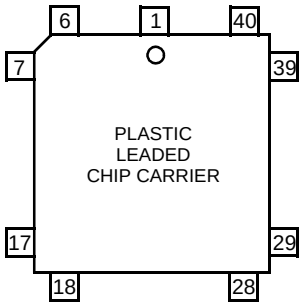
	PART ORDER NUMBER	MEMORY		TEMPERATURE RANGE AND PACKAGE	V_{DD} VOLTAGE RANGE		FREQUENCY		DWG #
		OTP	RAM				V_{DD} = 2.7-5.5V	V_{DD} = 4.5-5.5V	
1	P87C51MB2BA	64 KB	2048 B	0 to +70°C, PLCC44	2.7-5.5V	4.5-5.5V	0-12MHz	0-24MHz	SOT187-2
2	P87C51MC2BA	96 KB	3072 B	0 to +70°C, PLCC44	2.7-5.5V	4.5-5.5V	0-12MHz	0-24MHz	SOT187-2

LOGIC SYMBOL



PIN CONFIGURATION

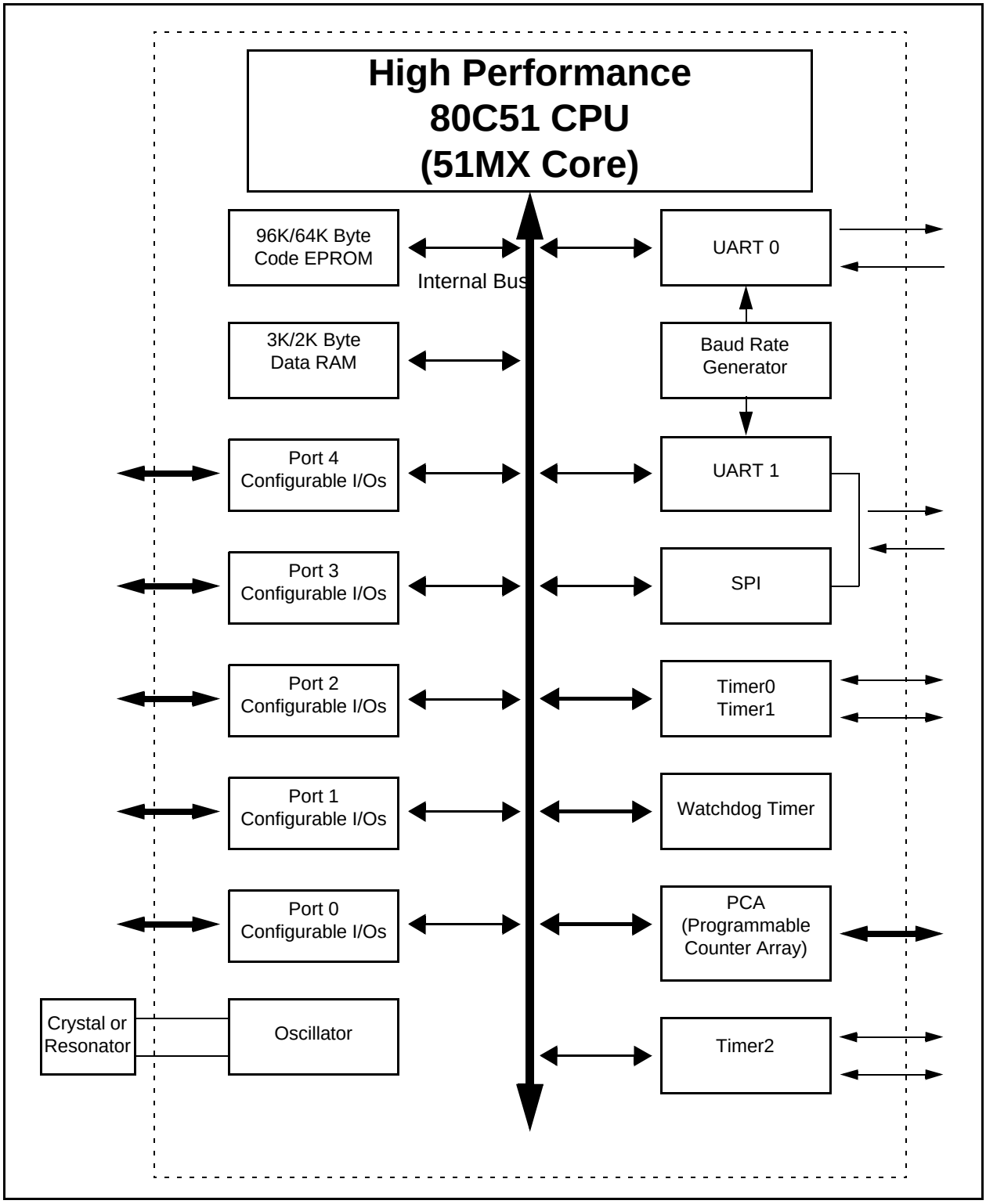
PLCC44



Pin	Function	Pin	Function
1	(NC/V_{SS})[1]	23	(NC/V_{DD})[1]
2	P1.0/T2	24	P2.0/A8/A16
3	P1.1/T2EX	25	P2.1/A9/A17
4	P1.2/ECI	26	P2.2/A10/A18
5	P1.3/CEX0	27	P2.3/A11/A19
6	P1.4/CEX1/MOSI	28	P2.4/A12/A20
7	P1.5/CEX2/SPICLK	29	P2.5/A13/A21
8	P1.6/CEX3	30	P2.6/A14/A22
9	P1.7/CEX4	31	P2.7/A15
10	RST	32	$\overline{PSEN}$
11	P3.0/RXD0	33	ALE
12	P4.0/RXD1/MISO[1]	34	P4.1/TXD1/$\overline{SS}$[1]
13	P3.1/$\overline{TXD0}$	35	$\overline{EA}$/Vpp
14	P3.2/$\overline{INT0}$	36	P0.7/AD7
15	P3.3/$\overline{INT1}$	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/$\overline{WR}$	40	P0.3/AD3
19	P3.7/$\overline{RD}$	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	V_{SS}	44	V_{DD}

1. Pins 1, 12, 23, 34 were not internally connected in some derivatives. Please refer to section on Pin Descriptions for details.

BLOCK DIAGRAM



PIN DESCRIPTIONS

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION		
P0.0 - P0.7	43 - 36	I/O	**Port 0:** Port 0 is an open drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impendance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.		
P1.0 - P1.7	2 - 9	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups on all pins. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (Note: When SFR bit SPEN (SPCTL.6) is '1', the pull-ups at P1.4 and P1.5 are disabled.)		
	2	I/O	**P1.0**	**T2**	Timer/Counter 2 external count input/Clockout
	3	I	**P1.1**	**T2EX**	Timer/Counter 2 Reload/Capture/Direction Control
	4	I	**P1.2**	**ECI**	External Clock Input to the PCA
	5	I/O	**P1.3**	**CEX0**	Capture/Compare External I/O for PCA module 0
	6	I/O	**P1.4**	**CEX1**	Capture/Compare External I/O for PCA module 1 (with pull-up on pin)
		I/O		**MOSI**	SPI Master Out/Slave In (Selected when SFR bit SPEN (SPCTL.6) is '1', in which case the pull-up for this pin is disabled)
	7	I/O	**P1.5**	**CEX2**	Capture/Compare External I/O for PCA module 2 (with pull-up on pin)
		I/O		**SPICLK**	SPI Clock (Selected when SFR bit SPEN (SPCTL.6) is '1', in which case the pull-up for this pin is disabled)
	8	I/O	**P1.6**	**CEX3**	Capture/Compare External I/O for PCA module 3
	9	I/O	**P1.7**	**CEX4**	Capture/Compare External I/O for PCA module 4
P2.0 - P2.7	24 - 31	I/O	**Port 2:** Port 2 is a 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR) or 23-bit addresses (MOVX @EPTR, EMOV). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @ Ri), port2 emits the contents of the P2 Special Function Register. Note that when 23-bit address is used, address bits A16-A22 will be output to P2.0-P2.6 when ALE is High, and address bits A8-A14 are output to P2.0-P2.6 when ALE is Low. Address bit A15 is output on P2.7 regardless of ALE.		
P3.0 - P3.7	11,13 -19	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally pulled low will source current because of the internal pull-ups.		
	11	I	**P3.0**	**RXD0**	Serial input port 0
	13	O	**P3.1**	**TXD0**	Serial output port 0
	14	I	**P3.2**	**INT0**	External interrupt 0
	15	I	**P3.3**	**INT1**	External interrupt 1
	16	I	**P3.4**	**T0**	Timer0 external input
	17	I	**P3.5**	**T1**	Timer1 external input
	18	O	**P3.6**	**WR**	External data memory write strobe
	19	O	**P3.7**	**RD**	External data memory read strobe

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
P4.0 - P4.1	12,34	I/O	**Port 4:** Port 4 is an 8-bit bidirectional I/O port with internal pull-ups on all pin. Port 4 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 4 pins that are externally pulled low will source current because of the internal pull-ups. (Note: When SFR bit SPEN (SPCTL.6) is '1', the pull-ups at these port pins are disabled.)
	12	I	**P4.0** **RXD1** Serial input port 1. (Note: This pin is a no connect pin on some derivatives.) (with pull-up on pin)
		I/O	**MISO** SPI Master In/Slave Out (Selected when SFR bit SPEN (SPCTL.6) is '1', in which case the pull-up for this pin is disabled)
	34	O	**P4.1** **TXD1** Serial output port 1. (Note: This pin is a no connect pin on some derivatives.) (with pull-up on pin)
		I	**$\overline{SS}$** SPI Slave Select (Selected when SFR bit SPEN (SPCTL.6) is '1', in which case the pull-up for this pin is disabled)
RST	10	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to $V_{DD.}$
ALE	33	O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. If SFR bit AO (AUXR.0) is '0', ALE is emitted at the constant rate as indicated above. With this bit set to '1', ALE will be active only during a MOVX instruction.
$\overline{PSEN}$	32	O	**Program Store Enable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}$/Vpp	35	I	**External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations. If $\overline{EA}$ is held high, the device executes from internal program memory. The value on the $\overline{EA}$ pin is latched when RST is released and any subsequent changes have no effect.
XTAL1	21	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	20	O	**Crystal 2:** Output from the inverting oscillator amplifier.
V_{SS}	22	I	**Ground:** 0V reference.
V_{DD}	44	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power Down modes.
(NC/V_{SS})	1	I	**No Connect/Ground:** This pin is a no connect pin on some derivatives, but is internally connected to V_{SS} on the P87C51Mx2. If connected externally, this pin must only be connected to the same V_{SS} as at pin 22. (Note: Connecting the second pair of V_{SS} and V_{DD} pins is not required. However, they may be connected in addition to the primary V_{SS} and V_{DD} pins to improve power distribution, reduce noise in output signals, and improve system-level EMI characteristics.)
(NC/V_{DD})	23	I	**No Connect/Power Supply:** This pin is a no connect pin on some derivatives, but is internally connected to V_{DD} on the P87C51Mx2. If connected externally, this pin must only be connected to the same V_{DD} as at pin 44. (Note: Connecting the second pair of V_{SS} and V_{DD} pins is not required. However, they may be connected in addition to the primary V_{SS} and V_{DD} pins to improve power distribution, reduce noise in output signals, and improve system-level EMI characteristics.)

SPECIAL FUNCTION REGISTERS

Note: Special Function Register (SFR) accesses are restricted in the following ways:

1. User must NOT attempt to access any SFR locations not defined.
2. SFR bits labeled '-', '0' or '1' can ONLY be written and read as follows:
   - '-' MUST be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
   - '0' MUST be written with '0', and will return a '0' when read.
   - '1' MUST be written with '1', and will return a '1' when read.

Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATE PORT FUNCTION MSB							LSB	Reset Value
			E7	E6	E5	E4	E3	E2	E1	E0	
ACC*	Accumulator	E0H									00H
AUXR#	Auxiliary Function Register	8EH	-	-	-	-	-	-	EXTRAM	AO	00H[%]
AUXR1#	Auxiliary Function Register 1	A2H	-	-	-	LPEP	GF2	0	-	DPS	00H[%]
			F7	F6	F5	F4	F3	F2	F1	F0	
B*	B Register	F0H									00H
BRGR0#§	Baud Rate Generator Rate Low	86H[‡]	BRATE11	BRATE10	BRATE9	BRATE8	BRATE7	BRATE6	BRATE5	BRATE4	00H
BRGR1#§	Baud Rate Generator Rate High	87H[‡]	BRATE3	BRATE2	BRATE1	BRATE0	-	-	-	-	00H[%]
BRGCON#	Baud Rate Generator Control	85H[‡]	-	-	-	-	-	-	S0BRGS	BRGEN	00H[%]
CCAP0H#	Module 0 Capture High	FAH									XXH
CCAP1H#	Module 1 Capture High	FBH									XXH
CCAP2H#	Module 2 Capture High	FCH									XXH
CCAP3H#	Module 3 Capture High	FDH									XXH
CCAP4H#	Module 4 Capture High	FEH									XXH
CCAP0L#	Module 0 Capture Low	EAH									XXH
CCAP1L#	Module 1 Capture Low	EBH									XXH
CCAP2L#	Module 2 Capture Low	ECH									XXH
CCAP3L#	Module 3 Capture Low	EDH									XXH
CCAP4L#	Module 4 Capture Low	EEH									XXH
CCAPM0#	Module 0 Mode	DAH	-	ECOM_0	CAPP_0	CAPN_0	MAT_0	TOG_0	PWM_0	ECCF_0	00H[%]
CCAPM1#	Module 1 Mode	DBH	-	ECOM_1	CAPP_1	CAPN_1	MAT_1	TOG_1	PWM_1	ECCF_1	00H[%]
CCAPM2#	Module 2 Mode	DCH	-	ECOM_2	CAPP_2	CAPN_2	MAT_2	TOG_2	PWM_2	ECCF_2	00H[%]
CCAPM3#	Module 3 Mode	DDH	-	ECOM_3	CAPP_3	CAPN_3	MAT_3	TOG_3	PWM_3	ECCF_3	00H[%]
CCAPM4#	Module 4 Mode	DEH	-	ECOM_4	CAPP_4	CAPN_4	MAT_4	TOG_4	PWM_4	ECCF_4	00H[%]

Special Function Registers (Continued)

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATE PORT FUNCTION MSB							LSB	Reset Value
			DF	DE	DD	DC	DB	DA	D9	D8	
CCON#	PCA Counter Control	D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	00H%
CH#	PCA Counter High	F9H									00H
CL#	PCA Counter Low	E9H									00H
CMOD#	PCA Counter Mode	D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00H%
DPTR	Data Pointer (2 bytes)										00H
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
EPL#	Extended Data Pointer Low	FCH‡									00H
EPM#	Extended Data Pointer Middle	FDH‡									00H
EPH#	Extended Data Pointer High	FEH‡									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IEN0*	Interrupt Enable 0	A8H	EA	EC	ET2	ES0/ ES0R	ET1	EX1	ET0	EX0	00H
			EF	EE	ED	EC	EB	EA	E9	E8	
IEN1*	Interrupt Enable 1	E8H	-	-	-	-	ESPI	ES1T	ES0T	ES1/ ES1R	00H%
			BF	BE	BD	BC	BB	BA	B9	B8	
IP0*	Interrupt Priority	B8H	-	PPC	PT2	PS0/ PS0R	PT1	PX1	PT0	PX0	00H
IP0H	Interrupt Priority 0 High	B7H	-	PPCH	PT2H	PS0H/ PS0RH	PT1H	PX1H	PT0H	PX0H	00H
			FF	FE	FD	FC	FB	FA	F9	F8	
IP1*	Interrupt Priority 1	F8H	-	-	-	-	PSPI	PS1T	PS0T	PS1/ PS1R	00H%
IP1H	Interrupt Priority 1 High	F7H	-	-	-	-	PSPIH	PS1TH	PS0TH	PS1H/ PS1RH	00H%
MXCON#	MX Control Register	FFH‡	-	-	-	-	-	EAM	ESMM	EIFM	00H%
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	CEX4	CEX3	CEX2/ SPICLK	CEX1/ MOSI	CEX0	ECI	T2EX	T2	FFH

Special Function Registers (Continued)

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATE PORT FUNCTION MSB							LSB	Reset Value
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	AD15	AD14/ AD22	ADA13/ AD21	AD12/AD20	AD11/ AD19	AD10/ AD18	AD9/ AD17	AD8/ AD16	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD0	RxD0	FFH
			C7‡	C6‡	C5‡	C4‡	C3‡	C2‡	C1‡	C0‡	
P4*#	Port 4	C0H‡	-	-	-	-	-	-	TxD1/$\overline{SS}$	RxD1/ MISO	FFH
PCON#	Power Control Register	87H	SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL	00H/10H&
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H
RCAP2H#	Timer2 Capture High	CBH									00H
RCAP2L#	Timer2 Capture Low	CAH									00H
			9F	9E	9D	9C	9B	9A	99	98	
S0CON*	Serial Port 0 Control	98H	SM0_0/ FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00H
S0BUF	Serial Port 0 Data Buffer Register	99H									xxH
S0ADDR	Serial Port 0 Address Register	A9H									00H
S0ADEN	Serial Port 0 Address Enable	B9H									00H
S0STAT#	Serial Port 0 Status	8CH‡	DBMOD_ 0	INTLO_0	CIDIS_0	DBISEL_0	FE_0	BR_0	OE_0	STINT_0	00H%
			87‡	86‡	85‡	84‡	83‡	82‡	81‡	80‡	
S1CON#*	Serial Port 1 Control	80H‡	SM0_1/ FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00H
S1BUF#	Serial Port 1 Data buffer Register	81H‡									XXH
S1ADDR#	Serial Port 1 Address Register	82H‡									00H
S1ADEN#	Serial Port 1 Address Enable	83H‡									00H
S1STAT#	Serial Port 1 Status	84H‡	DBMOD_ 1	INTLO_1	CIDIS_1	DBISEL1	FE_1	BR_1	OE_1	STINT_1	00H%
SP	Stack Pointer (or Stack Pointer Low Byte When EDATA Supported)	81H									08H
SPCTL#	SPI Control Register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	-	-	00H%
SPCFG#	SPI Configuration Register	E1H	SPIF	SPWCOL	-	-	PSC3	PSC2	PSC1	PSC0	00H%
SPDAT#	SPI Data	E3H									00H
SPE#	Stack Pointer High	FBH‡									00H

Special Function Registers (Continued)

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATE PORT FUNCTION MSB							LSB	Reset Value
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control Register	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON#*	Timer2 Control Register	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	00H
T2MOD#	Timer2 Mode Control	C9H	-	-	-	-	-	-	T2OE	DCEN	00H%
TH0	Timer 0 High	8CH									00H
TH1	Timer 1 High	8DH									00H
TH2	Timer 2 High	CDH									00H
TL0	Timer 0 Low	8AH									00H
TL1	Timer 1 Low	8BH									00H
TL2	Timer 2 Low	CCH									00H
TMOD	Timer 0 and 1 Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
WDTRST#	Watchdog Timer Reset	A6H									FFH
WDCON#	Watchdog Timer Control	8FH‡	-	-	-	-	-	WDPRE2	WDPRE1	WDPRE0	00H%

Notes:
* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
‡ Extended SFRs accessed by preceeding the instruction with 51MX escape (opcode A5h).
\- Reserved bits, must be written with 0's.
& Power on reset is 10H. Other reset is 00H.
§ BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is '0'. If any of them is written if BRGEN = 1, result is unpredictable.
% The unimplemented bits (labeled '-') in the SFRs are 'X's (unknown) at all times. '1's should NOT be written to these bits, as they may be used for other purposes in future derivatives. The reset values shown for these bits are '0's although they are unknown when read.

FUNCTIONAL DESCRIPTION

The following paragraphs briefly describe the features of the P87C51Mx2. For more detailed information, please refer to the P87C51Mx2 User Manual or the 51MX Architecture Reference.

INTERRUPTS

Table 1 summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, polling priority, and whether each interrupt may wake up the CPU from Power Down mode.

Description	Interrupt Flag Bit(s)	Vector Address	Interrupt Enable Bit(s)	Interrupt Priority	Polling Priority	Power Down Wakeup
External Interrupt 0	IE0	0003h	EX0 (IEN0.0)	IP0H.0, IP0.0	1 (highest)	Yes
Timer 0 Interrupt	TF0	000Bh	ET0 (IEN0.1)	IP0H.1, IP0.1	2	No
External Interrupt 1	IE1	0013h	EX1 (IEN0.2)	IP0H.2, IP0.2	3	Yes
Timer 1 Interrupt	TF1	001Bh	ET1 (IEN0.3)	IP0H.3, IP0.3	4	No
Serial Port 0 Tx and Rx[1,5]	TI_0 & RI_0[5]	0023h	ES0(IEN0.4)	IP0H.4, IP0.4	6	No
Serial Port 0 Rx[1,5]	RI_0[5]					
Timer 2 Interrupt	TF2, EXF2	002Bh	ET2 (IEN0.5)	IP0H.5, IP0.5	7	No
PCA interrupt	CF, CCFn*	0033h	EC (IEN0.6)	IP0H.6, IP0.6	5	No
Serial Port 1 Tx and Rx[2,6]	TI_1 & RI_1[6]	0053h	ES1 (IEN1.0)	IP1H.0, IP1.0	11	No
Serial Port 1 Rx[2,6]	RI_1[6]					
Serial Port 0 Tx[3]	TI_0	003Bh	EI10 (IEN1.1)	IP1H.1, IP1.1	8	No
Serial Port 1 Tx[4]	TI_1	0043h	EI11 (IEN1.2)	IP1H.2, IP1.2	9	No
SPI Interrupt	SPI	004Bh	EI11 (IEN1.3)	IP1H.3, IP1.3	10	No
Reserved		005Bh	EI12 (IEN1.4)	IP1H.4, IP1.4	12	No
		0063h	EI13 (IEN1.5)	IP1H.5, IP1.5	13	No
		006Bh	EI13 (IEN1.6)	IP1H.6, IP1.6	14	No
		0073h	EI14 (IEN1.7)	IP1H.7, IP1.7	15 (lowest)	No

1. S0STAT.5 = 0 selects combined Serial Port 0 Tx and Rx interrupt; S0STAT.5 = 1 selects Serial Port 0 Rx interrupt only (and TX interrupt will be different, see Note 3 below).
2. S1STAT.5 = 0 selects combined Serial Port 1 Tx and Rx interrupt; S1STAT.5 = 1 selects Serial Port 1 Rx interrupt only (and TX interrupt will be different, see Note 4 below).
3. This interrupt is used as Serial Port 0 Tx interrupt if and only if S0STAT.5 = 1, and is disabled otherwise.
4. This interrupt is used as Serial Port 1 Tx interrupt if and only if S1STAT.5 = 1, and is disabled otherwise.
5. If S0STAT.0 = 1, the following Serial Port 0 additional flag bits can cause this interrupt: FE_0, BR_0, OE_0.
6. If S1STAT.0 = 1, the following Serial Port 1 additional flag bits can cause this interrupt: FE_1, BR_1, OE_1.

Table 1: Summary of Interrupts

DATA RAM

The P87C51MB2 and P87C51MC2 have 2 Kbytes and 3 K bytes of on-chip RAM respectively. Usages of the different data segments are described in the 51MX Architecture Reference.

Data Memory		Size (in Bytes)	
Type	Description	P87C51MB2	P87C51MC2
DATA	memory that can be addressed directly and indirectly	128	128
IDATA	memory that can be addressed indirectly (where direct address is for SFR only)	128	128
EDATA	memory that can only be addressed indirectly	1024	1024
XDATA	memory (on-chip "External Data") that is accessed using the MOVX instructions	768	1792
	Total	2048	3072

Table 2: On-Chip Data Memory Usage.

PORT 4

The P87C51Mx2 has a fifth I/O port (Port 4) that is shared with the second UART pins (RXD1 and TXD1) and two of the SPI pins (MISO and $\overline{SS}$). This port is also bit addressable and can be accessed in the same manner as any other ports, except that the associated SFR is in the extended SFR space. Accesses to this SFR space is the same as those to the conventional SFR space except that the instructions must be preceeded by an escape code (A5h), as described in the 51MX Architecture Reference.

LOW POWER MODES

The P87C51Mx2 supports the standard 51MX low power modes - Stop Clock Mode, Idle Mode and Power-Down Mode.

The PCON register is the same as the standard 51MX PCON register. Note that bits PCON.7 and PCON.6 are for UART configurations (see section "UARTs").

ONCE™ MODE

The ONCE (“On-Circuit Emulation”) Mode facilitates testing and debugging of systems without the device having to be removed from the circuit. It is supported in the P87C51Mx2.

PERIPHERALS

The P87C51Mx2 peripherals are described in more detail in the User Manual. The on-chip peripherals include:

- Timers:
  - Timers 0 and 1.
  - Timer 2.

  Note: When Timer 1 or Timer 2 can only be used as a baud rate generator for UART 0, but not for UART 1.
- Two enhanced UARTs with an independent Baud Rate Generator - The section "UARTs" provides information regarding the two UARTs.

  Note: UART 1 shares the RXD1 and TXD1 with the SPI pins. The SPEN (SPCTL.6) bit must be cleared ’0’ (reset value) to enable UART 1 operation.
- Serial Peripheral Interface (SPI). **Note:** The SPI shares pins with the UART 1 shares the RXD1 and TXD1 with the SPI pins. The SPEN (SPCTL.6) bit must be set to ’1’ to enable SPI operation.
- Watchdog Timer.
- Programmable Counter Array (PCA).

UARTS

P87C51Mx2 includes two enhanced UART ports with one independent Baud Rate Generator:

- UART 0 is the standard 51MX enhanced UART as described in the User Manual. It can be selected to use Timer1 overflow, Timer2 overflow or the independent Baud Rate Generator.
- UART 1 only uses the independent Baud Rate Generator to generate its baud rate. It has the same baud rate for both transmission and reception.
- The Baud Rate Generator is described in the User Manual.

Each of the UARTs has one set of enhanced UART SFRs. Please refer to the descriptions on the corresponding SFRs in the User Manual:

Register	Description	SFR Location	51MX Extended SFR Location	See Description in User Manual on
S0CON	Serial Port 0 Control	98H		SCON
S0BUF	Serial Port 0 Data Buffer	99H		SBUF
S0ADDR	Serial Port 0 Address	A9H		SADDR
S0ADEN	Serial Port 0 Address Enable	B9H		SADEN
S0STAT	Serial Port 0 Status		8CH	SSTAT
S1CON	Serial Port 1 Control		80H	SCON
S1BUF	Serial Port 1 Data Buffer		81H	SBUF
S1ADDR	Serial Port 1 Address		82H	SADDR
S1ADEN	Serial Port 1 Address Enable		83H	SADEN
S1STAT	Serial Port 1 Status		84H	SSTAT

Table 3: UARTs 0 and 1 SFRs.

PCON.7 and PCON.6 SFR Bits

The PCON.7 and PCON.6 SFR bits configure the UARTs as follows:

- PCON.7 (SMOD1) - Baud Rate Control bit for serial port 0. When 0, the baud rate for UART 0 will be the input rate (T1 timer or baud rate generator, as determined by the BRGCON extended SFR) divided by two. When 1, the baud rate for UART 0 will be the input rate (T1 timer or baud rate generator). UART 1 is not affected by this bit
- PCON.6 (SMOD0) - Framing Error Location:
  - When 0, bit 7 of S0CON and S1CON will function as SM0 for UARTs 0 and 1 respectively.
  - When 1, bit 7 of S0CON and S1CON will be used for framing error status for UART 0 and 1 respectively.

  PCON.6 also determines when the UART receive interrupts RI_0 and RI_1 occur in UART modes 2 or 3. (Refer to User Manual for details.)

Baud Rate Selection

UART 0 and UART 1 selects the baud rate differently as shown in Tables 4 and 5:

S0CON.7 (SM0_0)	S0CON.6 (SM1_0)	T2CON.5/4 (RCLK - Receive TCLK - Transmit)	PCON.7 (SMOD1)	BRGCON.1 (S0BRGS)	Receive/Transmit Baud Rate for UART 0
0	0	X	X	X	$f_{OSC}/6$
0	1	0	0	X	T1_rate/32*
		0	1	X	T1_rate/16*
		1	X	0	T2_rate/16*
		1	X	1	$f_{OSC}/(BRATE \times 16+16)$*
1	0	X	0	X	$f_{OSC}/32$
		X	1	X	$f_{OSC}/16$
1	1	0	0	X	T1_rate/32*
		0	1	X	T1_rate/16*
		1	X	0	T2_rate/16*
		1	X	1	$f_{OSC}/(BRATE \times 16+16)$*

* UART 0 can have different receive and transmit baud rates.

Table 4: Baud Rate Generation for UART 0. Use T2CON.5 (RCLK) in Receive Baud Rate Selection, T2CON.4 (TCLK) in Transmit Baud Rate Selection

S1CON.7 (SM0_1)	S1CON.6 (SM1_1)	Baud Rate for UART 1
0	0	$f_{OSC}/6$
0	1	$f_{OSC}/(BRATE \times 16+16)$*
1	0	$f_{OSC}/(BRATE \times 16+16)$*
1	1	$f_{OSC}/(BRATE \times 16+16)$*

* UART 1 has the same receive and transmit baud rate.

Table 5: Baud Rate Generation for UART 1.

SECURITY BITS

The P87C51Mx2 has security bits to protect users' firmware codes. With none of the security bits programmed, the code in the program memory can be verified. With only security bit 1 (see Table 6) is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the internal memory. EA is latched on Reset and all further programming of EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security bits are programmed, all of the conditions above apply and all external program memory execution is disabled.

Security Bits[1,2]				
	Bit 1	**Bit 2**	**Bit 3**	**Protection Description**
1	U	U	U	No program security features enabled. EEPROM is programmable and verifiable.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verification is disabled.
4	P	P	P	Same as 3, external execution is disabled.

Notes:
1. P - programmed. U- unprogrammed.
2. Any other combination of security bits is not defined.

Table 6: EPROM Security Bits

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature under bias	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}	0 to + 13.0	V
Voltage on any other pin to V_{SS}	-0.5 to V_{DD}+0.5V	V
Maximum I_{OL} per I/O pin	20	mA
Power dissipation (based on package heat transfer, not device power consumption)	1.5	W

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification are not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7V to 5.5V unless otherwise specified;
T_{amb} = 0 to +70°C for commercial, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
V_{IL}	Input low voltage		-0.5		$0.2V_{DD}$-0.1	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, 4, $\overline{EA}$)		$0.2V_{DD}$+0.9		V_{DD}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{DD}$		V_{DD}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, 3, 4[8]	V_{DD} = 2.7V, I_{OL} = 1.6mA			0.4	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$[7,8]	V_{DD} = 2.7V, I_{OL} = 3.2mA			0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3, 4	V_{DD} = 4.5V, I_{OH} = -30µA V_{DD} = 2.7V, I_{OH} = -10µA	V_{DD} - 0.7			V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE[9], $\overline{PSEN}$[3]	V_{DD} = 2.7V, I_{OH} = -3.2mA	V_{DD} - 0.7			V
I_{IL}	Logical 0 input current, ports 1, 2, 3, 4	V_{IN} = 0.4V	-1		-75	µA
I_{TL}	Logical 1 -to-0 transition current, ports 1, 2, 3, 4[8]	4.5V < V_{DD} < 5.5V, V_{IN} = 2.0V, See Note 4			-650	µA
I_{L1}	Input leakage current, port 0	0.45 < V_{IN} < V_{DD}-0.3			±10	µA
I_{CC}	Power supply current					
	Active mode (see Note 5)	V_{DD} = 5.5V V_{DD} = 3.6V			7 + 2.7 /MHz × f_{OSC} 4 + 1.3 /MHz × f_{OSC}	mA
	Idle mode (see Note 5)	V_{DD} = 5.5V V_{DD} = 3.6V			4 + 1.3 /MHz × f_{OSC} 1 + 1.0 /MHz × f_{OSC}	mA
	Power-down mode or clock stopped (see Figure 16 for conditions)	V_{DD} = 5.0V V_{DD} = 5.5V		20	 100	µA µA
R_{RST}	Internal reset pull-down resistor		40		225	kΩ
C_{10}	Pin capacitance[10] (except $\overline{EA}$)				15	pF

Notes:
1. Typical ratings are not guaranteed. The values listed are at room temperature (+25°C), 5V, unless otherwise stated.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} of ALE and ports 1, 3 and 4. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading>100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the V_{DD}-0.7V specification when the address bits are stabilizing.
4. Pins of ports 1, 2, 3 and 4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V for 4.5V < V_{DD} < 5.5V.
5. See Figures 13 through 16 for I_{CC} test conditions. f_{OSC} is the oscillator frequency in MHz.
6. This value applies to T_{amb} = 0°C to +70°C.

7. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80pF
8. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15 mA
   Maximum I_{OL} per 8-bit port: 26 mA
   Maximum total I_{OL} for all outputs: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
9. ALE is tested to V_{OH1}, except when ALE is off then V_{OH} is the voltage specification.
10. Pin capacitance is characterized but not tested.

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0 to +70°C for commercial unless otherwise specified.[1,2,3]

SYMBOL	FIGURE(S)	PARAMETER	2.7V < VDD < 5.5V				4.5V < VDD < 5.5V				UNIT
			Variable Clock[4]		f_{OSC}=12MHz[4]		Variable Clock[4]		f_{OSC}=24MHz[4]		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{OSC}		Oscillator frequency	0	12			0	24			MHz
t_{CLCL}	15	CLock cycle			83				41.5		ns
t_{LHLL}	1,2	ALE pulse width	t_{CLCL}-66		16		t_{CLCL}-33		8		ns
t_{AVLL}	1,2,3, 4,5,6	Address valid to ALE low	t_{CHCX}-25		8		t_{CHCX}-12		4		ns
t_{LLAX}	1,2,3, 4,5,6	Address hold after ALE low	t_{CLCX}-25		8		t_{CLCX}-12		4		ns
t_{LLIV}	1,2	ALE low to valid instruction in		$2t_{CLCL}$-108		58		$2t_{CLCL}$-54		29	ns
t_{LLPL}	1,2	ALE low to $\overline{PSEN}$ low	t_{CLCX}-25		8		t_{CLCX}-12		4		ns
t_{PLPH}	1,2	$\overline{PSEN}$ pulse width	$t_{CLCL}+t_{CHCX}$ -66		50		$t_{CLCL}+t_{CHCX}$ -33		25		ns
t_{PLIV}	1,2	$\overline{PSEN}$ low to valid instruction in		t_{CLCL} $+t_{CHCX}$-91		25		t_{CLCL} $+t_{CHCX}$-46		12	ns
t_{PXIX}	1,2	Input instruction hold after $\overline{PSEN}$	0		0		0		0		ns
t_{PXIZ}	1,2	Input instruction float after $\overline{PSEN}$		t_{CLCX}-25		8		t_{CLCX}-12		4	ns
t_{AVIV}	1	Address (A8-A15) to valid instruction in (non-Extended Addressing Mode)		$2t_{CLCL}$ $+t_{CHCX}$-36		180		$2t_{CLCL}$ $+t_{CHCX}$-28		81	ns
t_{AVIV1}	2	Address (A8-A15) to valid instruction in (Extended Addressing Mode)		t_{CLCL} $+t_{CHCX}$-44		89		$2t_{CLCL}$ $+t_{CHCX}$-34		33	ns
t_{PLAZ}	1,2	$\overline{PSEN}$ low to address float		16		16		8		8	ns
Data Memory											
t_{RLRH}	3,4	$\overline{RD}$ pulse width	$3t_{CLCL}$-166		83		$3t_{CLCL}$-83		41.5		ns
t_{WLWH}	5,6	$\overline{WR}$ pulse width	$3t_{CLCL}$-166		83		$3t_{CLCL}$-83		41.5		ns
t_{RLDV}	3,4	$\overline{RD}$ low to valid data in		$2t_{CLCL}$ $+t_{CHCX}$-141		58		$2t_{CLCL}$ $+t_{CHCX}$-70		29	ns
t_{RHDX}	3,4	Data hold after $\overline{RD}$	0		0		0		0		ns
t_{RHDZ}	3,4	Data float after $\overline{RD}$		t_{CLCL}-34		49		t_{CLCL}-17		24	ns
t_{LLDV}	3,4	ALE low to valid data in		$4t_{CLCL}$-250		83		$4t_{CLCL}$-125		41	ns
t_{AVDV}	3	Address (A8-A15) to valid data in (non-Extended Addressing Mode)		$4t_{CLCL}$ $+t_{CHCX}$-36		346		$4t_{CLCL}$ $+t_{CHCX}$-28		164	ns
t_{AVDV1}	4	Address (A8-A15) to valid data in (Extended Addressing Mode)		$3t_{CLCL}$ $+t_{CHCX}$-44		255		$3t_{CLCL}$ $+t_{CHCX}$-34		116	ns
t_{LLWL}	3,4, 5,6	ALE low to $\overline{RD}$ or $\overline{WR}$ low	t_{CLCL} $+t_{CLCX}$-83	t_{CLCL} $+t_{CLCX}$+83		208	t_{CLCL} $+t_{CLCX}$-41	t_{CLCL} $+t_{CLCX}$+41		104	ns
t_{AVWL}	3,5	Address (A8-A15) valid to $\overline{WR}$ or $\overline{RD}$ low (non-Extended Addressing Mode)	$2t_{CLCL}$-15		151		$2t_{CLCL}$-20		63		ns
t_{AVWL1}	4,6	Address (A8-A15) valid to $\overline{WR}$ or $\overline{RD}$ low (Extended Addressing Mode)	t_{CLCL}-20		63		t_{CLCL}-25		16.5		ns
t_{QVWX}	5,6	Data valid to $\overline{WR}$ transition	t_{CLCX}-33		0		t_{CLCX}-16		0		ns
t_{WHQX}	5,6	Data hold after $\overline{WR}$	t_{CHCX}-24		9		t_{CHCX}-11		5		ns
t_{QVWH}	5,6	Data valid to $\overline{WR}$ high	$3t_{CLCL}$ $+t_{CLCX}$-207		75		$3t_{CLCL}$ $+t_{CLCX}$-103		37.5		ns
t_{RLAZ}	3,4	$\overline{RD}$ low to address float		0		0		0		0	ns
t_{WHLH}	3,4, 5,6	$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{CHCX}-24	t_{CHCX}+25	9	75	t_{CHCX}-11	t_{CHCX}+12	5	37	ns
External Clock											
t_{CHCX}	12	High time	33	t_{CLCL}-t_{CLCX}	33	50	16	t_{CLCL}-t_{CLCX}	16	24.5	ns
t_{CLCX}	12	Low time	33	t_{CLCL}-t_{CHCX}	33	50	16	t_{CLCL}-t_{CHCX}	16	24.5	ns
t_{CLCH}	12	Rise time		8		8		4		4	ns
t_{CHCL}	12	Fall Time		8		8		4		4	ns

SYMBOL	FIGURE(S)	PARAMETER	2.7V < VDD < 5.5V				4.5V < VDD < 5.5V				UNIT
			Variable Clock[4]		f_{OSC}=12MHz[4]		Variable Clock[4]		f_{OSC}=24MHz[4]		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Shift Register											
t_{XLXL}	7	Serial port clock cycle time	$6t_{CLCL}$		500		$6t_{CLCL}$		250		ns
t_{QVXH}	7	Output data setup to clock rising edge	$5t_{CLCL}$-221		195		$5t_{CLCL}$-110		98		ns
t_{XHQX}	7	Output data hold after clock rising edge	t_{CLCL}-50		34		t_{CLCL}-25		17		ns
t_{XHDX}	7	Input data hold after clock rising edge	0		0		0		0		ns
t_{XHDV}	7	Clock rising edge to input data valid		$5t_{CLCL}$-222		195		$5t_{CLCL}$-111		97	ns
SPI Interface											
f_{SPI}		Operating frequency - 3.0MHz - 6.0MHz	0 -	3.0 -	0 -	3.0 -	0 0	3.0 6.0	0 0	3.0 6.0	MHz
t_{SPICYC}	8, 9, 10, 11	Cycle time - 3.0MHz - 6.0MHz	333 -		333 -		333 166		333 166		ns
$t_{SPILEAD}$	10, 11	Enable lead time (Slave) - 3.0MHz - 6.0MHz	TBD -		TBD -		TBD TBD		TBD TBD		ns
t_{SPILAG}	10, 11	Enable lag time (Slave) - 3.0MHz - 6.0MHz	TBD -		TBD -		TBD TBD		TBD TBD		ns
$t_{SPICLKH}$	8, 9, 10, 11	SPICLK high time - Master - Slave	TBD TBD		TBD TBD		TBD TBD		TBD TBD		ns
$t_{SPICLKL}$	8, 9, 10, 11	SPICLK low time - Master - Slave	TBD TBD		TBD TBD		TBD TBD		TBD TBD		ns
t_{SPIDSU}	8, 9, 10, 11	Data setup time (Master or Slave)	TBD		TBD		TBD		TBD		ns
t_{SPIDH}	8, 9, 10, 11	Data hold time (Master or Slave)	TBD		TBD		TBD		TBD		ns
t_{SPIA}	10, 11	Access time (Slave)		TBD		TBD		TBD		TBD	ns
t_{SPIDIS}	10, 11	Disable time (Slave) - 3.0MHz - 6.0MHz		TBD TBD		TBD TBD		TBD TBD		TBD TBD	ns
t_{SPIDV}	8, 9, 10, 11	Enable to output data valid - 3.0MHz - 6.0MHz		TBD -		TBD -		TBD TBD		TBD TBD	ns
t_{SPIOH}	8, 9, 10, 11	Output data hold time	0		0		0		0		ns
t_{SPIR}	8, 9, 10, 11	Rise time - SPI outputs (SPICLK,MOSI, MISO) - SPI inputs (SPICLK,MOSI, MISO, $\overline{SS}$)		TBD TBD		TBD TBD		TBD TBD		TBD TBD	ns
t_{SPIF}	8, 9, 10, 11	Fall time - SPI outputs (SPICLK,MOSI, MISO) - SPI inputs (SPICLK,MOSI, MISO, $\overline{SS}$)		TBD TBD		TBD TBD		TBD TBD		TBD TBD	ns

Notes:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. Interfacing the microcontroller to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
4. Parts are tested down to 2 MHz, but are guaranteed to operate down to 0Hz.

EXPLANATION OF AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address

C – Clock

D – Input data

H – Logic level high

I – Instruction (program memory contents)

L – Logic level low, or ALE

P – PSEN

Q – Output data

R – RD signal

t – Time

V – Valid

W– WR signal

X – No longer a valid logic level

Z – Float

Examples:

t_{AVLL} - Time for address valid to ALE low.

t_{LLPL} - Time for ALE low to PSEN low

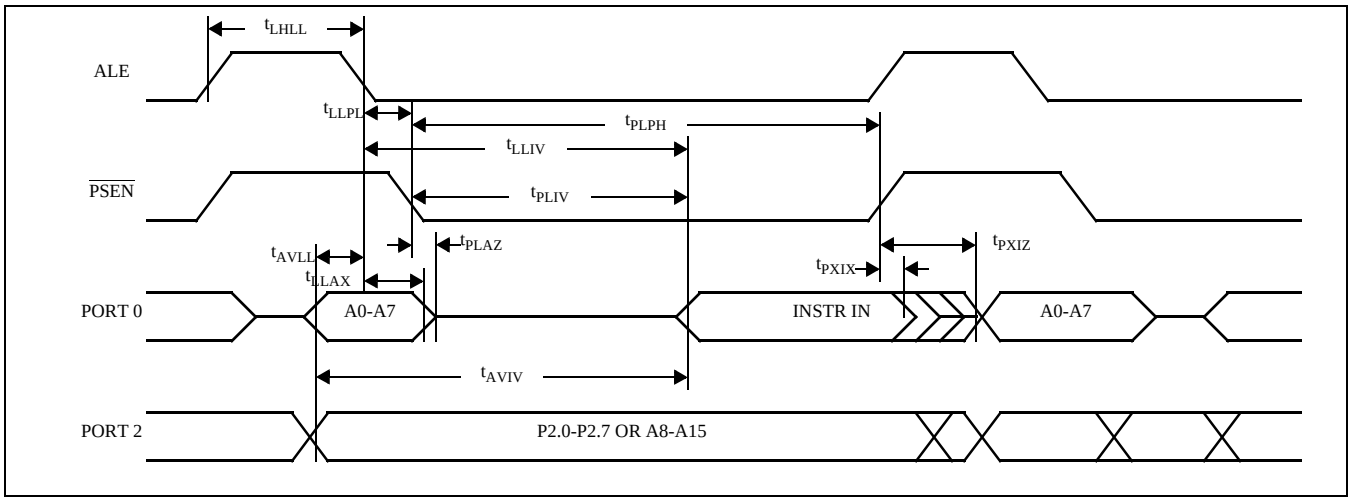


Figure 1: External Program Memory Read Cycle (Non-Extended Memory Cycle)

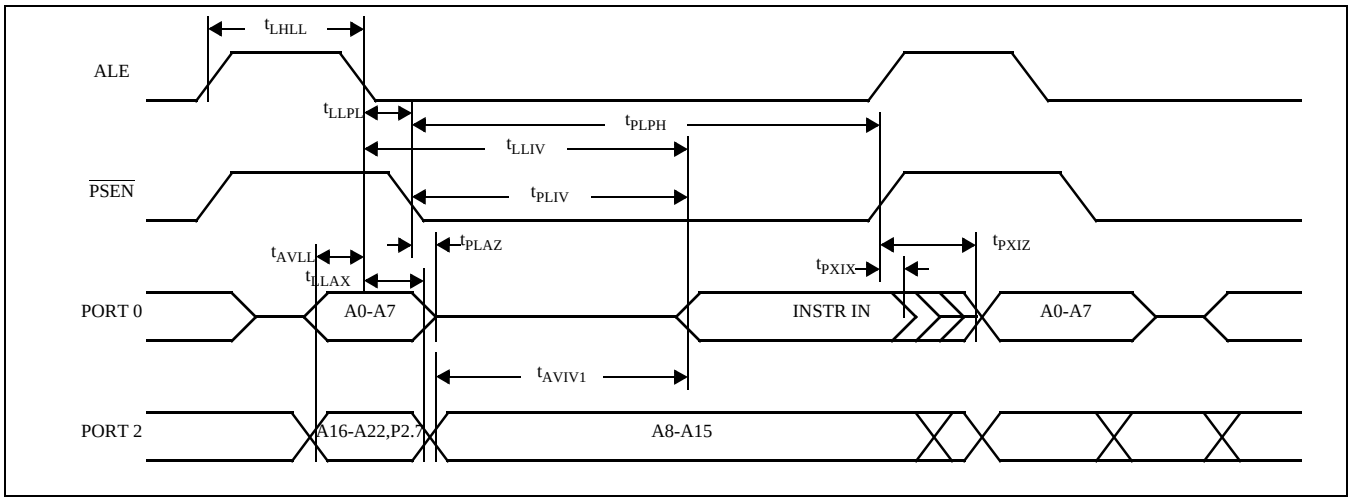


Figure 2: External Program Memory Read Cycle (Extended Memory Cycle)

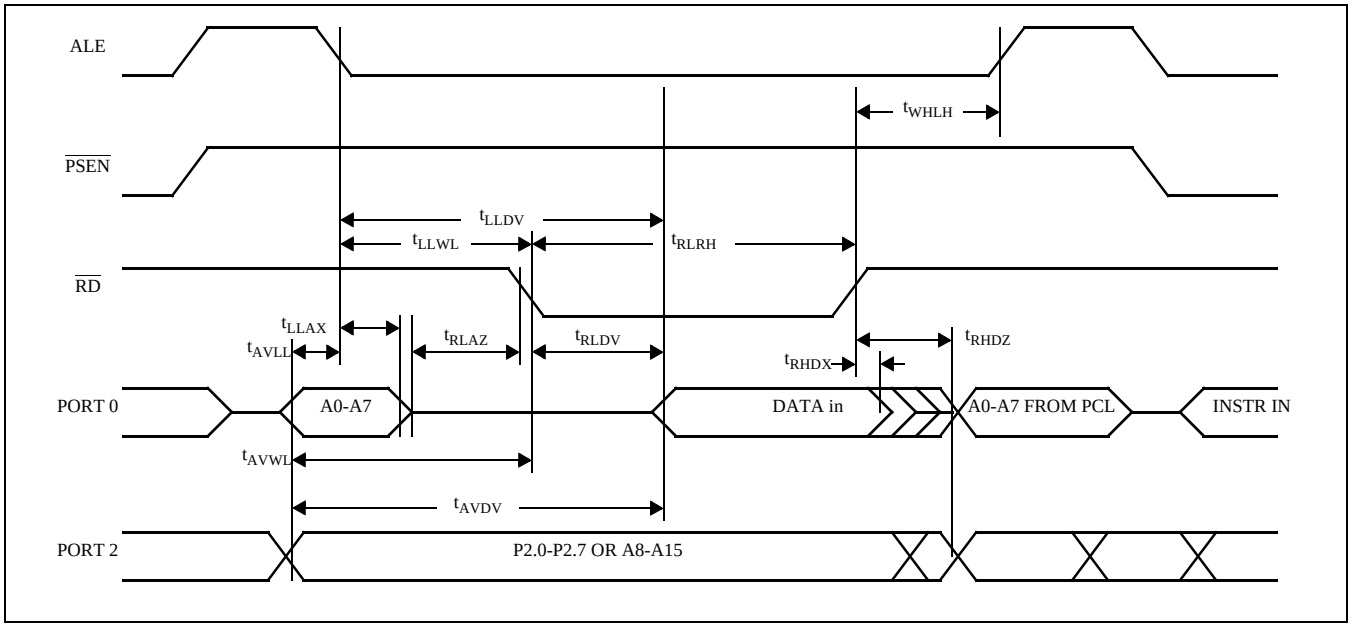


Figure 3: External Data Memory Read Cycle (Non-Extended Memory Cycle)

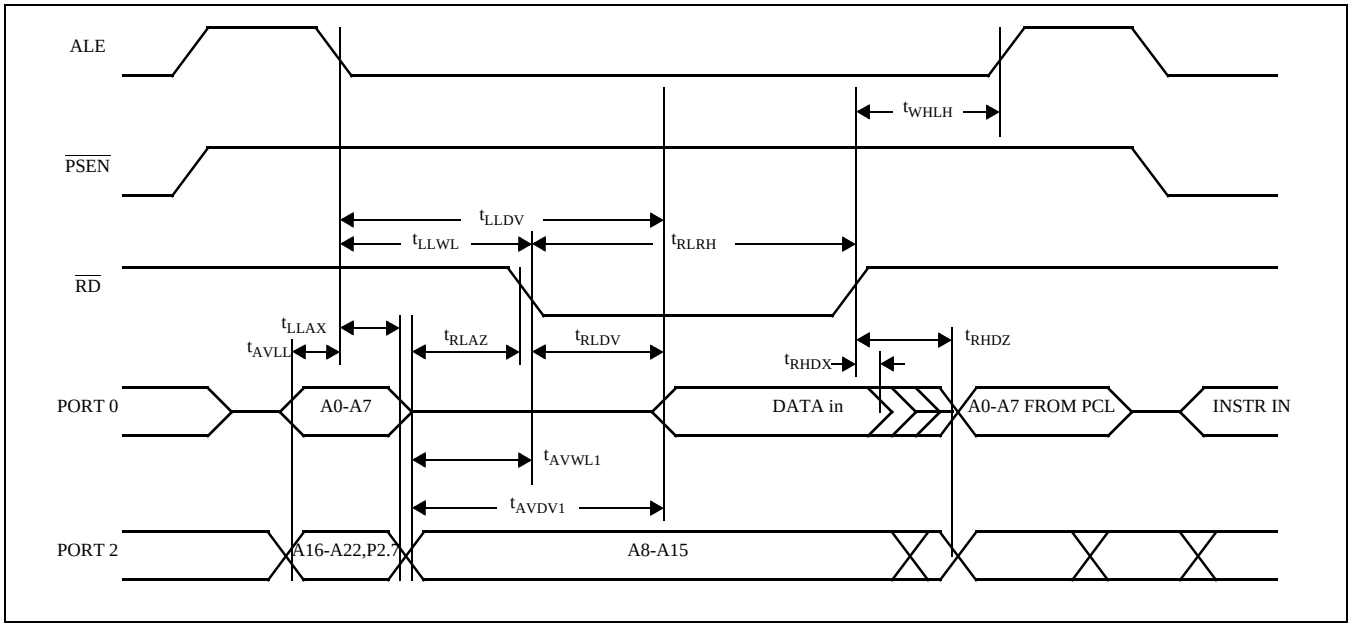


Figure 4: External Data Memory Read Cycle (Extended Memory Cycle)

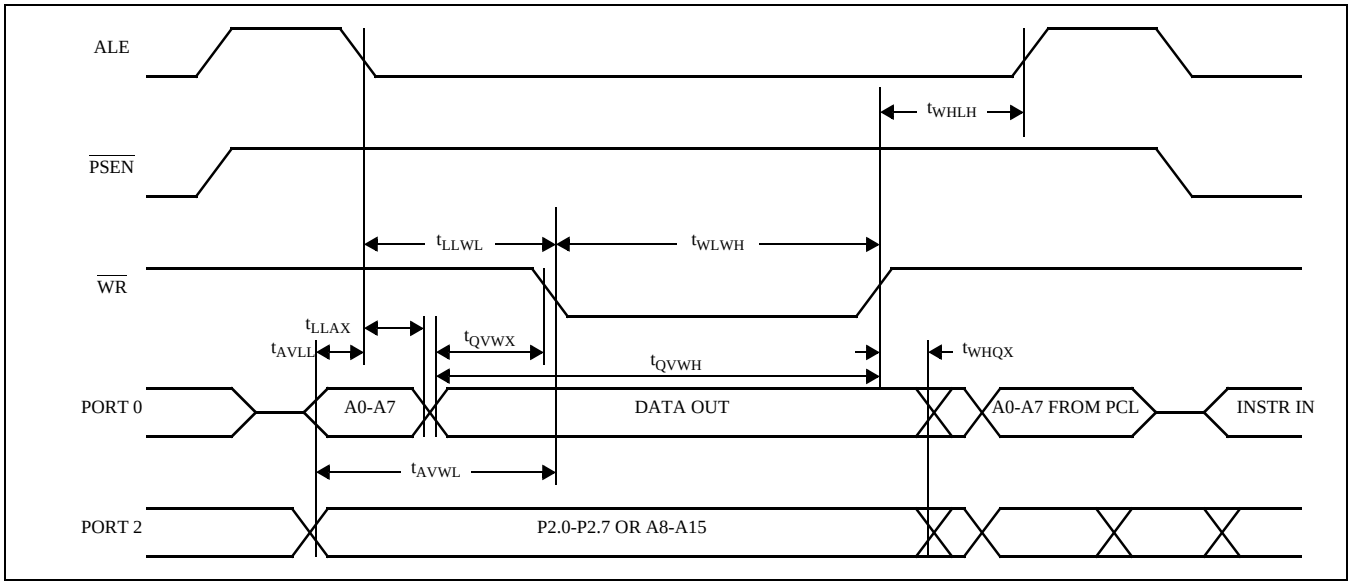


Figure 5: External Data Memory Write Cycle (Non-Extended Memory Cycle)

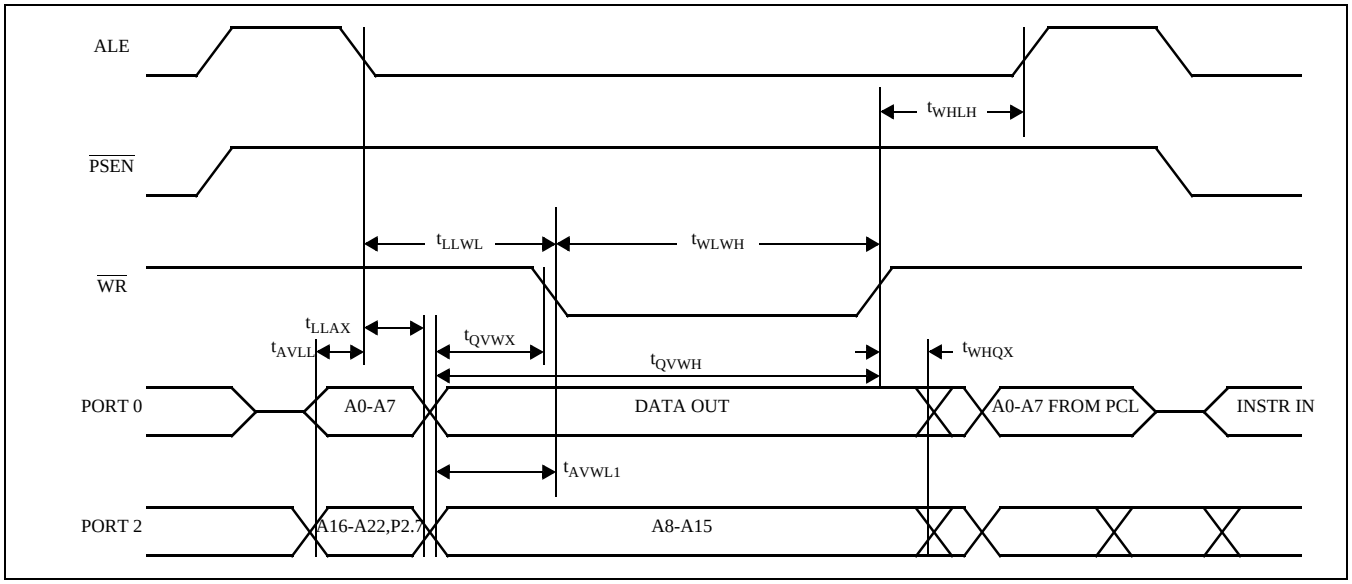


Figure 6: External Data Memory Write Cycle (Extended Memory Cycle)

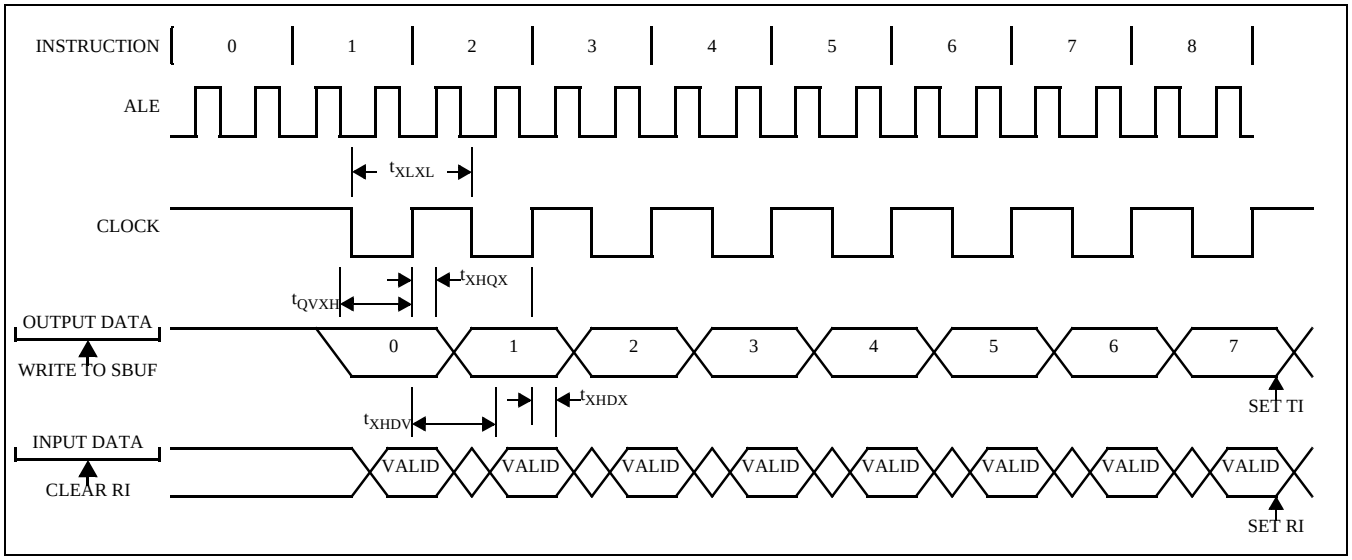


Figure 7: Shift Register Mode Timing

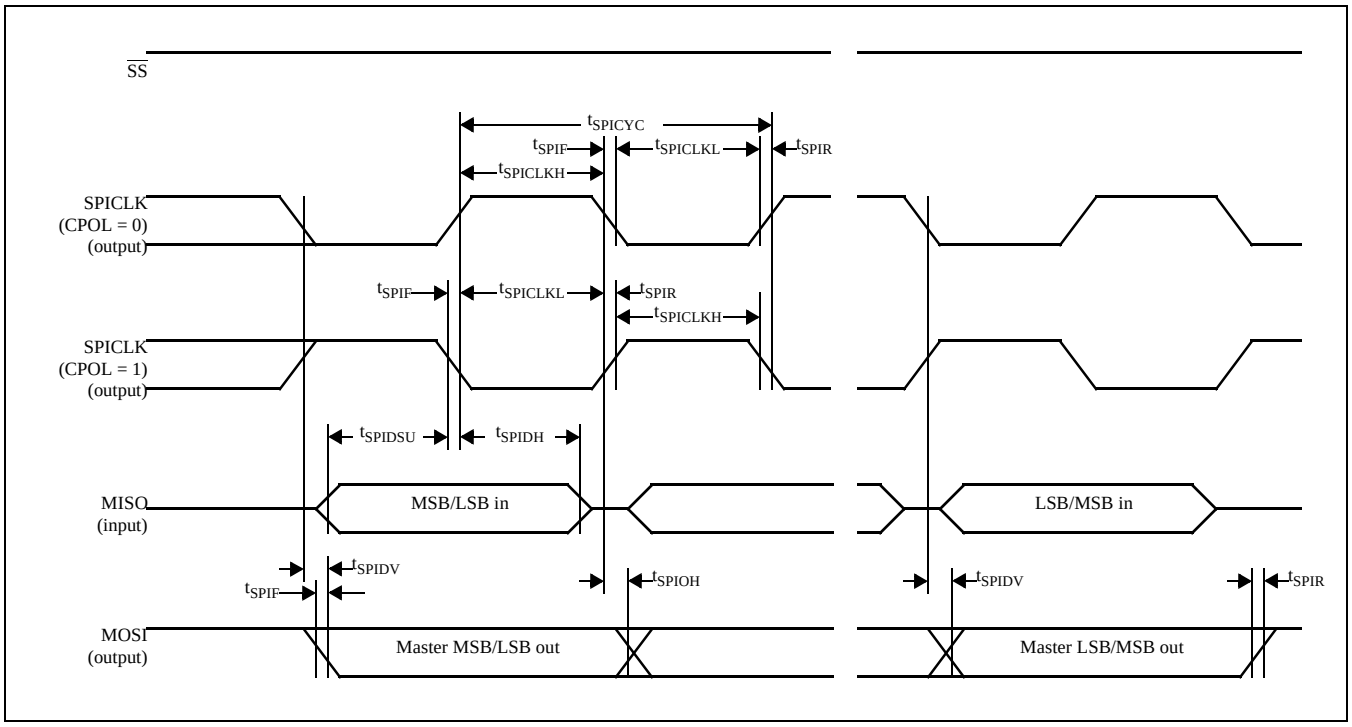


Figure 8: SPI Master Timing (CPHA = 0)

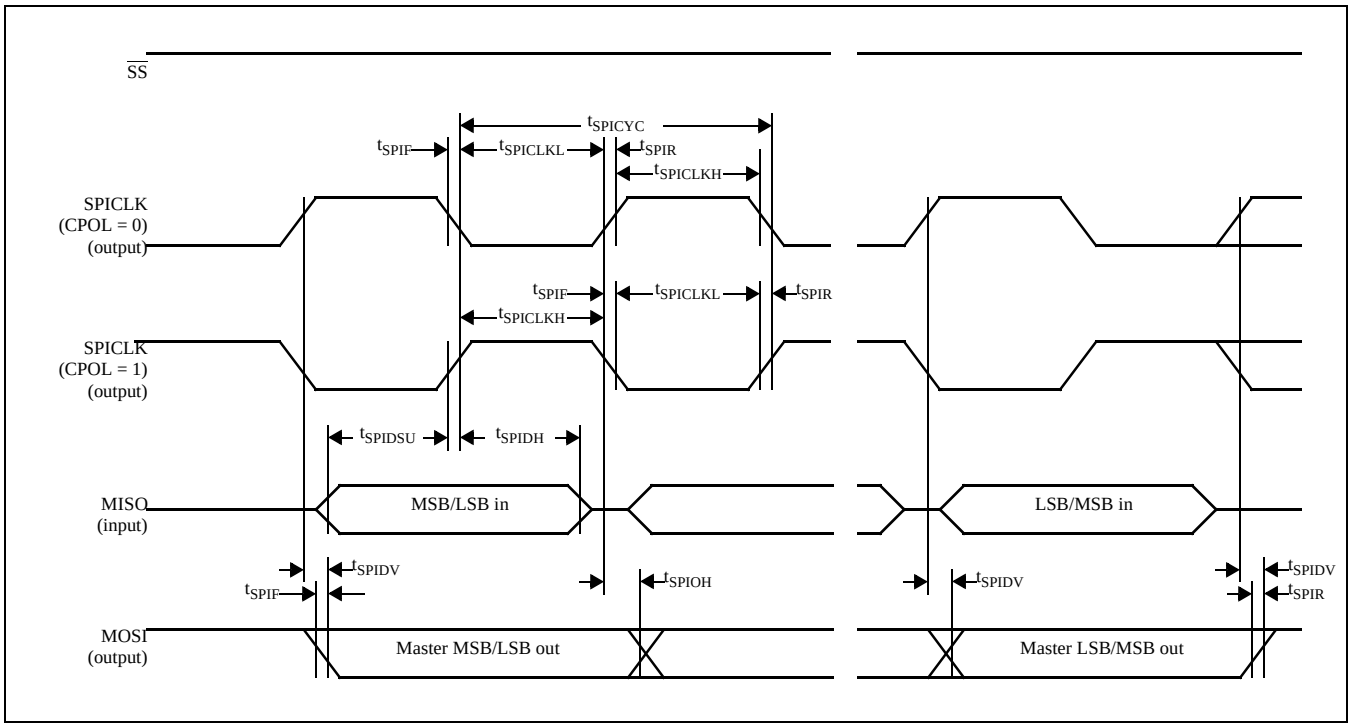


Figure 9: SPI Master Timing (CPHA = 1)

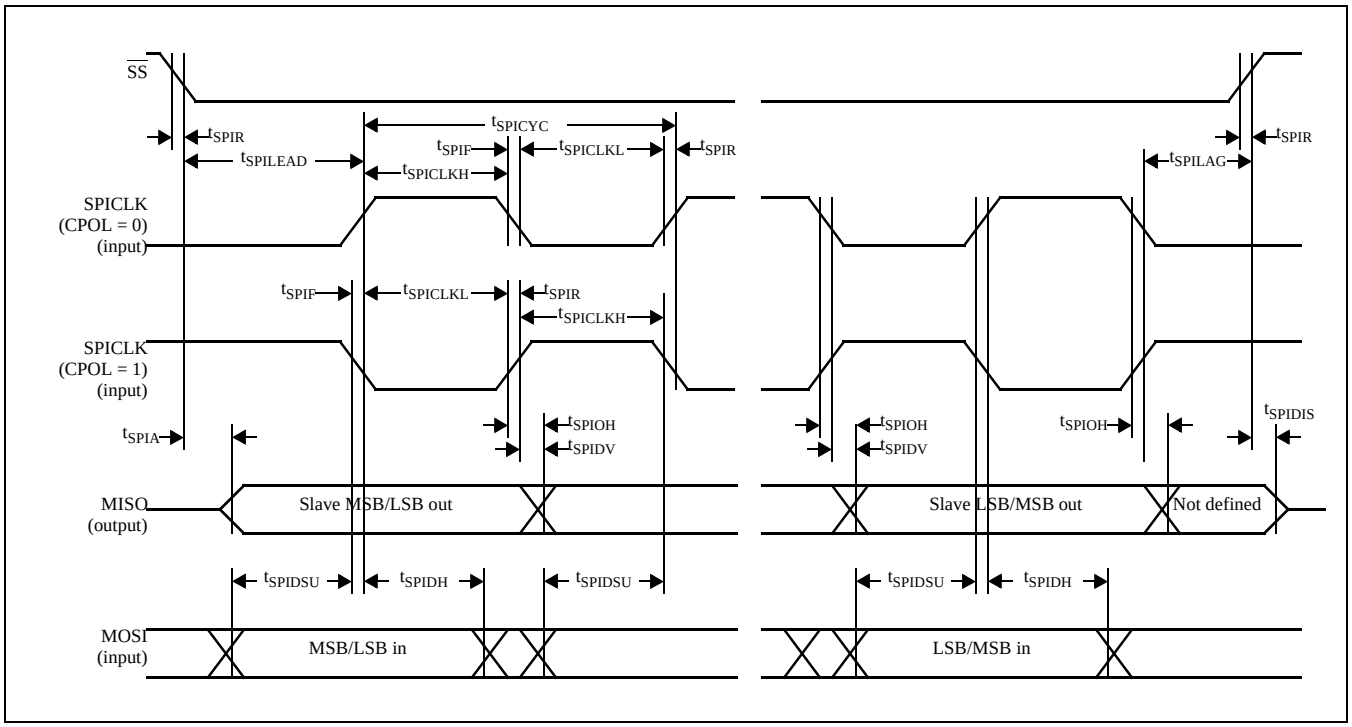


Figure 10: SPI Slave Timing (CPHA = 0)

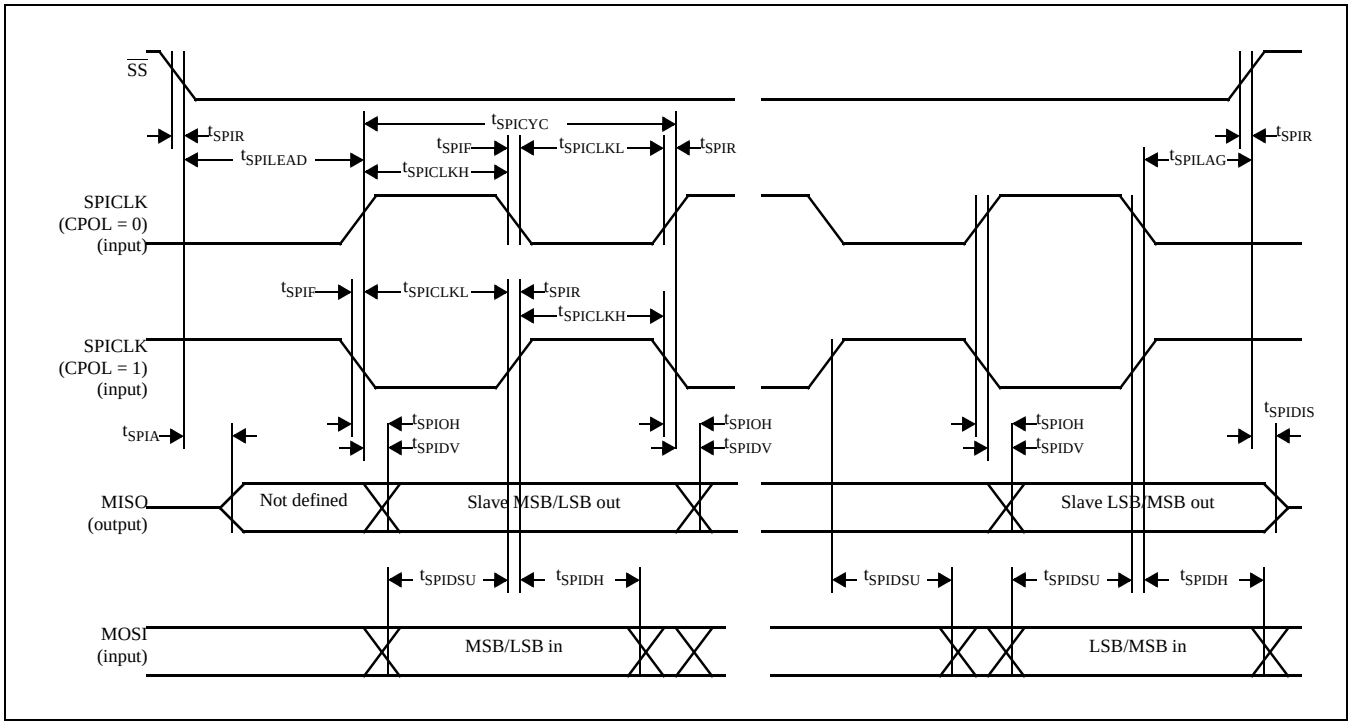


Figure 11: SPI Slave Timing (CPHA = 1)

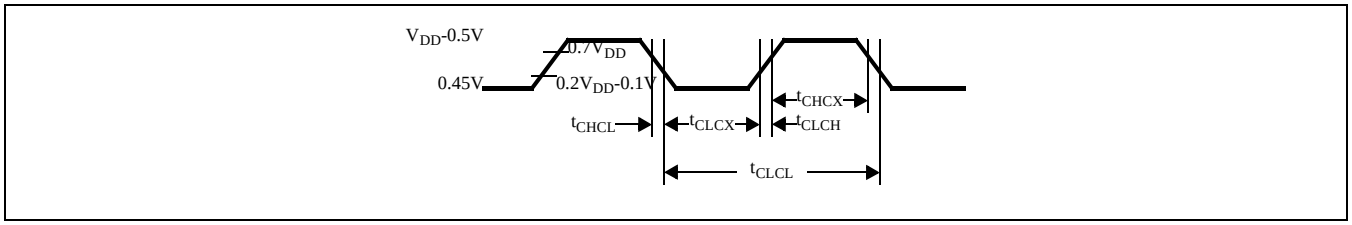


Figure 12: External Clock Drive

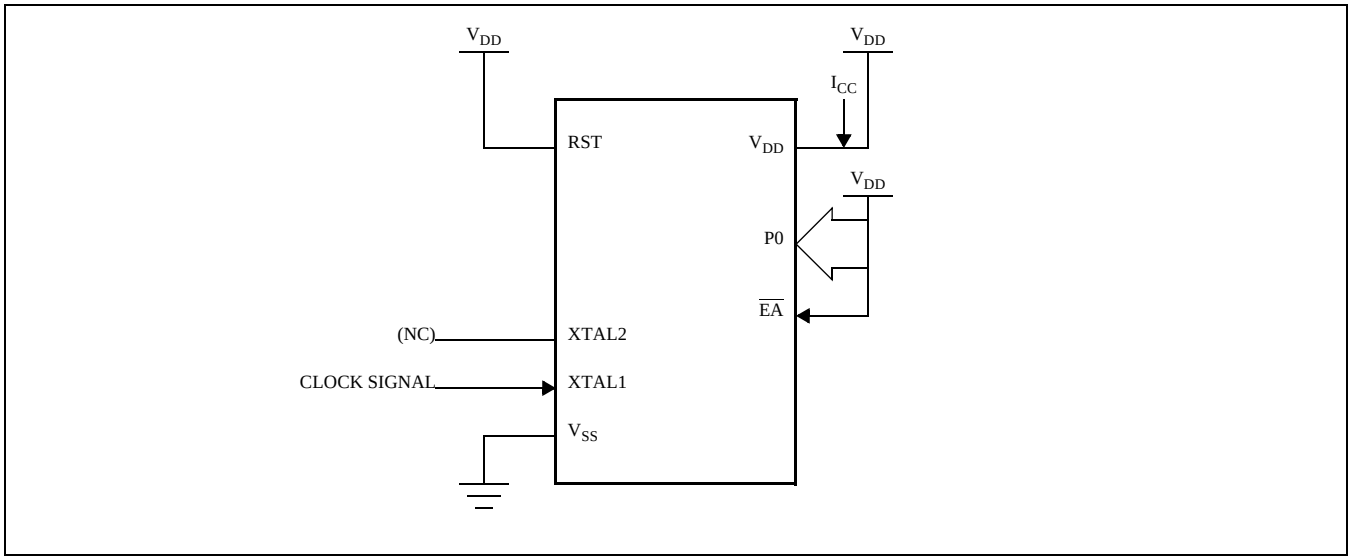


Figure 13: I_{CC} Test Condition, Active Mode (All other pins are disconnected)

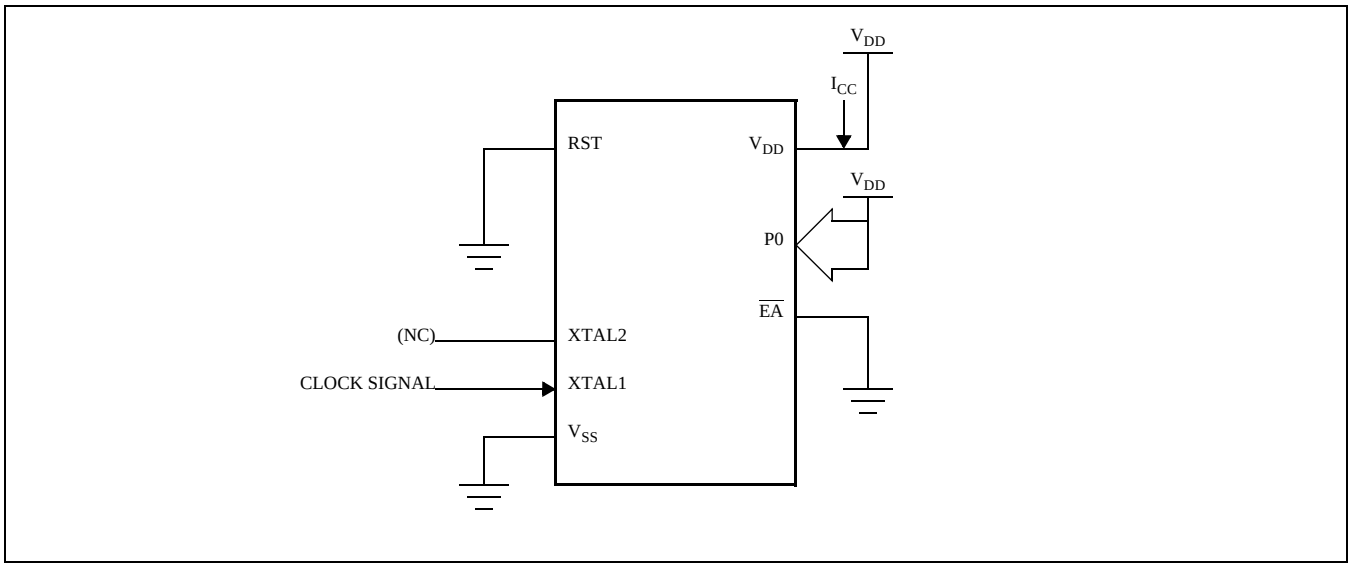


Figure 14: I_{CC} Test Condition, Idle Mode (All other pins are disconnected)

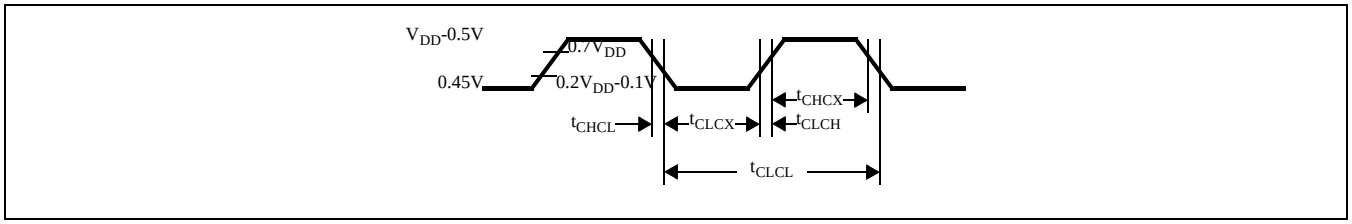


Figure 15: Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes $t_{CLCH} = t_{CHCL} = 5ns$

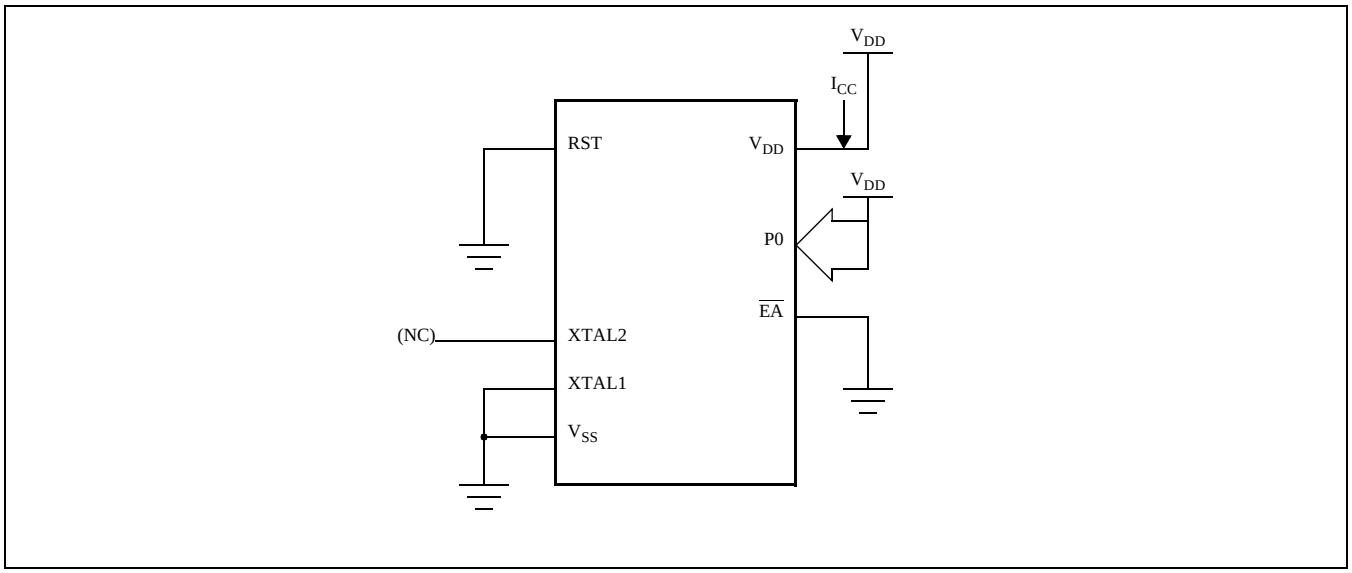


Figure 16: I_{CC} Test Condition, Power Down Mode (All other pins are disconnected, V_{DD} = 2.0V to 5.5V)

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Errata sheet

P87C51MB2/P87C51MC2

FUNCTIONAL DEVIATIONS

Deviation #1

RxD1 pin is an open drain configuration.

Work-around:

A resistor must be used if this pin is to be used as an output. These pins will become port 4 on the next release fixing this issue.

Deviation #2

Port 4 does not exist for the RxD1 and TxD1 pins. DC parameters differ from standard port pins.

Work-around:

None. These pins will become port 4 on the next release.

Deviation #3

RxD1, TxD1, and ALE pins will not go into once mode.

Work-around:

None. This will be fixed on the next release.

Deviation #4

In the UART, the contents of RB8 and SBUF change when they shouldn't if SM2=1 in modes 2 and 3.

Work-around:

None. Will be fixed on the next release.

Deviation #5

The UART double buffering will be implemented on the next release.

Work-around:

None.

Deviation #6

SPI block will be implemented on the next release.

Work-around:

None.

Deviation #7

Security bits are not 100% compatible with past 80c51 products.

Work-around:

The security bits will be compatible on the next release.

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Deviation #8

UART mode 0 receive data is sampled one clock later than standard 80C51 UARTS.

Work-around:

This requires an increased data hold time. This will be fixed on the next release.

Deviation #9

The PCA Watchdog timer function may not function properly at 24 MHz f_{OSC} when the PCA Count Pulse selection is set to “internal clock, $f_{OSC}/2$”.

Work-around:

None. This will be fixed on the next release.