DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1857A

SOUND CONTROL IC WITH SURROUND AND I²C BUS

DESCRIPTION

The μPC1857A is a sound control IC with I²C bus.

It has functions to control volume, balance, and tone, and a phase shift matrix surround function.

The surround function achieves wide sound expansion using only two front speakers. Three modes can be selected: movie mode that increases the presence of sound with stereo sound input, music mode emphasizing vocal music, and simulated mode that gives expansion and left and right sound depth with monaural sound input.

The μPC1857A can perform all control (mode switching, volume control and so on) using I²C.

FEATURES

- Volume control function : Attenuation adjustable from 0 to –80 dB in 64 steps
- Balance control function : The difference in attenuation adjustable from 0 to –80 dB in 64 steps
- Tone (bass, treble) control function : Adjustable in 32 steps from +10 to –10 dB
- Surround function (gain adjustable) : Three modes (movie, music, and simulated)
- Mute function
- Mixing function
- Output selection function (for two mono channels input)
- All parameters can be controlled via I²C bus.

APPLICATIONS

- TV, PC monitor

ORDERING INFORMATION

Part Number	Package
μPC1857ACT	30-pin plastic shrink DIP (400 mil)

The information in this document is subject to change without notice.

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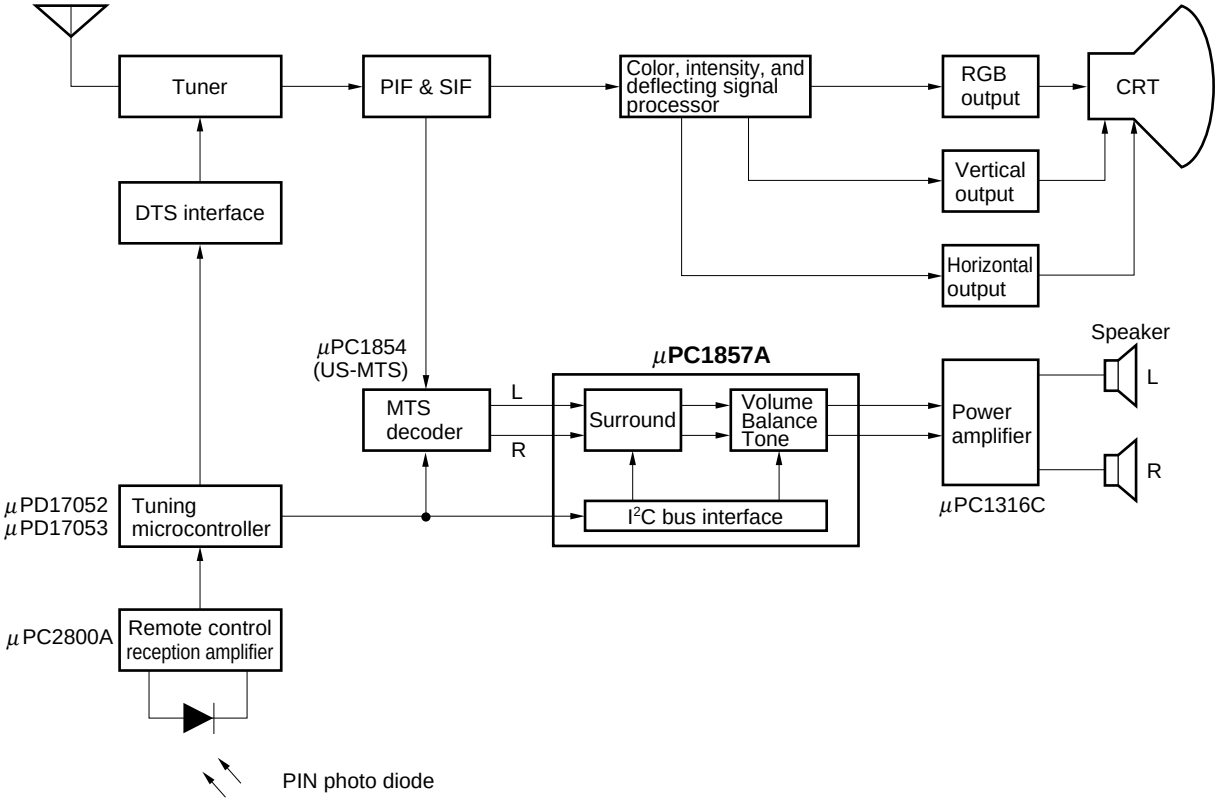
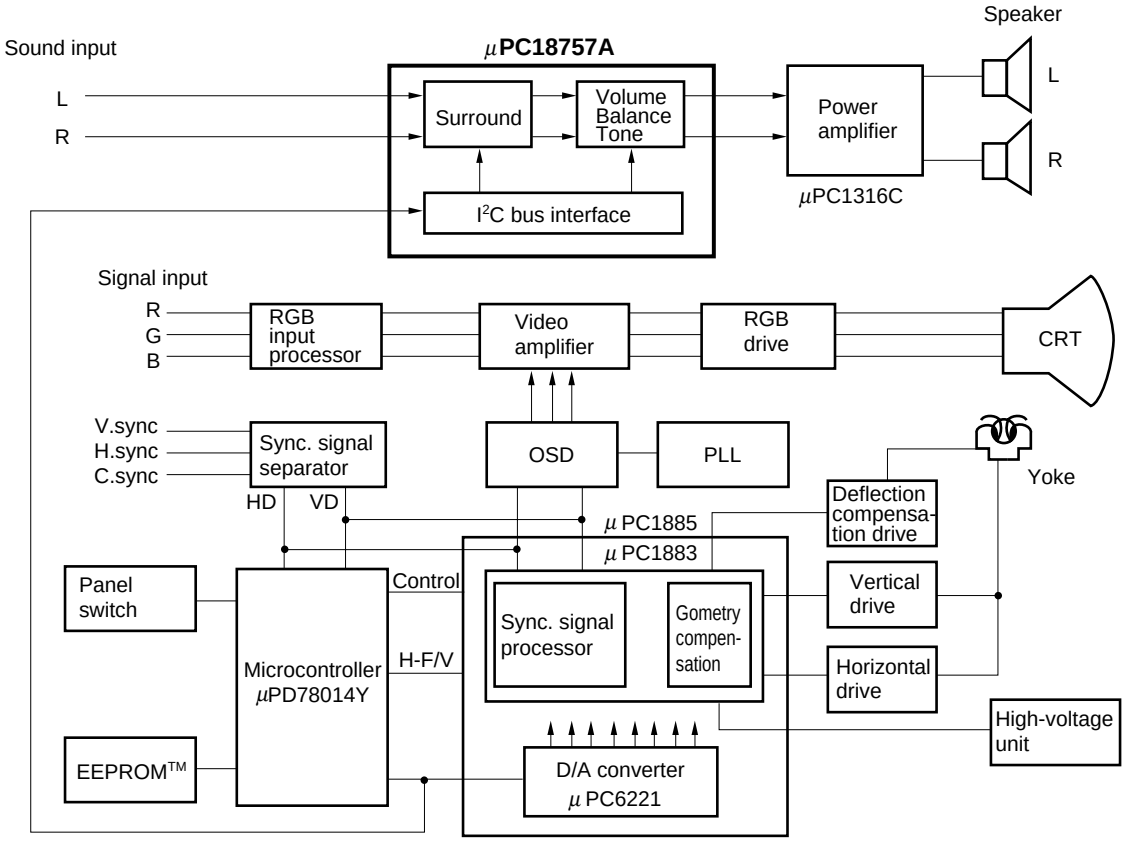
SYSTEM BLOCK DIAGRAM

- **TV**

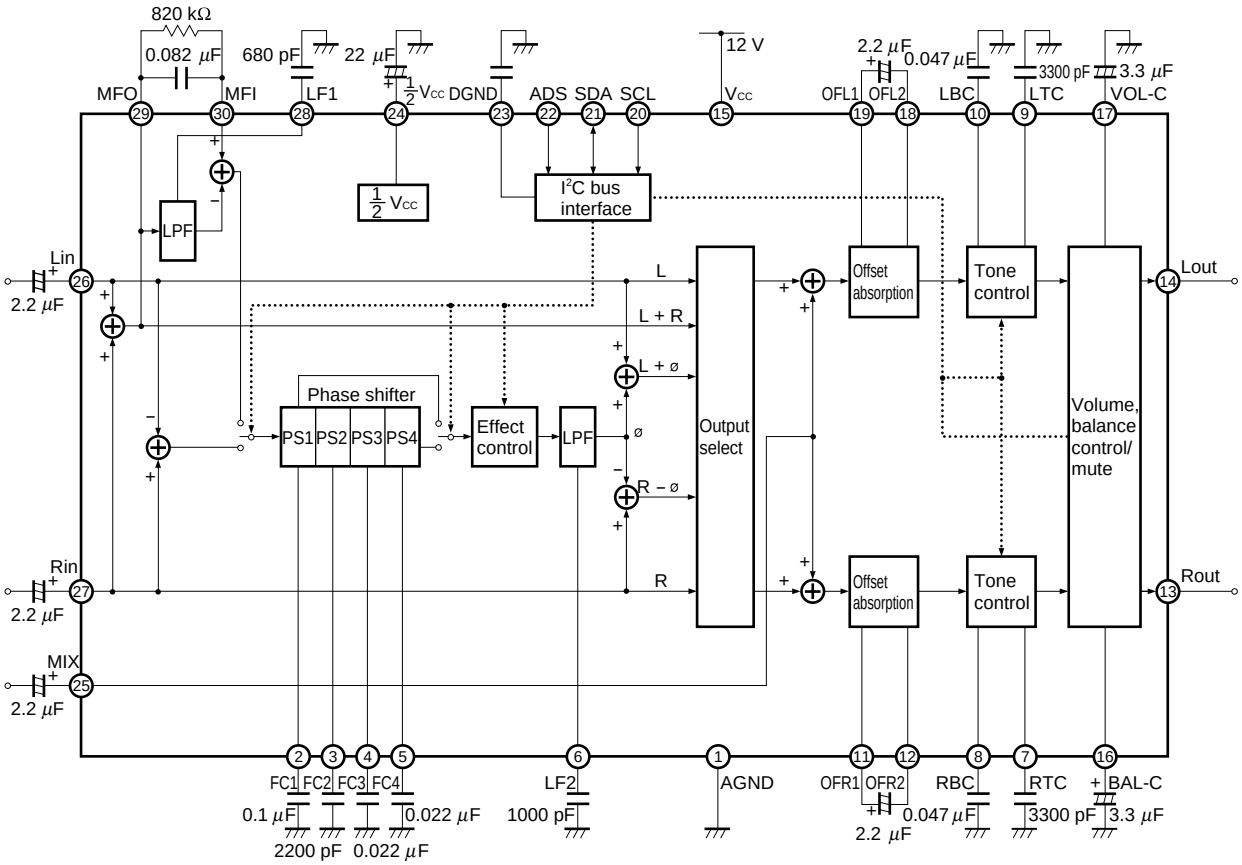


Remark DTS: Digital Tuning System
MTS: Multichannel Television Sound

- **PC monitor**

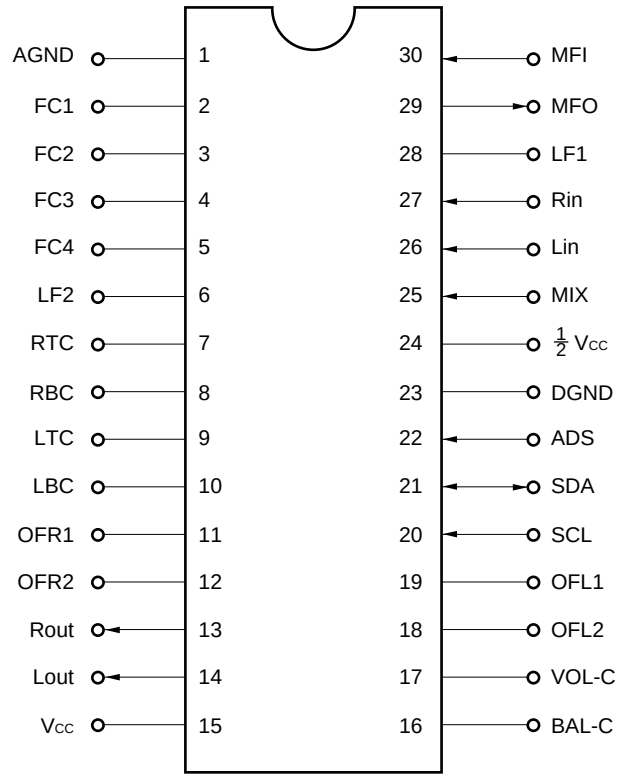

Speaker
Sound input
μPC18757A
L
R
Surround
Volume
Balance
Tone
Power
amplifier
L
R
μPC1316C
I2C bus interface
Signal input
R
G
B
RGB
input
processor
Video
amplifier
RGB
drive
CRT
V.sync
H.sync
C.sync
Sync. signal
separator
OSD
PLL
Yoke
HD
VD
μPC1885
μPC1883
Deflection
compensa-
tion drive
Panel
switch
Control
Microcontroller
μPD78014Y
H-F/V
Sync. signal
processor
Gometry
compen-
sation
Vertical
drive
Horizontal
drive
High-voltage
unit
EEPROM™
D/A converter
μPC6221

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

30-pin plastic shrink DIP (400 mil)

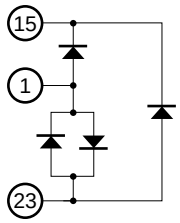
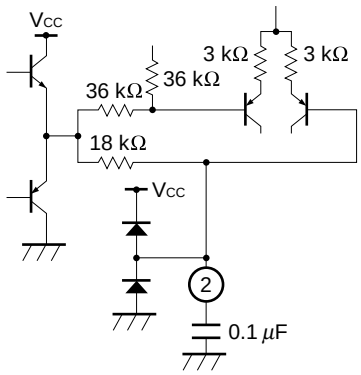
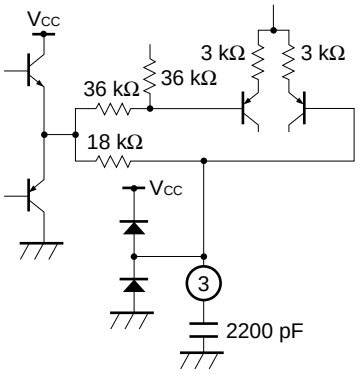
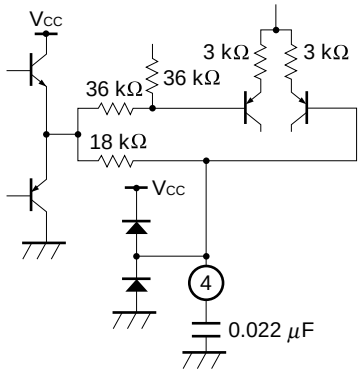


½ VCC	:	Reference Voltage Filter	MFO	:	Monaural Filter Output
ADS	:	Slave Address Select	MIX	:	Mixer Input
AGND	:	Analog Ground	OFL1, OFL2	:	L-channel Offset Absorption
BAL-C	:	Balance Control Offset Absorption	OFR1, OFR2	:	R-channel Offset Absorption
DGND	:	Ground for I^2C Bus	RBC	:	R-channel Bass Capacitor
FC1-FC4	:	Phase Shift Filter	Rin	:	R-channel Signal Input
LBC	:	L-channel Bass Capacitor	Rout	:	R-channel Signal Output
LF1, LF2	:	Low-pass Filter	RTC	:	R-channel Treble Capacitor
Lin	:	L-channel Signal Input	SCL	:	Serial Clock for I^2C Bus
Lout	:	L-channel Signal Output	SDA	:	Serial Data for I^2C Bus
LTC	:	L-channel Treble Capacitor	VCC	:	Power Supply
MFI	:	Monaural Filter Input	VOL-C	:	Volume Control Offset Absorption

CONTENTS

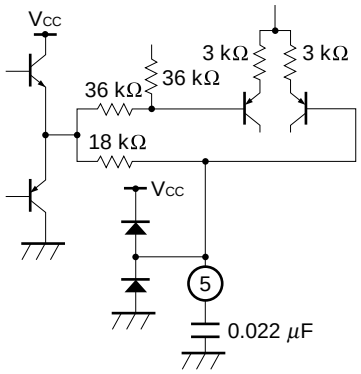
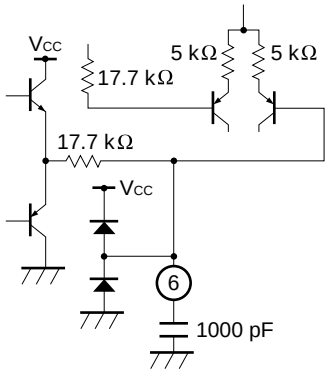
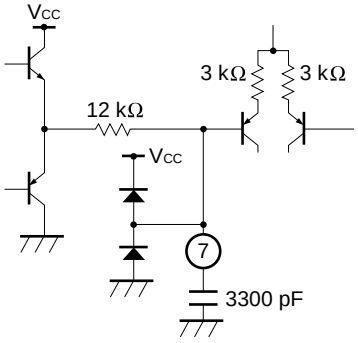
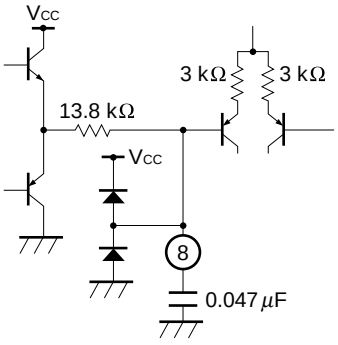
1. PIN FUNCTIONS

Table 1-1. Pin Function List (1/7)

Pin Number	Pin Name	Equivalent Circuit	Description
1	AGND		Ground for analog signal. Pin voltage: approx. 0.0 V
2	FC1		Connection pin for capacitor which determines time constant of phase shifter. Pin voltage: approx. 6.0 V
3	FC2		
4	FC3		

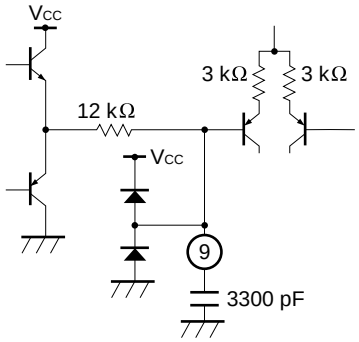
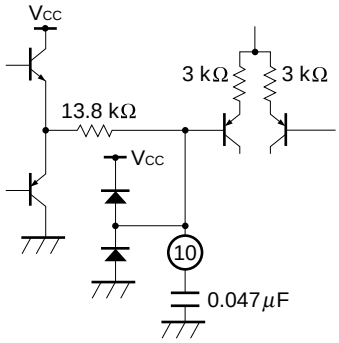
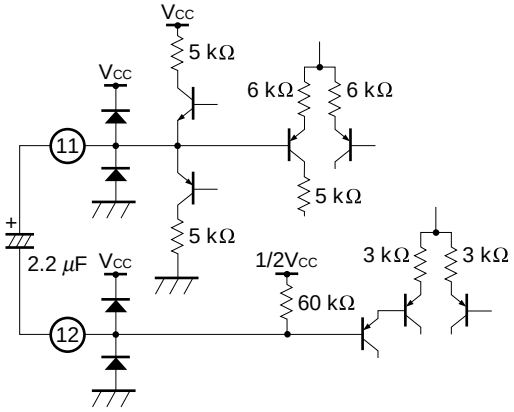
Remark Pin voltage is the reference value when V_{CC} = 12 V.

Table 1-1. Pin Function List (2/7)

Pin Number	Pin Name	Equivalent Circuit	Description
5	FC4		Connection pin for capacitor which determines time constant of phase shifter. Pin voltage: approx. 6.0 V
6	LF2		Low-pass filter. Pin voltage: approx. 6.0 V
7	RTC		Connection pin for capacitor for treble boost/cut frequency characteristic of R-channel signal. Pin voltage: approx. 6.0 V
8	RBC		Connection pin for capacitor for bass boost/cut frequency characteristic of R-channel signal. Pin voltage: approx. 6.0 V

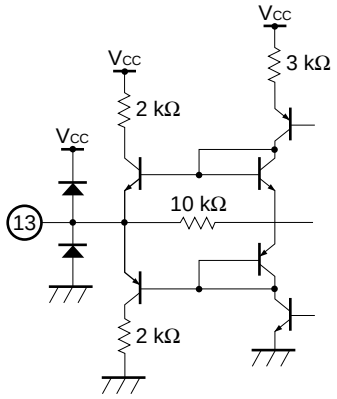
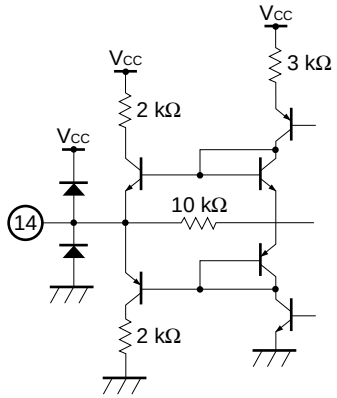
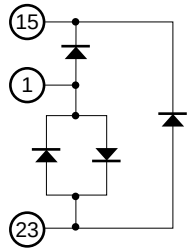
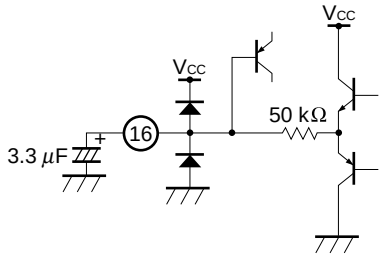
Remark Pin voltage is the reference value when V_{CC} = 12 V.

Table 1-1. Pin Function List (3/7)

Pin Number	Pin Name	Equivalent Circuit	Description
9	LTC		Connection pin for capacitor for treble boost/cut frequency characteristic of L-channel signal. Pin voltage: approx. 6.0 V
10	LBC		Connection pin for capacitor for bass boost/cut frequency characteristic of L-channel signal. Pin voltage: approx. 6.0 V
11	OFR1		Pin that absorbs offset voltage of R channel. Pin voltage: approx. 6.0 V
12	OFR2		

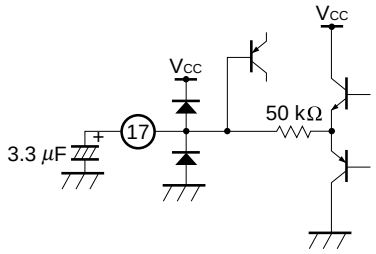
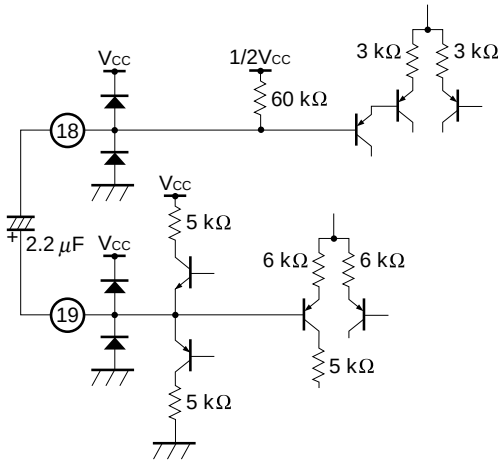
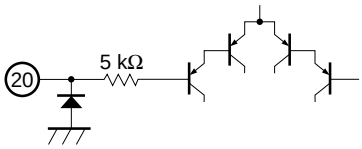
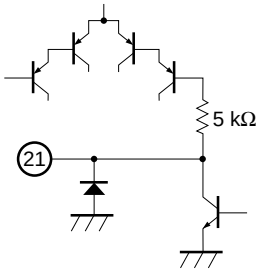
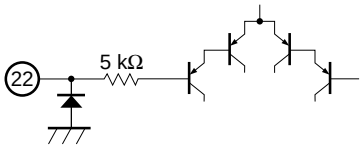
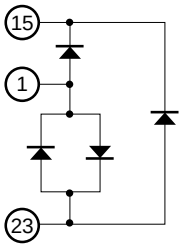
Remark Pin voltage is the reference value when V_{CC} = 12 V.

Table 1-1. Pin Function List (4/7)

Pin Number	Pin Name	Equivalent Circuit	Description
13	Rout		R-channel signal output pin. Pin voltage: approx. 6.0 V
14	Lout		L-channel signal output pin. Pin voltage: approx. 6.0 V
15	Vcc		Supply voltage. Pin voltage: approx. 12.0 V
16	BAL-C		Pin for D/A converter capacitor for balance control. Pin voltage: approx. 4.8 V

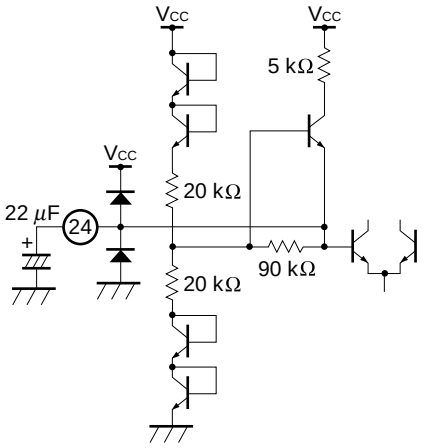
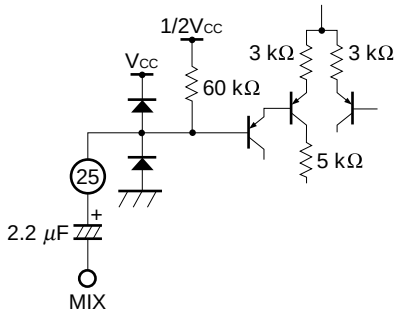
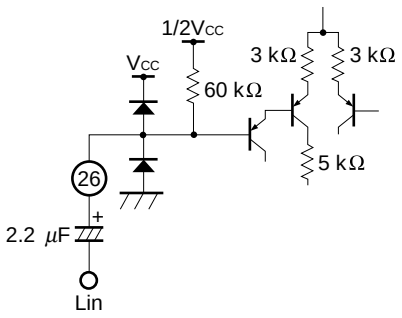
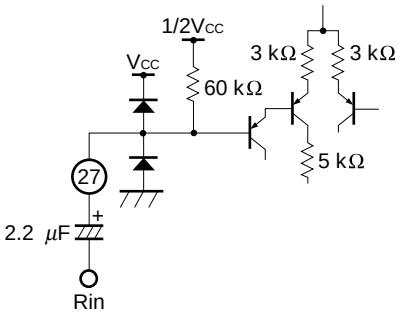
Remark Pin voltage is the reference value when Vcc = 12 V.

Table 1-1. Pin Function List (5/7)

Pin Number	Pin Name	Equivalent Circuit	Description
17	VOL-C		Pin for D/A converter capacitor for volume control. Pin voltage: approx. 6.0 V
18	OFL2		Pin that absorbs offset voltage of L channel. Pin voltage: approx. 6.0 V
19	OFL1		
20	SCL		Serial clock line (I^2C bus clock Input) pin. Pin voltage: approx. 0.0 V
21	SDA		Serial data line (I^2C bus data I/O) pin Pin voltage: approx. 0.2 V
22	ADS		Slave address select pin. Pin voltage: approx. 0.0 V
23	DGND		GND for I^2C bus signal. Pin voltage: approx. 0.0 V

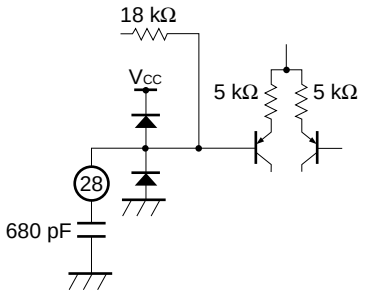
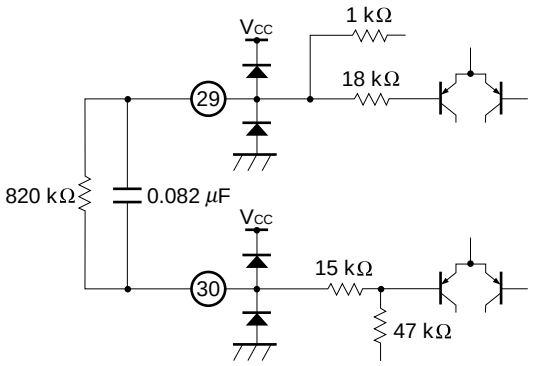
Remark Pin voltage is the reference value when V_{CC} = 12 V.

Table 1-1. Pin Function List (6/7)

Pin Number	Pin Name	Equivalent Circuit	Description
24	$\frac{1}{2}$ V_{CC}		Filter pin for middle point of supply voltage. Pin voltage: approx. 6.0 V
25	MIX		Mixing signal input pin. Input impedance: 60 kΩ Pin voltage: approx. 6.0 V
26	Lin		L-channel signal input pin. Input impedance: 60 kΩ Pin voltage: approx. 6.0 V
27	Rin		R-channel signal input pin. Input impedance: 60 kΩ Pin voltage: approx. 6.0 V

Remark Pin voltage is the reference value when V_{CC} = 12 V.

Table 1-1. Pin Function List (7/7)

Pin Number	Pin Name	Equivalent Circuit	Description
28	LF1		Low-pass filter. Pin voltage: approx. 6.0 V
29	MFO		Filter output pin for surround function (simulated mode) (see **4.3 Surround Function**). Pin voltage: approx. 6.0 V
30	MFI		Filter input pin for surround function (simulated mode) (see **4.3 Surround Function**). Pin voltage: approx. 6.0 V

Remark Pin voltage is the reference value when V_{CC} = 12 V.

2. ATTENTIONS

(1) Attention on Pop Noise Reduction

When changing the surround mode, use the mute function (approx. 200 ms) for pop noise reduction (see **4.4.1 Mute**).

When turning ON/OFF power to the μPC1857A, use the external mute function for pop noise reduction.

(2) Attention on Supply Voltage

Drive data on the I^2C bus after supply voltage of total application system becomes stable.

3. I²C BUS INTERFACE

The μPC1857A has serial bus function.

This serial bus (I²C bus) is a double-wired bus developed by Philips. It is composed of 2 wires: serial clock line (SCL) and serial data line (SDA).

The μPC1857A has built-in I²C bus interface circuit, and five rewritable registers (8 bits).

SCL (Serial Clock Line)

The host CPU outputs a serial clock to synchronize with the data. The μPC1857A takes in the serial data based on this clock.

Input level is compatible with CMOS.

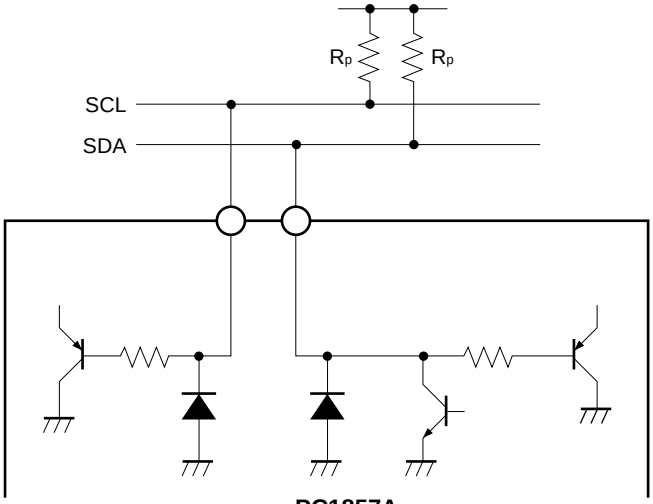
Clock frequency is 0 to 100 kHz.

SDA (Serial Data Line)

The host CPU outputs the data which is synchronized with the serial clock. The μPC1857A takes in this data based on the clock.

Input level is compatible with CMOS.

Figure 3-1. Internal Equivalent Circuit of Interface Pin



3.1 Data Transfer

3.1.1 Start condition

Start condition is made by SDA falling from “High” to “Low” while SCL is “High” as shown in Figure 3-2.

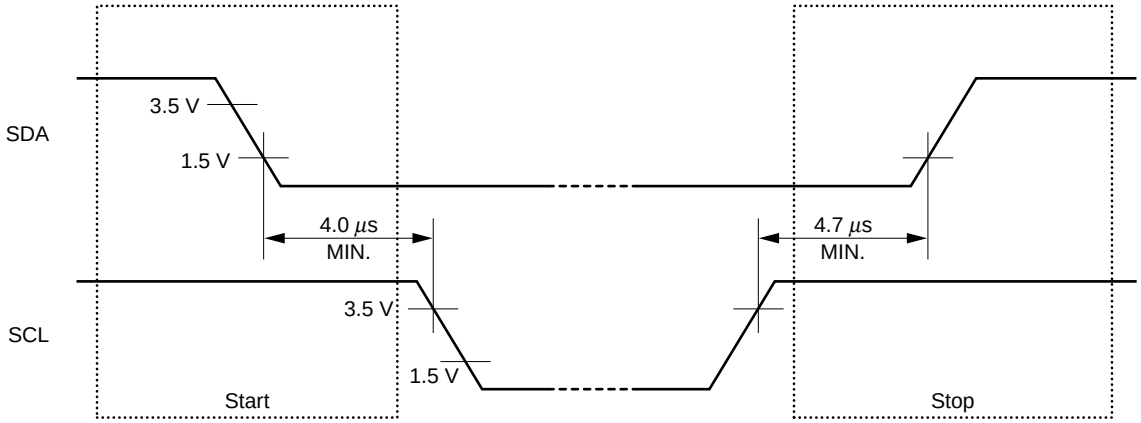
When this start condition is received, the μPC1857A takes in the data synchronized with the serial clock after that.

3.1.2 Stop condition

Stop condition is made by SDA rising from “Low” to “High” while SCL is “High” as shown in Figure 3-2.

When this stop condition is received, the μPC1857A stops taking in or outputting data.

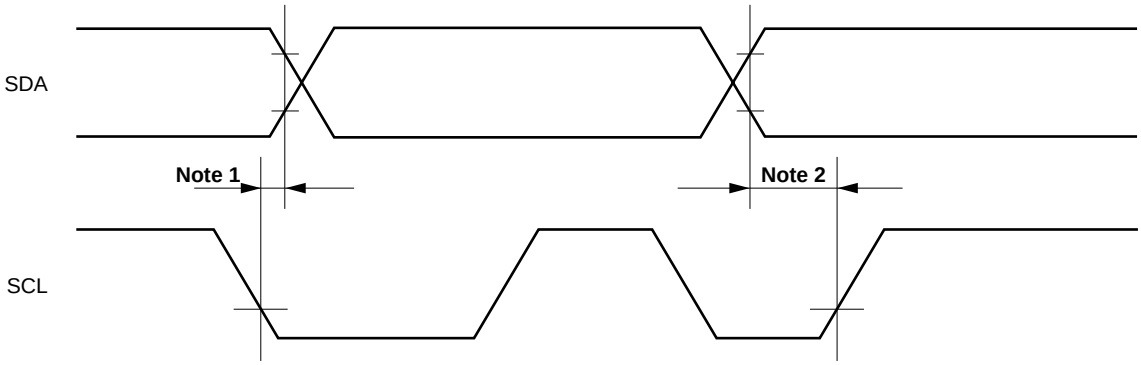
Figure 3-2. Start/Stop Condition of Data Transfer



3.1.3 Data transfer

When transferring data, the data must be changed while SCL is “Low” as shown in Figure 3-3. Never change the data while SCL is “High”.

Figure 3-3. Data Transfer



Notes 1. Data hold time for I^2C device: 300 ns MIN., Data hold time for CPU: 5 μs MIN.

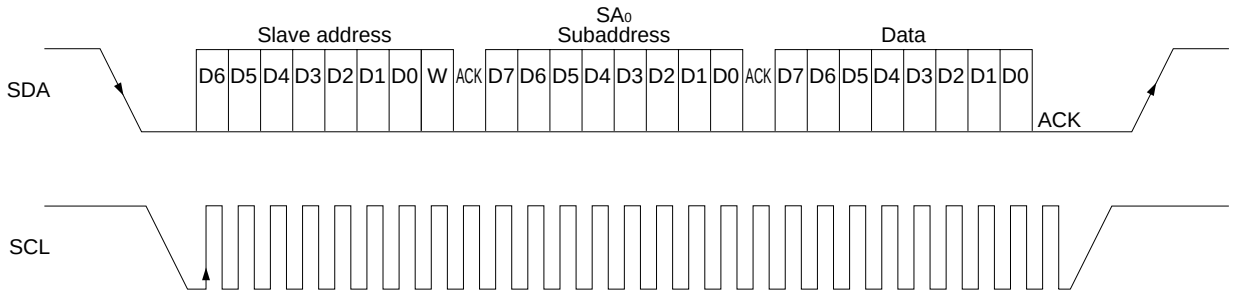
2. Data setup time: 250 ns MIN.

Remark Clock frequency: 0 to 100 kHz

3.2 Data Transfer Format

Figure 3-4 shows an example of data transfer in write mode.

Figure 3-4. Example of Data Transfer in Write Mode



Remark W: Write mode, ACK: Acknowledge bit

Data is composed of 8 bits. One acknowledge bit always follows these 8 bits of data. Data must be transferred starting from the MSB.

The 1 byte immediately following the start condition specifies a slave address (chip address). This slave address is composed of 7 bits.

Table 3-1 shows the slave address of the μPC1857A. This slave address is registered by Philips.

Table 3-1. Slave Address of μPC1857A

Bias Voltage of ADS (Pin 22)	Slave Address						
	D6	D5	D4	D3	D2	D1[Note]	D0
5 V	1	0	0	0	1	1	0
GND	1	0	0	0	1	0	0

Note The user can set bit D1 freely.
0: Bias voltage of ADS (pin 22) is 0 V.
1: Bias voltage of ADS (pin 22) is 5 V.

The 1 bit following the slave address is a read/write bit which specifies the direction of the data to be subsequently transferred. Write “0” to this read/write bit because the μPC1857A is write mode only.

The byte following the slave address is the subaddress byte of the μPC1857A.

The μPC1857A has five subaddresses, from SA_0 to SA_4, and each of these addresses is composed of 8 bits. The data to be set to a subaddress follows this subaddress byte.

3.2.1 1-byte data transfer

The format in which 1-byte data is to be transferred is as follows:

Start	Slave address	Write mode	ACK	Subaddress	ACK	Data	ACK	Stop

3.2.2 Successive data transfer

The μPC1857A has an automatic increment function which can be used to transfer successive data (refer to **4.4.6 Automatic increment**).

By using this function, the internal subaddress is automatically incremented if a slave address and a subaddress have been set, so that the data from subsequent subaddresses can be transferred in succession.

Incrementing the subaddress of the μPC1857A is stopped when the subaddress reaches “04H”.

The format in which 5 bytes of data are to be transferred in succession by using the automatic increment function is as follows:

Start	Slave address	Write mode	ACK	Subaddress	ACK	Data 1	ACK	Data 2	ACK	----------	Data 5	ACK	Stop

The host CPU transfers “00H” as subaddress SA_0 after start and slave addresses, as shown above. Data SA_0 is transferred after this subaddress SA_0, and without transferring the stop condition the data SA_1, SA_2, SA_3, and SA_4 are transferred successively, and then the stop condition is transferred.

To successively change data at a fixed subaddress, for example to turn up/down the volume, turn off the automatic increment function.

3.2.3 Acknowledge

On the I^2C bus, an acknowledge bit is appended to the 9th bit following the data. This acknowledge bit is used to judge whether data transfer has been successful. The host CPU judges whether data transfer has been successful or not, depending on whether the status of the acknowledge bit is “H” or “L”.

When the acknowledge bit is “L”, it indicates success. When the acknowledge bit is “H”, it indicates failure of transfer or forced release of bus (NAK status). The NAK status occurs when a wrong slave address is transferred to a slave IC or data transfer from slave side is finished in the read status.

4. EXPLANATION OF EACH COMMAND

4.1 Subaddress List

Bit / Subaddress	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
00H	Output mute 0: OFF 1: ON	0	Output select D5 D4 Lout Rout 0 0 L R 0 1 L L 1 0 R R 1 1 L + R L + R		Surround mode D3 D2 Mode 0 0 Simulated 0 1 Music 1 0 Movie 1 1 OFF		Surround effect D1 D0 Gain 0 0 0 dB 0 1 –3 dB 1 0 –6 dB 1 1 –12 dB	
01H	Mix 0: OFF 1: ON	Automatic increment 0: OFF 1: ON	Volume level Volume : MAX to MIN Data : 111111 to 000000					
02H	0	Automatic increment 0: OFF 1: ON	Balance L volume : MIN to MAX to MAX R volume : MAX to MAX to MIN Data : 111111 to 100000 to 000000					
03H	0	Automatic increment 0: OFF 1: ON	0	Bass level Gain : Boost to 0 to Cut Data : 11111 to 10000 to 00000				
04H	0	Automatic increment 0: OFF 1: ON	0	Treble level Gain : Boost to 0 to Cut Data : 11111 to 10000 to 00000				

Cautions 1. Be sure to write "0" to bit D7 of subaddresses 02H through 04H, bit D6 of subaddress 00H, and bit D5 of subaddresses 03H and 04H.

2. The surround mode is OFF: 00H (D3, D2 = 11) in any mode other than stereo mode is selected for output: 00H (D5, D4 = 00).

4.2 Initialization

After power application, be sure to initialize the subaddresses as shown below.

Table 4-1. Initialization of μPC1857A (recommendation value)

Bit / Subaddress	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
00H	0	0	0	0	1	1	0	0
01H	0	–	–	–	–	–	–	–
02H	0	–	1	0	0	0	0	0
03H	0	–	0	1	0	0	0	0
04H	0	–	0	1	0	0	0	0

Caution Until initialization is completed, mute using an external unit.

Remark – : Don't care.

4.3 Surround Function

For how to set the surround mode, refer to the table below.

Table 4-2. Setting Surround Mode

Setting / Surround Mode	Subaddress: 00H		Description	
	D3	D2	Units of Phase Shifter	Effect
Simulated	0	0	4 units	Monaural to pseudo-stereo
Music	0	1	1 unit	Stereo sound to surround
Movie	1	0	4 units	
OFF	1	1	–	Through

Caution When changing the surround mode, use the mute function (approx. 200 ms) for pop noise reduction.

4.4 Explanation of Each Command

4.4.1 Mute

The mute function can be turned ON/OFF by using data of bit D7 of subaddress 00H.

Figure 4-1. Mute

	D7	D6	D5	D4	D3	D2	D1	D0
Subaddress 00H	Mute	0	Output selection		Surround mode		Surround effect	

Output mute

0	Mute: OFF
1	Mute: ON

Caution When changing the surround mode, and when turning ON/OFF power, use the mute function (approx. 200 ms) for pop noise reduction.

4.4.2 Output selection

Output can be selected by using data of bits D5 and D4 of subaddress 00H.

Figure 4-2. Output Selection

	D7	D6	D5	D4	D3	D2	D1	D0
Subaddress 00H	Mute	0	Output selection		Surround mode		Surround effect	

Output selection

Data		Output	
D5	D4	Lout	Rout
0	0	L	R
0	1	L	L
1	0	R	R
1	1	L + R	L + R

Caution The surround mode is OFF (D3, D2 = 11) in modes other than the stereo mode (D5, D4 = 00).

4.4.3 Surround mode

The following surround modes can be selected by using data of bits D3 and D2 of subaddress 00H.

Simulated : Simulated stereo sound for monaural source. The difference between the signal that has gone through HPF and the signal that has gone through LPF is calculated, and the phase of the difference is shifted and added to the original signal. The simulated stereo effect is created if the output frequency characteristics of the L-channel and R-channel signals is comb-shaped.

Music : Surround sound for stereo source. The phase of the differential signal between L and R channels (L-R signal) is rotated by a phase shifter (1-unit), and is added to the original signal.

Movie : Surround sound for stereo source. The phase of the differential signal between L and R channels (L-R signal) is rotated by a phase shifter (4-unit), and is added to the original signal.

OFF : Original signal as is.

Figure 4-3. Surround Mode

	D7	D6	D5	D4	D3	D2	D1	D0
Subaddress 00H	Mute	0	Output selection		Surround mode		Surround effect	

Surround mode

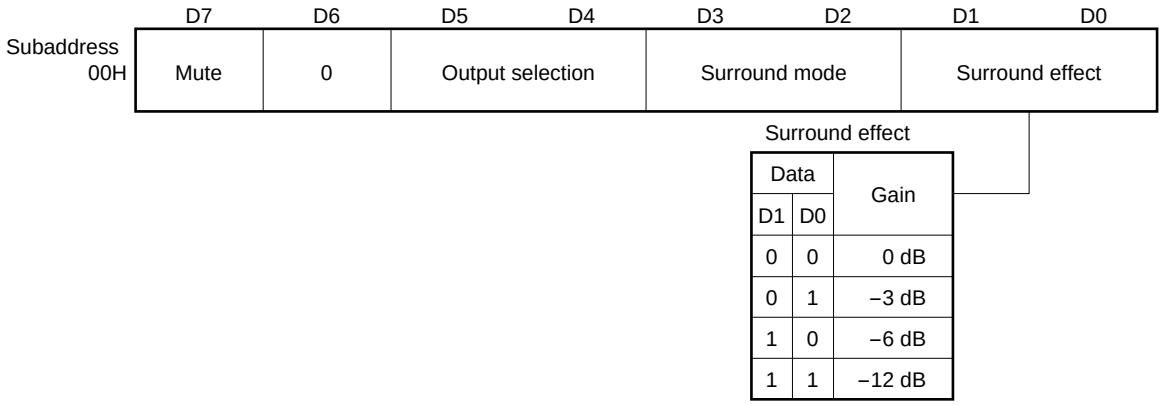
Data		Mode
D3	D2	
0	0	Simulated
0	1	Music
1	0	Movie
1	1	OFF

Caution The surround mode is OFF (D3, D2 = 11) if the stereo mode is not selected by the output selection bits (D5, D4 = 00).

4.4.4 Surround effect

The surround effect can be changed in four steps by using the data of bits D1 and D0 of subaddress 00H.

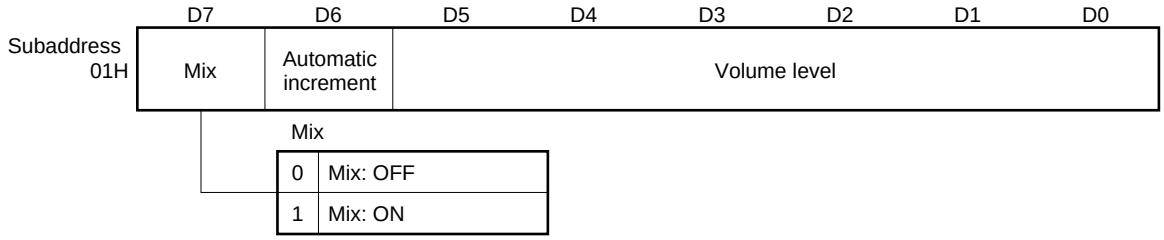
Figure 4-4. Surround Effect



4.4.5 Mix

Mixing of the signal input to the MIX pin can be turned ON/OFF by using the data of bit D7 of subaddress 01H.

Figure 4-5. Mix

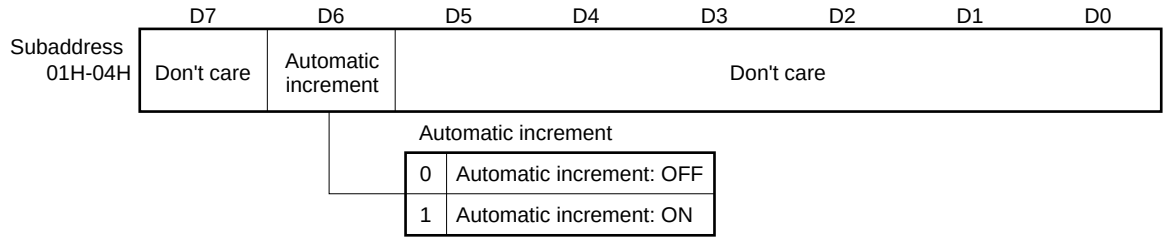


4.4.6 Automatic increment

The automatic increment function can be turned ON/OFF by using the data of bit D6 of subaddresses 01H through 04H.

This is effective when transmitting data successively (refer to **3.2.2 Successive data transfer**).

Figure 4-6. Automatic Increment



Caution Subaddress 00H does not have an automatic increment function. It is always set to ON.

The automatic increment function automatically increments the subaddress when data is transferred successively.

Automatic increment ON : The subaddress is automatically incremented immediately after byte data with D6 = 1 has been transferred.
This setting is useful if the data at every subaddress is to be set at once for initialization. The subaddress is always incremented immediately after the data of subaddress: 00H has been transferred.

Automatic increment OFF : The subaddress is fixed immediately after byte data with D6 = 0 has been transferred. This setting is useful when the data at the same subaddress is to be successively changed, for example to turn up/down the volume.

There is an automatic increment function ON/OFF bit in subaddresses 01H through 04H. Incrementing subaddresses is individually controlled by the automatic increment function ON/OFF bit of each subaddress.

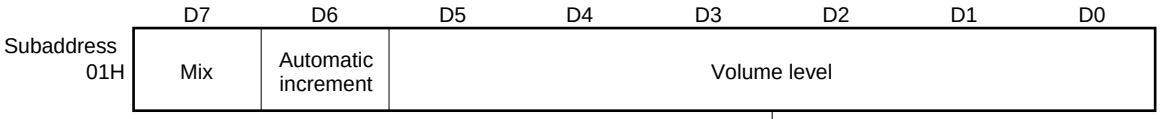
For example, if the automatic increment function of subaddress 01H is turned ON, and that of subaddress 02H is turned OFF, the subaddress is automatically incremented from 01H to 02H, and is fixed to 02H.

Even if the automatic increment function ON/OFF bit of subaddress 04H is set to ON, the subaddress is not incremented. If the next data is transferred after the data of 04H has been set (acknowledge bit: L), acknowledge enters the NAK status (acknowledge bit: H), and data transfer from the host CPU is stopped.

4.4.7 Volume level

The volume of output can be controlled in 64 steps by using the data of bits D5 through D0 of subaddress 01H.

Figure 4-7. Volume Level



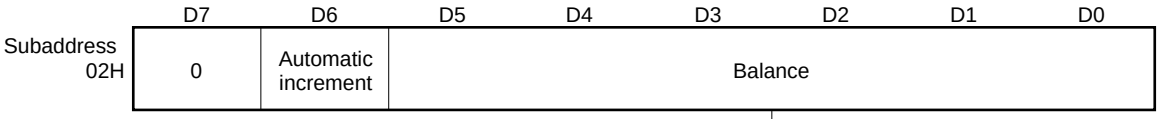
Volume level

Data D5-D0	Volume
000000 to 111111	MIN. to MAX.

4.4.8 Balance

The balance of output of the Lout and Rout pins can be controlled in 64 steps by using the data of bits D5 through D0 of subaddress 02H.

Figure 4-8. Balance



Balance

Data	Volume	
D5-D0	Lout	Rout
000000 to 100000	MAX. to MAX.	MIN. to MAX.
to 111111	to MIN.	to MAX.

4.4.9 Bass level

The bass level of output can be controlled in 32 steps by using the data of bits D4 through D0 of subaddress 03H.

Figure 4-9. Bass Level

	D7	D6	D5	D4	D3	D2	D1	D0
Subaddress 03H	0	Automatic increment	0	Bass level				

Bass level

Data D4-D0	Gain
00000	Cut
to	to
10000	0
to	to
11111	Boost

4.4.10 Treble level

The treble level of output can be controlled in 32 steps by using the data of bits D4 through D0 of subaddress 04H.

Figure 4-10. Treble Level

	D7	D6	D5	D4	D3	D2	D1	D0
Subaddress 04H	0	Automatic increment	0	Treble level				

Treble level

Data D4-D0	Gain
00000	Cut
to	to
10000	0
to	to
11111	Boost

5. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (Unless otherwise specified, T_A = 25 °C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}	Without signal	14.0	V
Input signal voltage	V_{IN}	Pins Lin, Rin, MIX	V_{CC}	V
I^2C bus input signal voltage	V_{CNT}	Pins SDA, SCL	V_{CC} + 0.2	V
Permissible package dissipation	P_D	T_A = 75 °C	500	mW
Operating temperature	T_A	V_{CC} = 12 V	–20 to +75	°C
Storage temperature	T_{stg}		–40 to +125	°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.

Recommended Operating Conditions (Unless otherwise specified, T_A = 25 °C)

Parameter	Symbol	Condition	Rating			Unit
			MIN.	TYP.	MAX.	
Supply voltage	V_{CC}	Gain between input and output: 0 dB	8.1	12.0	13.2	V
Input signal voltage	V_{IN}	V_{CC} = 12 V, gain between input and output: 0 dB	0.0	1.4	7.9	V_{p-p}
I^2C bus input voltage (H)	V_{cntH}	Pins SDA, SCL	3.5	5.0	6.0	V
I^2C bus input voltage (L)	V_{cntL}		–0.1	0	+1.5	V

Electrical Characteristics (1/5)

(Unless otherwise specified, V_{CC} = 12 V, T_A = 25 °C, RH ≤ 70%, f = 1 kHz, V_{IN} = 0.5 $V_{r.m.s.}$, no load)

Parameter	Symbol	Test Condition	Subaddress Data					Rating			Unit
			00	01	02	03	04	MIN.	TYP.	MAX.	
Circuit current	I_{CC}	No signal	0D	3F	20	10	10	12	18	25	mA
Maximum input voltage Lin → Lout	VOM-L	Lin = variable (tested) Lout = THD 1%	0D	3F	20	10	10	2.8	3.1	–	$V_{r.m.s.}$
Maximum input voltage Rin → Rout	VOM-R	Rin = variable (tested) Rout = THD 1%						2.8	3.1	–	$V_{r.m.s.}$
Distortion rate Lin → Lout	THDL	Lin = 2.0 $V_{r.m.s.}$ Rin = GND	0D	2B	20	10	10	–	0.1	0.5	%
Distortion rate Rin → Rout	THDR	Lin = GND Rin = 2.0 $V_{r.m.s.}$						–	0.1	0.5	%
Voltage gain Lin → Lout	GV-LL	Lin = 0.5 $V_{r.m.s.}$ Rin = GND	0D	3F	20	10	10	–1.0	0	+1.0	dB
Voltage gain Rin → Rout	GV-RR	Lin = GND Rin = 0.5 $V_{r.m.s.}$						–1.0	0	+1.0	dB
Voltage gain MIX → Lout	GV-ML	MIX = 0.5 $V_{r.m.s.}$ Lin, Rin = GND	0D	BF	20	10	10	5.0	6.0	7.0	dB
Voltage gain MIX → Rout	GV-MR							5.0	6.0	7.0	dB
Ripple rejection ratio V_{CC} → Lout	SVRR-L	V_{CC} = 100 $mV_{r.m.s.}$ f = 100 Hz Lin, Rin = GND	0D	14	20	10	10	–	–	–50	dB
Ripple rejection ratio V_{CC} → Rout	SVRR-R							–	–	–50	dB
Output noise voltage (surround OFF) Lout	Vn-L (OFF)	Rg = 0 Ω, JIS-A	0D	3F	20	10	10	–	–	50	$\mu V_{r.m.s.}$
Output noise voltage (surround OFF) Rout	Vn-R (OFF)							–	–	50	$\mu V_{r.m.s.}$
Cross talk Lin → Rout	CT-L	Lin = 0.5 $V_{r.m.s.}$ Rin = GND	0D	3F	20	10	10	–	–80	–70	dB
Cross talk Rin → Lout	CT-R	Lin = GND Rin = 0.5 $V_{r.m.s.}$						–	–80	–70	dB

Electrical Characteristics (2/5)

(Unless otherwise specified, V_{CC} = 12 V, T_A = 25 °C, RH ≤ 70%, f = 1 kHz, V_{IN} = 0.5 $V_{r.m.s.}$, no load)

Parameter	Symbol	Test Condition	Subaddress Data					Rating			Unit
			00	01	02	03	04	MIN.	TYP.	MAX.	
Volume attenuation 1 Lin → Lout1	VOL-L1	Lin = 0.5 $V_{r.m.s.}$ Rin = GND	0D	3F	20	10	10	–1.5	0	+1.5	dB
Volume attenuation 2 Lin → Lout2	VOL-L2			20				–20.0	–14.0	–7.0	dB
Volume attenuation 3 Lin → Lout3	VOL-L3			00				–	–	–80.0	dB
Volume attenuation deviation Rin → R/Lout1	VOL-RL1	Lin = GND Rin = 0.5 $V_{r.m.s.}$ Difference from VOL-L1	0D	3F	20	10	10	–1.0	0	+1.0	dB
Volume attenuation deviation Rin → R/ Lout2	VOL-RL2	Lin = GND Rin = 0.5 $V_{r.m.s.}$ Difference from VOL-L2		20				–1.0	0	+1.0	dB
Volume attenuation deviation Rin → R/ Lout3	VOL-RL3	Lin = GND Rin = 0.5 $V_{r.m.s.}$ Difference from VOL-L3		00				–3.0	0	+3.0	dB
Mute attenuation Lin → Lout	MUTE-L	Lin = 2.0 $V_{r.m.s.}$ Rin = GND	8D	3F	20	10	10	–	–	–80.0	dB
Mute attenuation Rin → Rout	MUTE-R	Lin = GND Rin = 2.0 $V_{r.m.s.}$						–	–	–80.0	dB
Balance attenuation L1 Lin → Lout1	BAL-L1	Lin = 0.5 $V_{r.m.s.}$ Rin = GND	0D	3F	01	10	10	–1.5	0	+1.5	dB
Balance attenuation L2 Lin → Lout2	BAL-L2				28			–2.5	–0.5	+1.0	dB
Balance attenuation L3 Lin → Lout3	BAL-L3				30			–15.0	–10.0	–5.0	dB
Balance attenuation L4 Lin → Lout4	BAL-L4				3F			–	–	–80.0	dB
Balance attenuation R1 Rin → Rout1	BAL-R1	Lin = GND Rin = 0.5 $V_{r.m.s.}$	0D	3F	3F	10	10	–1.5	0	+1.5	dB
Balance attenuation R2 Rin → Rout2	BAL-R2				18			–2.5	–0.5	+1.0	dB
Balance attenuation R3 Rin → Rout3	BAL-R3				10			–15.0	–10.0	–5.0	dB
Balance attenuation R4 Rin → Rout4	BAL-R4				01			–	–	–80.0	dB

Electrical Characteristics (3/5)

(Unless otherwise specified, V_{CC} = 12 V, T_A = 25 °C, RH ≤ 70%, f = 1 kHz, V_{IN} = 0.5 $V_{r.m.s.}$, no load)

Parameter	Symbol	Test Condition	Subaddress Data					Rating			Unit
			00	01	02	03	04	MIN.	TYP.	MAX.	
Tone control, bass characteristic Lin → Lout1	BASS-L1	f = 100 Hz Lin = 0.5 $V_{r.m.s.}$ Rin = GND	0D	3F	20	1F	10	7.0	10.0	13.0	dB
Tone control, bass characteristic Lin → Lout2	BASS-L2					10		–2.0	0	+2.0	dB
Tone control, bass characteristic Lin → Lout3	BASS-L3					01		–13.0	–10.0	–7.0	dB
Tone control, bass characteristic deviation Rin → Rout1/Lout1	BASS-RL1	f = 100 Hz, Lin = GND Rin = 0.5 $V_{r.m.s.}$ Difference from BASS-L1	0D	3F	20	1F	10	–1.0	0	+1.0	dB
Tone control, bass characteristic deviation Rin → Rout2/Lout2	BASS-RL2	f = 100 Hz, Lin = GND Rin = 0.5 $V_{r.m.s.}$ Difference from BASS-L2				10		–1.0	0	+1.0	dB
Tone control, bass characteristic deviation Rin → Rout3/Lout3	BASS-RL3	f = 100 Hz, Lin = GND Rin = 0.5 $V_{r.m.s.}$ Difference from BASS-L3				01		–1.0	0	+1.0	dB
Tone control, treble characteristic Lin → Lout1	TREB-L1	f = 10 kHz Lin = 0.5 $V_{r.m.s.}$ Rin = GND	0D	3F	20	10	1F	7.0	10.0	13.0	dB
Tone control, treble characteristic Lin → Lout2	TREB-L2						10	–2.0	0	+2.0	dB
Tone control, treble characteristic Lin → Lout3	TREB-L3						01	–13.0	–10.0	–7.0	dB
Tone control, treble characteristic deviation Rin → Rout1/Lout1	TREB-RL1	f = 10 kHz, Lin = GND Rin = 0.5 $V_{r.m.s.}$ Difference from TREB-L1	0D	3F	20	10	1F	–1.0	0	+1.0	dB
Tone control, treble characteristic deviation Rin → Rout2/Lout2	TREB-RL2	f = 10 kHz, Lin = GND Rin = 0.5 $V_{r.m.s.}$ Difference from TREB-L2					10	–1.0	0	+1.0	dB
Tone control, treble characteristic deviation Rin → Rout3/Lout3	TREB-RL3	f = 10 kHz, Lin = GND Rin = 0.5 $V_{r.m.s.}$ Difference from TREB-L3					01	–1.0	0	+1.0	dB

Electrical Characteristics (4/5)

(Unless otherwise specified, V_{CC} = 12 V, T_A = 25 °C, RH ≤ 70%, f = 1 kHz, V_{IN} = 0.5 $V_{r.m.s.}$, no load)

Parameter	Symbol	Test Condition	Subaddress Data					Rating			Unit
			00	01	02	03	04	MIN.	TYP.	MAX.	
Surround voltage gain, music mode Lin → Lout	MUS-L	f = 1 kHz Lin = 0.5 $V_{r.m.s.}$ Rin = GND	05	3F	20	10	10	3.5	5.5	7.5	dB
Surround voltage gain, music mode Lin → Rout	MUS-R							–2.5	–0.5	+1.5	dB
Surround voltage gain, movie mode Lin → Lout	MOV-L	f = 1 kHz Lin = 0.5 $V_{r.m.s.}$ Rin = GND	09	3F	20	10	10	3.0	7.0	11.0	dB
Surround voltage gain, movie mode Lin → Rout	MOV-R							0	4.0	8.0	dB
Surround voltage gain, simulated mode LRin → Lout1	SIM-L1	f = 250 Hz Lin = 0.5 $V_{r.m.s.}$ Rin = 0.5 $V_{r.m.s.}$	01	3F	20	10	10	–0.5	+3.5	+6.5	dB
Surround voltage gain, simulated mode LRin → Lout2	SIM-L2	f = 1 kHz Lin = 0.5 $V_{r.m.s.}$ Rin = 0.5 $V_{r.m.s.}$						–	–3.0	+4.5	dB
Surround voltage gain, simulated mode LRin → Lout3	SIM-L3	f = 4 kHz Lin = 0.5 $V_{r.m.s.}$ Rin = 0.5 $V_{r.m.s.}$						2.0	6.0	10.0	dB
Surround voltage gain, simulated mode LRin → Rout1	SIM-R1	f = 250 Hz Lin = 0.5 $V_{r.m.s.}$ Rin = 0.5 $V_{r.m.s.}$	01	3F	20	10	10	–	–5.5	–1.0	dB
Surround voltage gain, simulated mode LRin → Rout2	SIM-R2	f = 1 kHz Lin = 0.5 $V_{r.m.s.}$ Rin = 0.5 $V_{r.m.s.}$						0	3.0	6.0	dB
Surround voltage gain, simulated mode LRin → Rout3	SIM-R3	f = 4 kHz Lin = 0.5 $V_{r.m.s.}$ Rin = 0.5 $V_{r.m.s.}$						–	–7.0	+5.0	dB

Remark For the surround mode, refer to **4.3 Surround Function**.

Electrical Characteristics (5/5)

(Unless otherwise specified, V_{CC} = 12 V, T_A = 25 °C, RH ≤ 70%, f = 1 kHz, V_{IN} = 0.5 $V_{r.m.s.}$, no load)

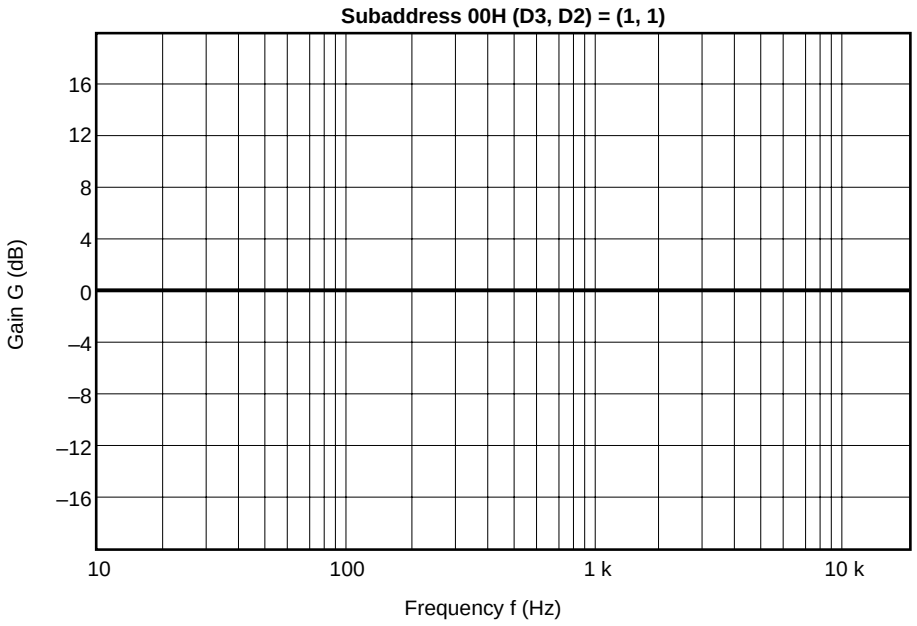
Parameter	Symbol	Test Condition	Subaddress Data					Rating			Unit
			00	01	02	03	04	MIN.	TYP.	MAX.	
Output selector, DC offset Lin → Lout	OFST LRL	No signal Voltage conversion of Lout Lout: L output → R output	1D ↓ 2D	3F	20	10	10	–100	0	+100	mV
Output selector, DC offset Lin → Lout	OFST LL + RL	No signal Voltage conversion of Lout Lout: L output → L+R output	1D ↓ 3D					–100	0	+100	mV
Output selector, DC offset Rin → Lout	OFST RL + RL	No signal Voltage conversion of Lout Lout: R output → L+R output	2D ↓ 3D					–100	0	+100	mV
Output selector, DC offset Rin → Rout	OFST RLR	No signal Voltage conversion of Rout Rout: R output → L output	2D ↓ 1D	3F	20	10	10	–100	0	+100	mV
Output selector, DC offset Rin → Rout	OFST RL + RR	No signal Voltage conversion of Rout Rout: R output → L+R output	2D ↓ 3D					–100	0	+100	mV
Output selector, DC offset Lin → Rout	OFST LL + RR	No signal Voltage conversion of Rout Rout: L output → L+R output	1D ↓ 3D					–100	0	+100	mV

6. CHARACTERISTIC CURVES

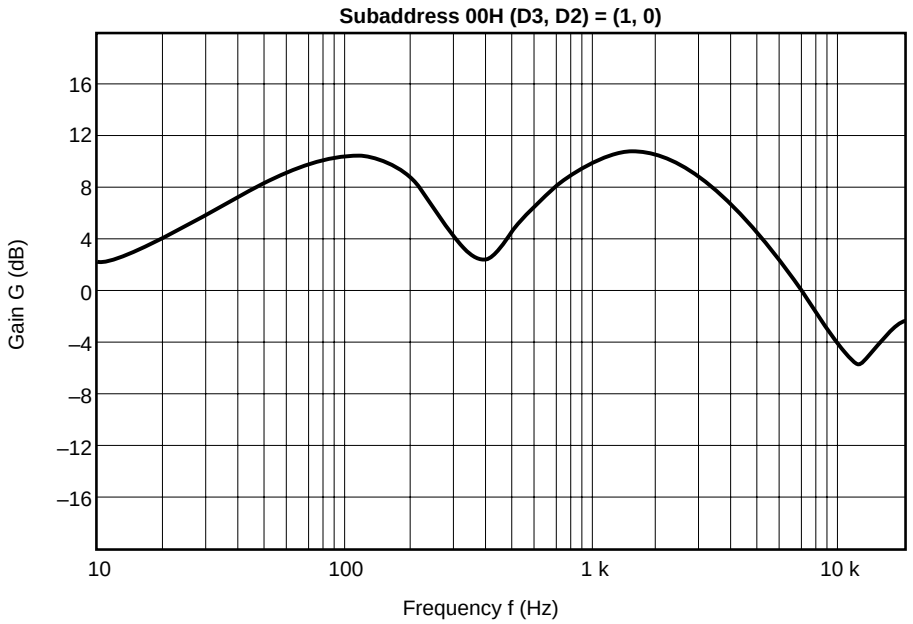
6.1 Frequency Characteristic in Each Mode

V_{CC} = 12 V, V_{IN} = 0.5 $V_{r.m.s.}$
Stereo mode: subaddress 00H (D5, D4) = (0,0)
Surround effect (0 dB attenuation): subaddress 00H (D1, D0) = (0,0)

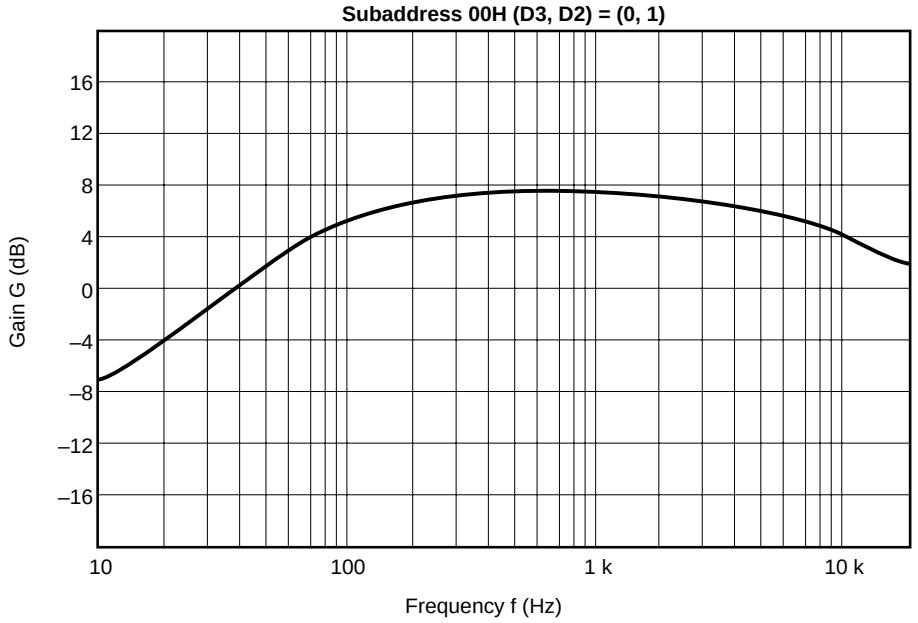
(1) OFF mode Lch/Rch



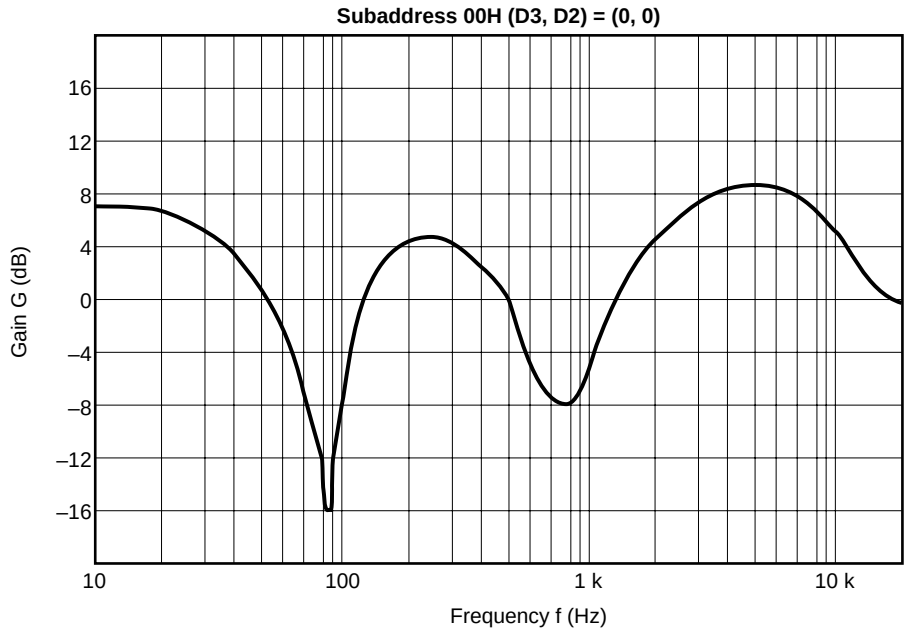
(2) Movie mode Lch/Rch



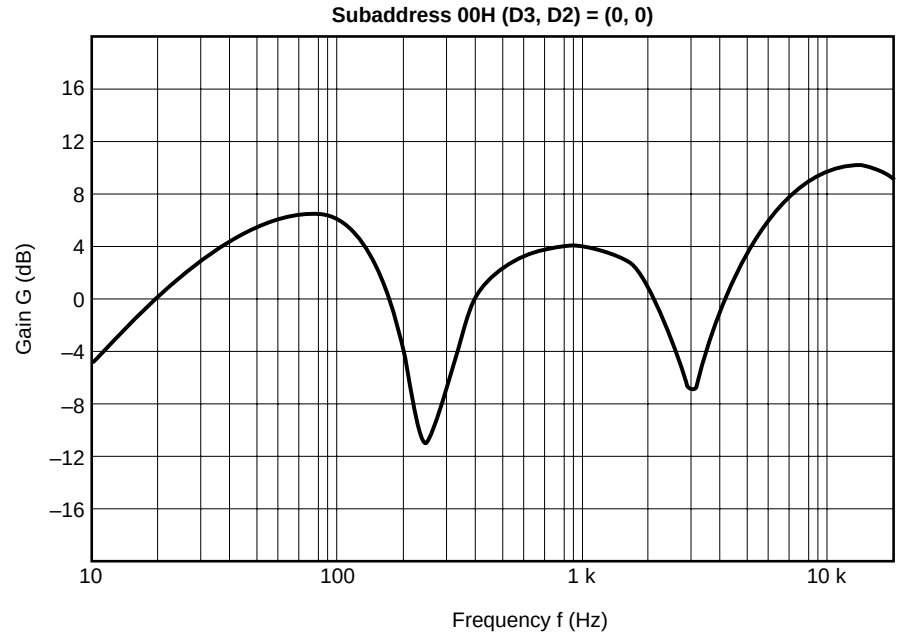
(3) Music mode Lch/Rch



(4) Simulated mode Lch



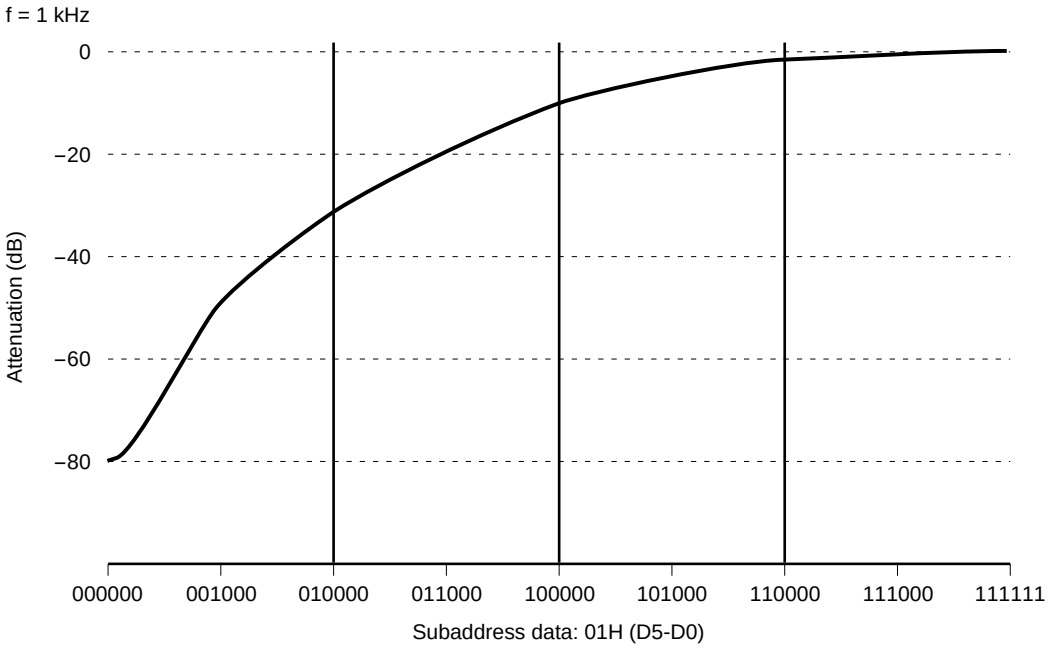
(5) Simulated mode Rch



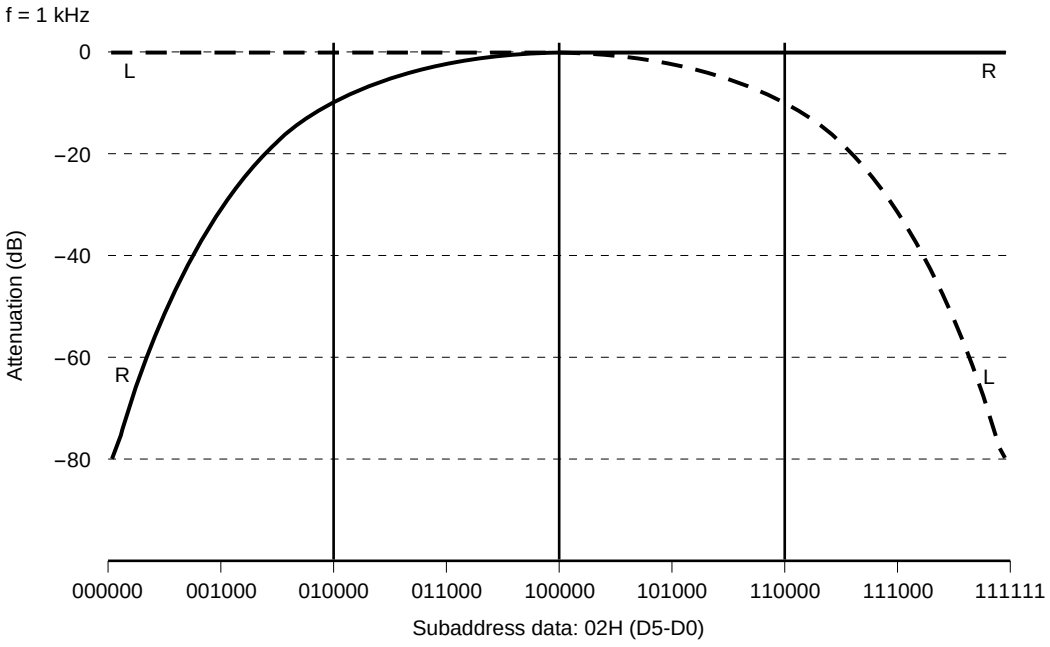
6.2 Control Characteristic

V_{CC} = 12 V, V_{IN} = 0.5 $V_{r.m.s}$
Surround mode (OFF): subaddress 00H (D3, D2) = (1, 1)

(1) Volume control characteristic

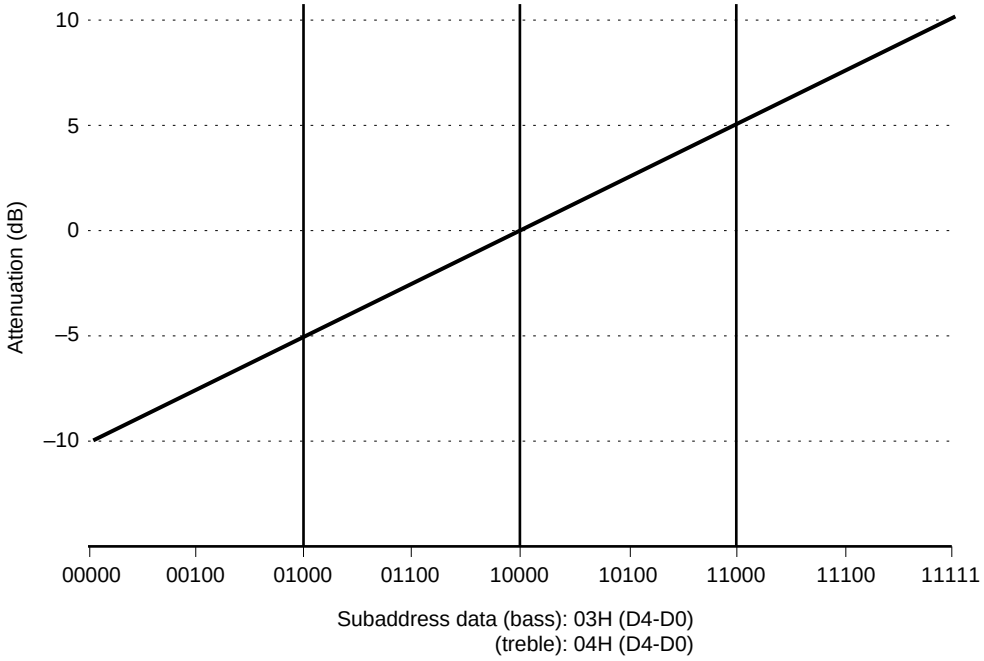


(2) Balance control characteristic

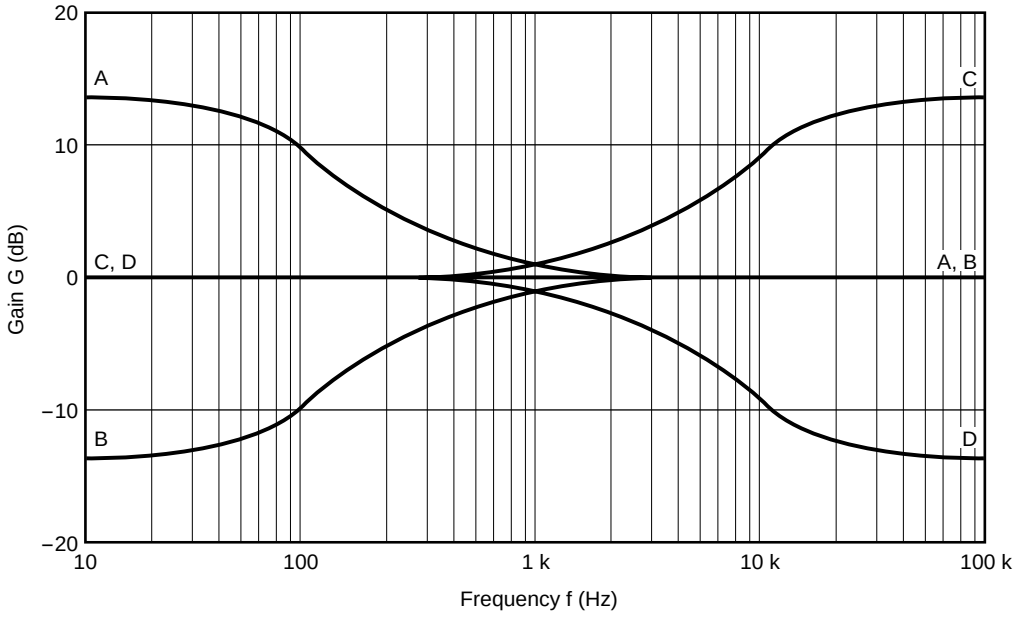


(3) Tone control characteristic (bass/treble)

Bass: f = 100 Hz, treble: f = 10 kHz



(4) Tone frequency characteristic



Curve	Subaddress	Data (D4-D0)
A	03H	11111
B		00001
C	04H	11111
D		00001

6.3 I/O Characteristic

Vcc = 12 V

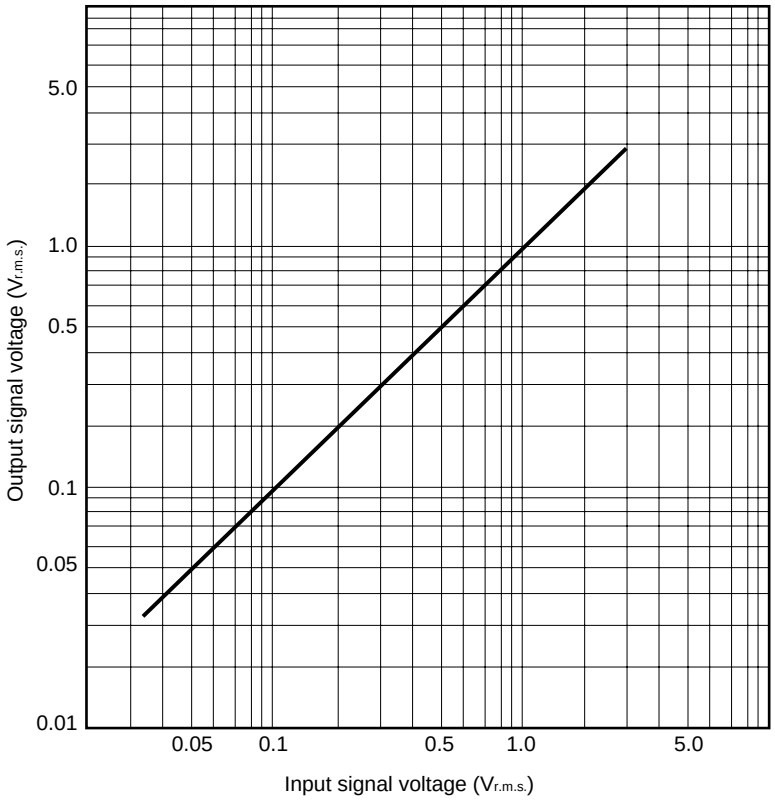
Volume (MAX.) : Subaddress 01H (D5-D0) = (111111)

Balance (center) : Subaddress 02H (D5-D0) = (100000)

Bass (FLAT) : Subaddress 03H (D4-D0) = (10000)

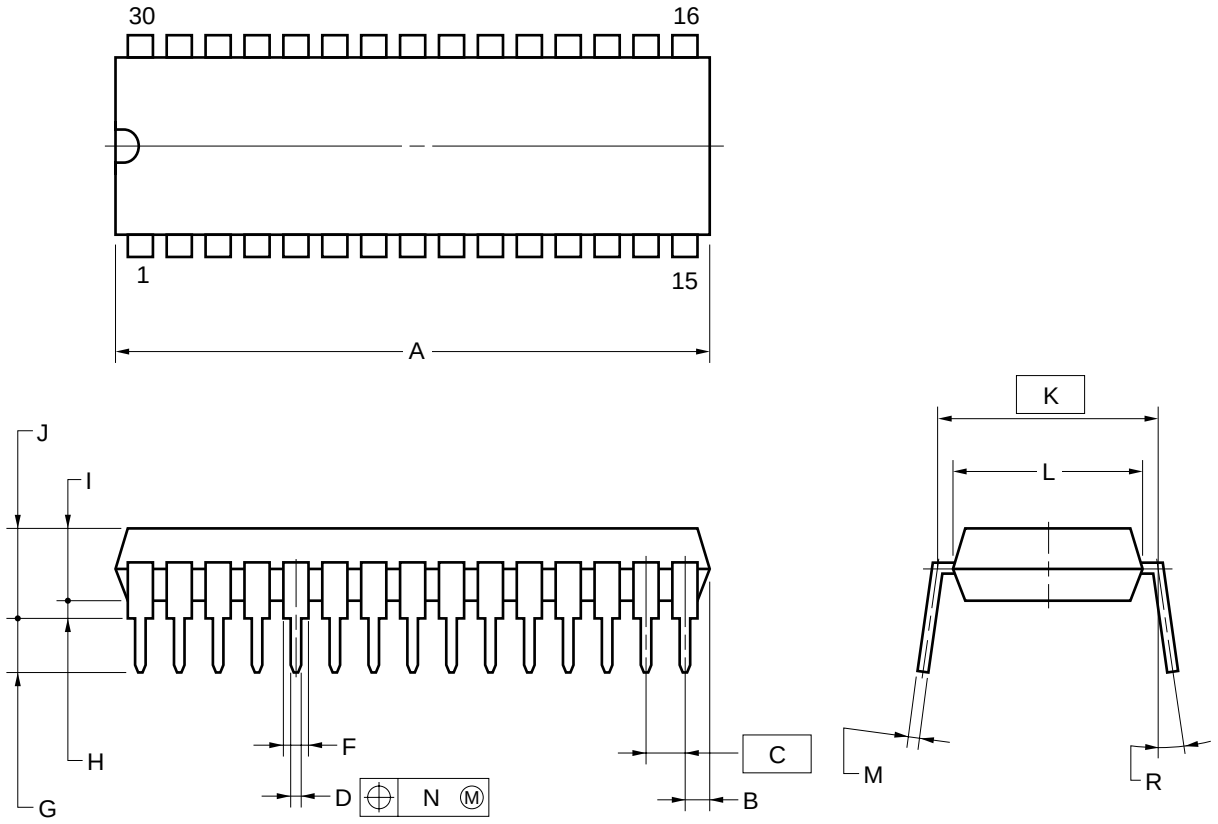
Treble (FLAT) : Subaddress 04H (D4-D0) = (10000)

Surround mode (OFF) : Subaddress 00 (D3, D2) = (1, 1)



7. PACKAGE DRAWING

30 PIN PLASTIC SHRINK DIP (400 mil)



NOTES

1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
3. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	27.3±0.2	$1.075^{+0.008}_{-0.009}$
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	1.0±0.15	$0.039^{+0.007}_{-0.006}$
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	3.45±0.2	$0.136^{+0.008}_{-0.009}$
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6±0.2	$0.339^{+0.008}_{-0.009}$
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

S30C-70-400B-2

8. RECOMMENDED SOLDERING CONDITIONS

It is recommended to solder this product under the conditions described below.

For details of the recommended soldering conditions, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended, consult NEC.

Soldering condition of through-hole type

μPC1857ACT: 30-pin plastic shrink DIP (400 mil)

Soldering Method	Soldering Condition
Wave soldering (only pins)	Soldering bath temperature: 260 °C MAX., Time: 10 seconds
Partial heating	Pin temperature: 300 °C MAX., Time: 3 seconds MAX. (per pin)

Caution Apply wave soldering only to the pins, and exercise care that solder does not directly contact the package.

[MEMO]

[MEMO]

[MEMO]

Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

EEPROM is a trademark of NEC Corp.

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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