# NEC

## 4-BIT SINGLE-CHIP MICROCOMPUTER

The $\mu$PD75P216A is a One-Time PROM version of the $\mu$PD75216A. The $\mu$PD75P216A is suitable for small-scale production or experimental production in system development.

**Also see documents for the $\mu$PD75216A.**

### FEATURES

- The $\mu$PD75216A compatible
- 16256 ✕ 8 bits of on-chip one-time PROM
- Port 6 without pull-down resistor
- High voltage output for display
  S0 to S8, T0 to T9:  On-chip load resistor
  S9, T10 to T15:        Open drain
- Power-on reset circuit is not available
- Single power supply (5 V $\pm$ 10 %)
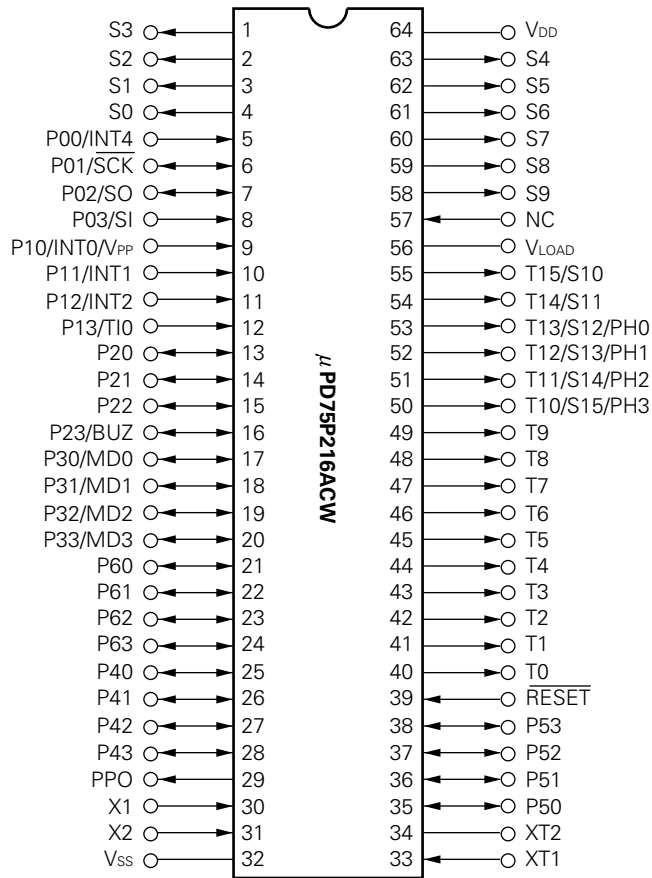
### ORDERING INFORMATION

| Part Number | Package | Quality Grade |
|---|---|---|
| $\mu$PD75P216ACW | 64-pin plastic shrink DIP (750 mil) | Standard |

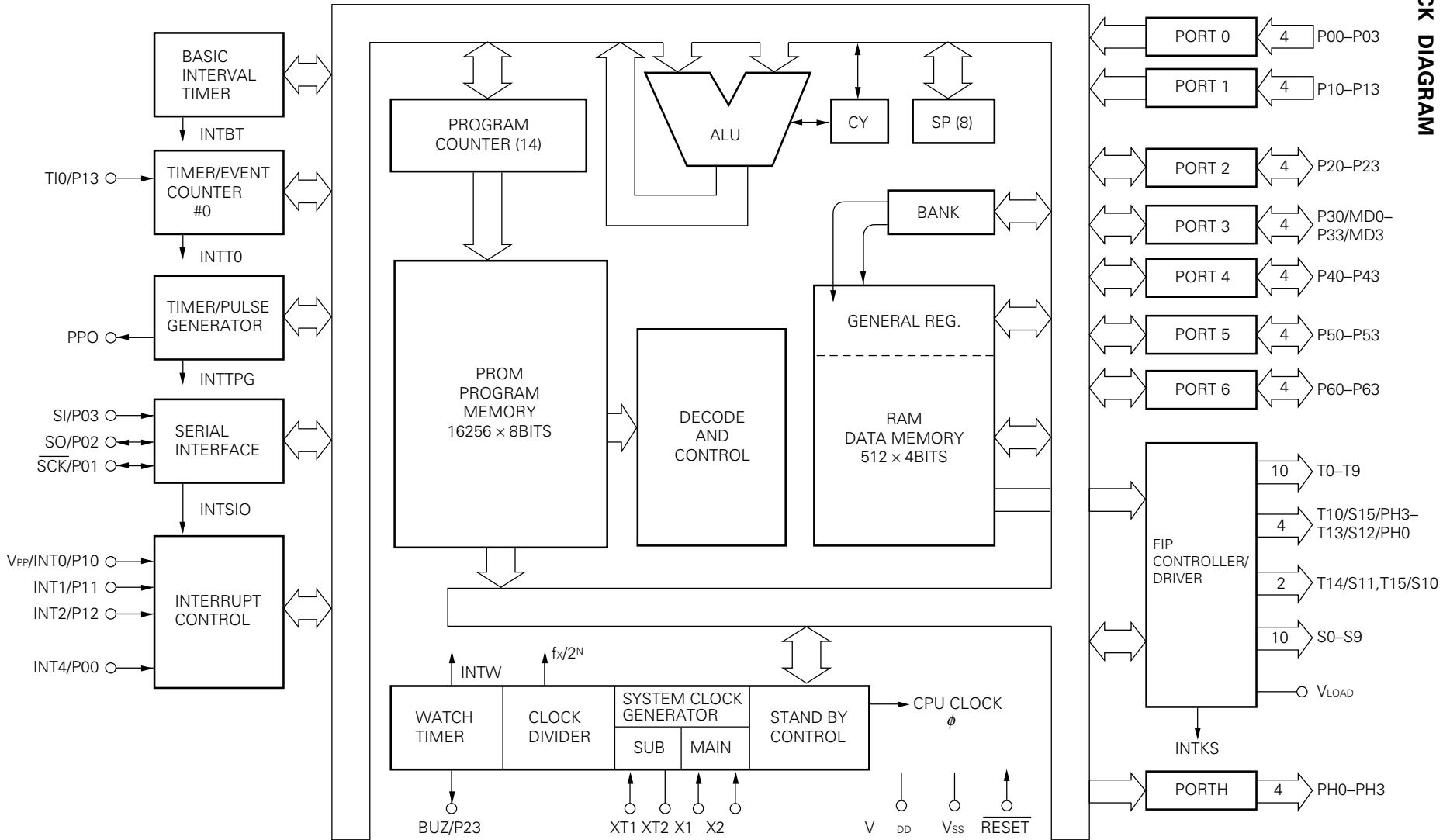**Caution   Pull-up resistor mask options are not available.**

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

**The information in this document is subject to change without notice.**

The mark ★ shows revised points.

**PIN CONFIGURATION (Top View)**

| Pin | | | Pin | |
|---|---|---|---|---|
| S3 | 1 | | 64 | V$_{DD}$ |
| S2 | 2 | | 63 | S4 |
| S1 | 3 | | 62 | S5 |
| S0 | 4 | | 61 | S6 |
| P00/INT4 | 5 | | 60 | S7 |
| P01/$\overline{SCK}$ | 6 | | 59 | S8 |
| P02/SO | 7 | | 58 | S9 |
| P03/SI | 8 | | 57 | NC |
| P10/INT0/V$_{PP}$ | 9 | | 56 | V$_{LOAD}$ |
| P11/INT1 | 10 | | 55 | T15/S10 |
| P12/INT2 | 11 | | 54 | T14/S11 |
| P13/TI0 | 12 | | 53 | T13/S12/PH0 |
| P20 | 13 | | 52 | T12/S13/PH1 |
| P21 | 14 | | 51 | T11/S14/PH2 |
| P22 | 15 | | 50 | T10/S15/PH3 |
| P23/BUZ | 16 | | 49 | T9 |
| P30/MD0 | 17 | | 48 | T8 |
| P31/MD1 | 18 | | 47 | T7 |
| P32/MD2 | 19 | | 46 | T6 |
| P33/MD3 | 20 | | 45 | T5 |
| P60 | 21 | | 44 | T4 |
| P61 | 22 | | 43 | T3 |
| P62 | 23 | | 42 | T2 |
| P63 | 24 | | 41 | T1 |
| P40 | 25 | | 40 | T0 |
| P41 | 26 | | 39 | $\overline{RESET}$ |
| P42 | 27 | | 38 | P53 |
| P43 | 28 | | 37 | P52 |
| PPO | 29 | | 36 | P51 |
| X1 | 30 | | 35 | P50 |
| X2 | 31 | | 34 | XT2 |
| V$_{SS}$ | 32 | | 33 | XT1 |

$\mu$**PD75P216ACW**

## CONTENTS

## 1. PIN FUNCTIONS

### 1.1 PORT PINS

| Pin name | Input/output | Shared pin | Function | | 8-bit I/O | When reset | I/O circuit type **Note** |
|---|---|---|---|---|---|---|---|
| P00 | Input | INT4 | 4-bit input port (PORT0). | | × | Input | Ⓑ |
| P01 | I/O | $\overline{\text{SCK}}$ | | | | | Ⓕ |
| P02 | I/O | SO | | | | | Ⓖ |
| P03 | Input | SI | | | | | Ⓑ |
| P10 | Input | INT0/V$_{PP}$ | | With noise elimination function | × | Input | Ⓑ |
| P11 | | INT1 | | With noise elimination function | | | |
| P12 | | INT2 | 4-bit input port (PORT1). | | | | |
| P13 | | TI0 | | | | | |
| P20 | I/O | — | 4-bit I/O port (PORT2). | | × | Input | E |
| P21 | | — | | | | | |
| P22 | | — | | | | | |
| P23 | | BUZ | | | | | |
| P30 - P33 | I/O | MD0 - MD3 | Programmable 4-bit I/O port (PORT3). I/O can be specified bit by bit. | | × | Input | E |
| P40 - P43 | I/O | — | 4-bit I/O port (PORT4). Can directly drive LEDs. Data input/output pins for the PROM write and verify (Four low-order bits). | | ○ | Input | E |
| P50 - P53 | I/O | — | 4-bit I/O port (PORT5). Can directly drive LEDs. Data input/output pins for the PROM write and verify (Four high-order bits). | | ○ | Input | E |
| P60 - P63 | I/O | — | Programmable 4-bit I/O port (PORT6). I/O can be specified bit by bit. Suitable for keyboard input. | | × | Input | E |
| PH0 | Output | T13/S12 | 4-bit P-ch open-drain output port Can withstand high voltage and high current (PORTH) | | × | High impedance | I-D |
| PH1 | | T12/S13 | | | | | |
| PH2 | | T11/S14 | | | | | |
| PH3 | | T10/S15 | | | | | |

**Note** The circle ( ○ ) indicates the Schmitt triggered input.

## 1.2 NON-PORT PINS

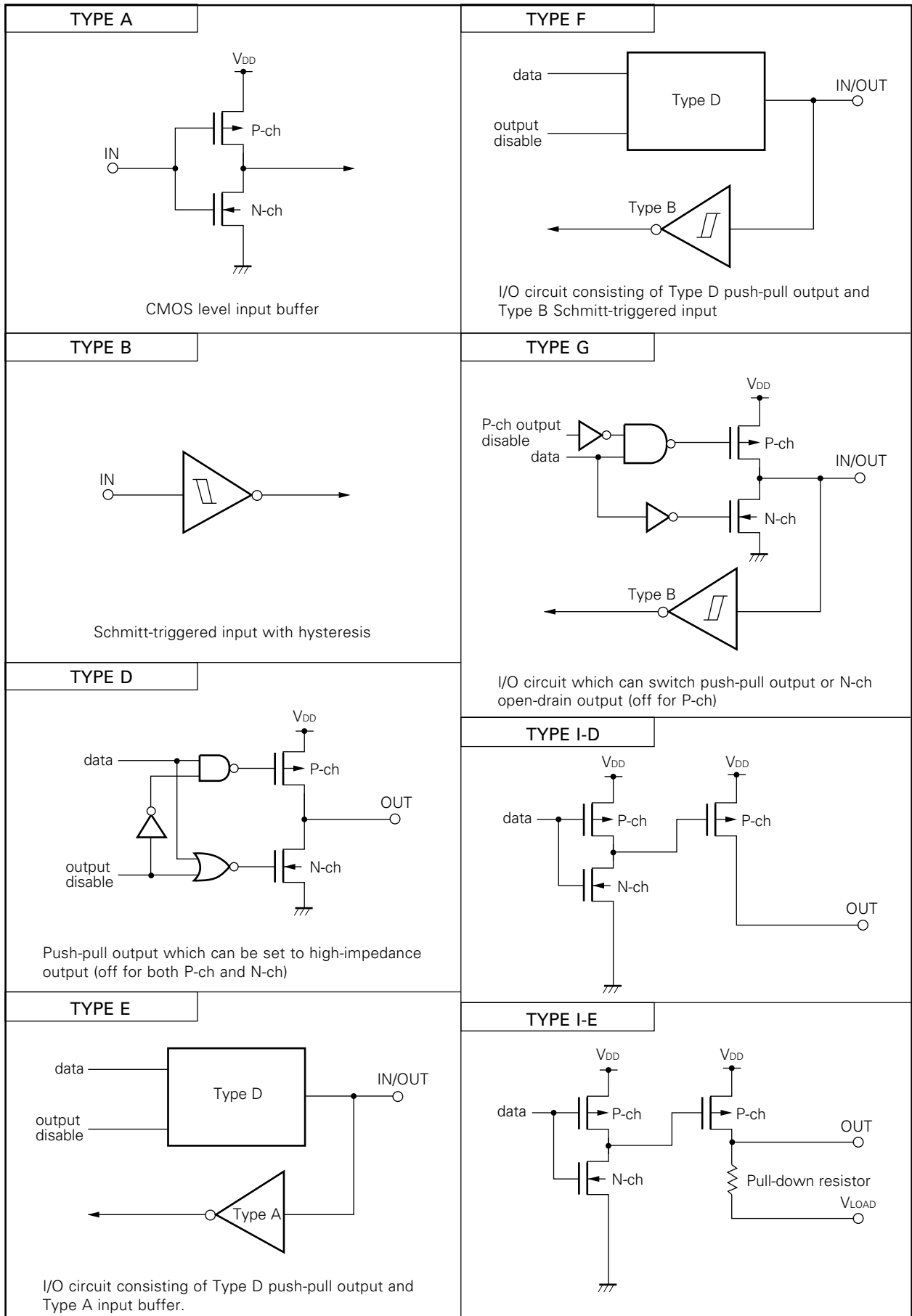| Pin name | Input/output | Shared pin | Function | | When reset | I/O circuit type Note 1 |
|---|---|---|---|---|---|---|
| T0 - T9 | | — | Note 2 | Used for digit output<br>Can withstand high voltage and high current | Low level | I - E |
| T10/S15 - T13/S12 | Output | PH3-PH0 | | For digit/segment output<br>Can withstand high voltage and high current<br>Unused pin can be used as PORTH. | High impedance | I - D |
| T14/S11, T15/S10 | | | Note 3 | For digit/segment output<br>Can withstand high voltage and high current<br>Static output is possible. | | |
| S9 | | — | | For segment output<br>Can withstand high voltage<br>Static output is possible | | |
| S0 -S8 | | | Note 2 | For segment output<br>Can withstand high voltage | Low level | I - E |
| PPO | Output | — | Pulse output by timer/pulse generator | | High impedance | D |
| TI0 | Input | P13 | External event pulse input to timer event counter | | | Ⓑ |
| $\overline{SCK}$ | I/O | P01 | Input and output to serial clock | | Input | Ⓕ |
| SO | I/O | P02 | Serial data output or serial data input and output | | Input | Ⓖ |
| SI | Input | P03 | Serial data input or normal input | | Input | Ⓑ |
| INT4 | Input | P00 | Edge detection vectored interrupt input<br>(detected at both rising edge and falling edge) | | — | Ⓑ |
| INT0 | Input | P10/V$_{PP}$ | Edge detection vectored interrupt input with noise elimination function (edge-detection selectable) | | — | Ⓑ |
| INT1 | | P11 | | | — | |
| INT2 | Input | P12 | Testable input for edge-detection<br>(detected at rising edge) | | — | Ⓑ |
| BUZ | I/O | P23 | Fixed frequency output<br>(For buzzer or system clock trimming) | | Input | E |
| X1, X2 | Input | — | Crystal/ceramic resonator connection for main system clock generation. When external clock signal is used, it is applied to X1, and its reverse phase signal is applied to X2. | | — | — |
| XT1 | Input | — | Crystal connection for subsystem clock generation. When external clock signal is used, it is applied to XT1 and XT2 is open. | | — | — |
| XT2 | — | | | | — | |
| $\overline{RESET}$ | Input | — | System reset input (low-level active) | | — | Ⓑ |
| MD0 - MD3 | I/O | P30 - P33 | Operation mode selection during the PROM write/verify cycles. | | — | E |
| V$_{PP}$ | | P10/INT0 | +12.5 V is applied as the programming voltage during the PROM write/verify cycles | | — | Ⓑ |
| V$_{LOAD}$ | | — | Pull-down resistor connection of FIP controller/driver | | — | I - E |
| V$_{DD}$ | | — | Positive power supply<br>+6 V is applied as the programming voltage during the PROM write/verify cycles | | — | — |
| V$_{SS}$ | | — | GND potential | | — | — |
| NC Note 4 | | — | No connection | | — | — |

**Note 1.** The circle (○) indicates the Schmitt triggered input.
    **2.** Pull-down resistor is incorporated.
    **3.** Open-drain output
    **4.** NC pin should be connected to V$_{PRE}$ when sharing print board with the μPD75216A.

**Fig. 1-1  Pin Input/Output Circuit**



**TYPE A**

CMOS level input buffer

**TYPE B**

Schmitt-triggered input with hysteresis

**TYPE D**

Push-pull output which can be set to high-impedance output (off for both P-ch and N-ch)

**TYPE E**

I/O circuit consisting of Type D push-pull output and Type A input buffer.

**TYPE F**

I/O circuit consisting of Type D push-pull output and Type B Schmitt-triggered input

**TYPE G**

I/O circuit which can switch push-pull output or N-ch open-drain output (off for P-ch)

**TYPE I-D**

**TYPE I-E**

## 1.3 TREATMENT OF UNUSED PINS

**Table 1-2   Recommended Connection for Unused Pins**

| Pin | Recommended connection |
|---|---|
| P00/INT4 | Connect to $V_{SS}$ |
| P01/$\overline{SCK}$ | Connect to $V_{SS}$ or $V_{DD}$ |
| P02/SO | |
| P03/SI | |
| P10/INT0/$V_{PP}$ | Connect to $V_{SS}$ |
| P11/INT1, P12/INT2 | |
| P13/T10 | |
| P20 - P22 | Input: Connect to $V_{SS}$ or $V_{DD}$<br>Output: Open |
| P23/BUZ | |
| P30/MD0 - P33/MD3 | |
| P40 - P43 | |
| P50 - P53 | |
| P60 - P63 | |
| PPO | Open |
| S0 - S9 | |
| T15/S10, T14/S11 | |
| T0 - T9 | |
| T10/S15/PH3-T13/S12/PH0 | |
| XT1 | Connect to $V_{SS}$ or $V_{DD}$ |
| XT2 | Open |

## 2.  DIFFERENCES  BETWEEN  THE  μPD75P216A  AND  THE  μPD75216A,  μPD75208

**Table 2-1    Differences between the μPD75P216A and the μPD75216A, μPD75208**

| Parameter | | μPD75P216A | μPD75216A | μPD75208 |
|---|---|---|---|---|
| ROM | | One-time PROM | Mask ROM | |
| | | 16256 × 8 bits (0000H – 3F7FH) | | 8064 × 8 bits (0000H – 1F7FH) |
| RAM | | 512 × 4 bits | | 497 × 4 bits |
| FIP® Controller Driver | | 9 – 16 segments | | 9 – 12 segments |
| Pull-Down Registor | Port 6 | N/A | Mask option | |
| | S0 – S8, T0 – T9 | On-chip | | |
| | S9, T10 – T15 | N/A (Open-drain) | | |
| Power-On Reset | | N/A | Mask option | |
| Power-On Flag | | | | |
| Pin Connection | | P10/INT0/$V_{PP}$ | P10/INT0 | |
| | | P30/MD0 – P33/MD3 | P30 – P33 | |
| | | NC | $V_{PRE}$ | |
| Operating Ambient Temperature | | –10 to +70 °C | –40 to +85 °C | |
| Operating Supply Voltage | | 5 V ± 10 % | 2.7 to 6.0 V | |
| Package | | 64-pin plastic shrink DIP (750 mil) | 64-pin plastic shrink DIP (750 mil) 64-pin plastic QFP (14 × 20 mm) | |

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## 3. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY

The *µ*PD75P216A contains $16256 \times 8$ bits of one-time PROM available of writing. The following table shows the pin functions during the write and verify cycles. Note that it is not necessary to enter an address, because the address is updated by pulsing the X1 clock pins.

**Table 3-1    Used Pin at PROM Write and Verify**

| Pin name | Function |
|---|---|
| V$_{PP}$ | Voltage application pin for write and verify (Normally V$_{DD}$ potential) |
| X1, X2 | Address-update clock input during write/verify. The inverted signal of the X1 should be input to the X2. |
| MD0 - MD3 | Operation mode selection pins for write and verify |
| P40 - P43 (lower 4 bits) P50 - P53 (higher 4 bits) | 8-bit data input/output pins for write and verify |
| V$_{DD}$ | Supply voltage application pin Normally 5 V $\pm$ 10 %; 6 V is applied during write/verify |

**Caution 1.  The pins which are not used during write or verify should be treated as follows**

- **Port, XT1, $\overline{\text{RESET}}$ ... Connect to V$_{SS}$ through pull-down resistors**
- **S0 to S9, T0 to T15, PPO, V$_{LOAD}$ ... Connect to V$_{DD}$ through pull-up resistors**
- **XT2 ... Open**

**2.  The *µ*PD75P216A do not have a UV erase window, thus the PROM contents cannot be erased with ultra violet ray.**

### 3.1  PROM WRITE AND VERIFY OPERATION

When +6 V and +12.5 V are applied to the V$_{DD}$ and V$_{PP}$ pins, respectively, the PROM is placed in the write/verify mode. The operation is selected by the MD0 to MD3 pins, as shown in the table.

**Table 3-2    PROM Write and Verify Operation**

| Operation mode specification | | | | | | Operation mode |
|---|---|---|---|---|---|---|
| V$_{PP}$ | V$_{DD}$ | MD0 | MD1 | MD2 | MD3 | |
| +12.5 | +6 V | H | L | H | L | Clear program memory address to 0 |
| | | L | H | H | H | Write mode |
| | | L | L | H | H | Verify mode |
| | | H | $\times$ | H | H | Program inhibit mode |

$\times$: Don't care.

**3.2 PROM WRITE PROCEDURE**

PROM can be written at high speed using the following procedure: (see the following figure)

(1)   Pull unused pins to Vss through resistors. Set the X1 pin low.

(2)   Supply 5 volts to the VDD and VPP pins.

(3)   Wait for 10 *μ*s.

(4)   Select the zero clear program memory address mode.

(5)   Supply 6 volts to the VDD and 12.5 volts to the VPP pins.

(6)   Select the program inhibit mode.

(7)   Write data in the 1 ms write mode.

(8)   Select the program inhibit mode.

(9)   Select the verify mode. If the data is correct, proceed to step (10). If not repeat steps (7), (8) and (9).

(10)  Perform one additional write (duration of 1ms × number of writes at (7) to (9)).

(11)  Select the program inhibit mode.

(12)  Apply four pulses to the X1 pin to increment the program memory address by one.

(13)  Repeat steps (7) to (12) until the end address is reached.

(14)  Select the zero clear program memory address mode.

(15)  Return the VDD and VPP pins back to + 5 volts.

(16)  Turn off the power.

**Fig. 3-1   Timing of Program Memory Write**
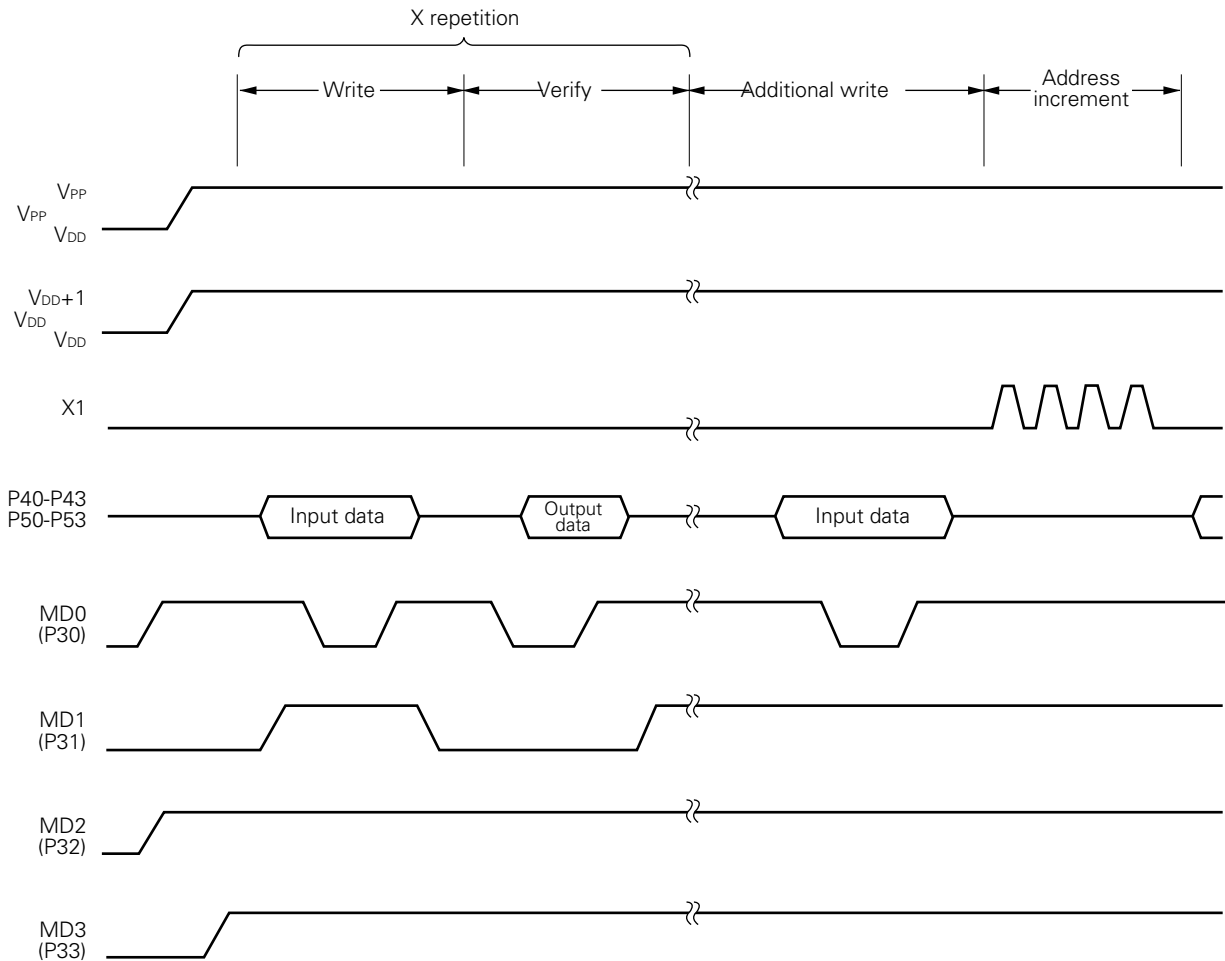
**3.3 PROM READ PROCEDURE**

The PROM contents can be read in the verify mode by using the following procedure: (see the following figure)

(1)   Pull unused pins to Vss through resistors. Set the X1 pin low.

(2)   Supply 5 volts to the VDD and VPP pins.

(3)   Wait for 10 $\mu$s.

(4)   Select the zero clear program memory address mode.

(5)   Supply 6 volts to the VDD and 12.5 volts to the VPP pins.

(6)   Select the program inhibit mode.

(7)   Select the verify mode. Apply four pulses to the X1 pin. Every four clock pulses will output the data stored in one address.

(8)   Select the program inhibit mode.

(9)   Select the zero clear program memory address mode.

(10) Return the VDD and VPP pins back to + 5 volts.

(11) Turn off the power.

**Fig. 3-2   Timing of Program Memory Read**
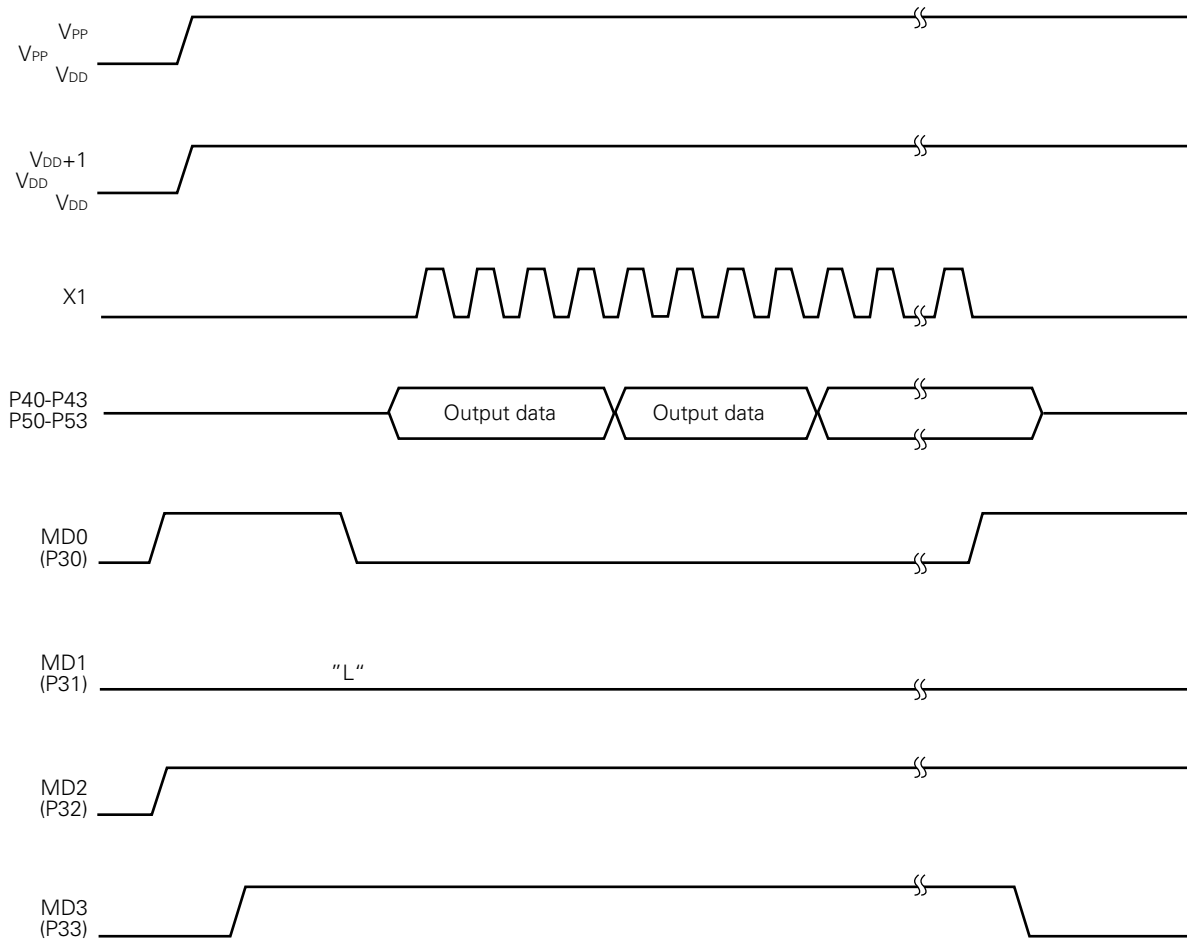
## 4. ELECTRICAL SPECIFICATIONS

**Absolute Maximum Ratings (T$_a$ = 25 °C)**
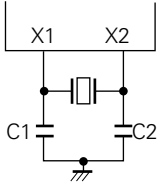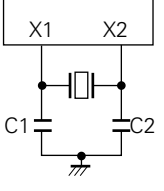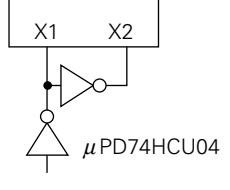
| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | V$_{DD}$ | | −0.3 to +7.0 | V |
| | V$_{LOAD}$ | | V$_{DD}$ −40 to V$_{DD}$ + 0.3 | V |
| | V$_{PP}$ | | −0.3 to +13.5 | V |
| Input voltage | V$_I$ | | −0.3 to V$_{DD}$ +0.3 | V |
| Output voltage | V$_O$ | Other than display pins | −0.3 to V$_{DD}$ +0.3 | V |
| | V$_{OD}$ | Display pins | V$_{DD}$ −40 to V$_{DD}$ + 0.3 | V |
| High-level output current | I$_{OH}$ | Single pin; other than display pins | −15 | mA |
| | | Single pin; S0 – S9 | −15 | mA |
| | | Single pin; T0 – T15 | −30 | mA |
| | | Total of all pins other than diplay | −20 | mA |
| | | Total of all display pins | −120 | mA |
| Low level output current | I$_{OL}$ | Single pin | 17 | mA |
| | | Total of all pins | 60 | mA |
| Operating temperature | T$_{opt}$ | | −10 to +70 | °C |
| Storage temperature | T$_{stg}$ | | −65 to +150 | °C |

**Operating Supply Voltage (T$_a$ = −10 to + 70 °C)**
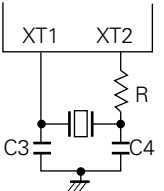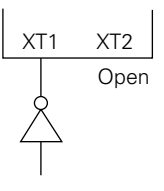
| Parameter | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|
| CPU [Note] | | 4.5 | 5.5 | V |
| Display controller | | 4.5 | 5.5 | V |
| Timer/pulse generator | | 4.5 | 5.5 | V |
| Other hardwares [Note] | | 4.5 | 5.5 | V |

**Note** Except system clock oscillation circuit, display controller, timer/pulse generator.

**Main System Clock Configurations (T$_a$ = –10 to +70 °C, V$_{DD}$ = 5 V ± 10 %)**

| Resonator | Recommended constants | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Ceramic resonator | X1  X2<br>C1  C2 | Oscillation frequency (f$_{XX}$) Note 1 | V$_{DD}$ = Oscillator operating voltage range | 2.0 | | 5.0 Note 3 | MHz |
| | | Oscillation stabilization time Note 2 | After V$_{DD}$ reaches the minimum oscillator operating voltage range | | | 4 | ms |
| Crystal resonator | X1  X2<br>C1  C2 | Oscillation frequency (f$_{XX}$) Note 1 | | 2.0 | 4.19 | 5.0 Note 3 | MHz |
| | | Oscillation stabilization time Note 2 | | | | 10 | ms |
| External clock | X1  X2<br>µPD74HCU04 | X1 input frequency (f$_X$) Note 1 | | 2.0 | | 5.0 Note 3 | MHz |
| | | X1 input high- and low-level width (t$_{XH}$, t$_{XL}$) | | 100 | | 250 | ns |

**Subsystem Clock Configurations (T$_a$ = –10 to +70 °C, V$_{DD}$ = 5 V ± 10 %)**

| Resonator | Recommended constants | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Crystal resonator | XT1  XT2  R<br>C3  C4 | Oscillation frequency (f$_{XT}$) Note 1 | | 32 | 32.768 | 35 | kHz |
| | | Oscillation stabilization time Note 2 | | | 1 | 2 | s |
| External clock | XT1  XT2  Open | XT1 input frequency (f$_{XT}$) | | 32 | | 100 | kHz |
| | | X1 input high- and low-level width (t$_{XTH}$, t$_{XTL}$) | | 10 | | 32 | µs |

**Note 1.** The oscillation frequency and input frequency only indicate the characteristics of the oscillation circuit.  Refer to the AC characteristics for the instruction execution time.

**2.** The oscillation stabilization time is the time until the oscillation enters a stable state after the application of V$_{DD}$ or the release of STOP mode.

★ **3.** When the oscillation frequency is 4.19 < f$_X$ ≤ 5.0 MHz, PCC = 0011 should not be selected as the instruction execution time. If PCC = 0011 is selected, 1 machine cycle is less than the specified minimum value, which is 0.95 µs.

**Capacitance (T$_a$ = 25 °C, V$_{DD}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input capacitance | | C$_{IN}$ | | | | 15 | pF |
| Output capacitance | Other than display output | C$_{OUT}$ | f = 1 MHz Unmeasured pins returned to 0 V | | | 15 | pF |
| | Display output | | | | | 35 | pF |
| Input/Output capacitance | | C$_{IO}$ | | | | 15 | pF |

**DC Characteristics (T$_a$ = –10 to +70 °C, V$_{DD}$ = 5 V $\pm$ 10 %)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-level input voltage | V$_{IH1}$ | All except ports 0, 1, 6, X1, X2, XT1, $\overline{RESET}$ | | 0.7 V$_{DD}$ | | V$_{DD}$ | V |
| | V$_{IH2}$ | Port 0, 1 $\overline{RESET}$ | | 0.75 V$_{DD}$ | | V$_{DD}$ | V |
| | V$_{IH3}$ | X1, X2, XT1 | | V$_{DD}$–0.4 | | V$_{DD}$ | V |
| | V$_{IH4}$ | Port 6 | | 0.65 V$_{DD}$ | | V$_{DD}$ | V |
| Low-level input voltage | V$_{IL1}$ | All except ports 0, 1, 6, X1, X2, XT1, $\overline{RESET}$ | | 0 | | 0.3 V$_{DD}$ | V |
| | V$_{IL2}$ | Port 0, 1, 6 $\overline{RESET}$ | | 0 | | 0.2 V$_{DD}$ | V |
| | V$_{IL3}$ | X1, X2, XT1 | | 0 | | 0.4 | V |
| High-level output voltage | V$_{OH}$ | All outputs | I$_{OH}$ = –1 mA | V$_{DD}$–1.0 | | | V |
| | | | I$_{OH}$ = –100 $\mu$A | V$_{DD}$–0.5 | | | V |
| Low-level output voltage | V$_{OL}$ | Port 4, 5 | I$_{OL}$ = 15 mA | | 0.4 | 2.0 | V |
| | | All outputs | I$_{OL}$ = 1.6 mA | | | 0.4 | V |
| High-level input leakage current | I$_{LIH1}$ | All except X1, X2, XT1 | V$_I$ = V$_{DD}$ | | | 3 | $\mu$A |
| | I$_{LIH2}$ | X1, X2, XT1 | | | | 20 | $\mu$A |
| Low-level input leakage current | I$_{LIL1}$ | All except X1, X2, XT1 | V$_I$ = 0 V | | | –3 | $\mu$A |
| | I$_{LIL2}$ | X1, X2, XT1 | | | | –20 | $\mu$A |
| High-level output leakage current | I$_{LOH}$ | All outputs | V$_O$ = V$_{DD}$ | | | 3 | $\mu$A |
| Low-level output leakage current | I$_{LOL1}$ | All except display output | V$_O$ = 0 V | | | –3 | $\mu$A |
| | I$_{LOL2}$ | Display outputs | V$_O$ = V$_{LOAD}$ = V$_{DD}$ – 35 V | | | –10 | $\mu$A |
| Display output current | I$_{OD}$ | S0 - S9 | V$_{OD}$ = V$_{DD}$ – 2 V | –3 | –5.5 | | mA |
| | | T0 - T15 | | –15 | –22 | | mA |
| On-chip pull-down resistor | R$_L$ | Display outputs | V$_{OD}$ – V$_{LOAD}$ = 35 V | 25 | 70 | 135 | k$\Omega$ |
| Power supply current [Note 1] | I$_{DD1}$ | 4.19 MHz Crystal oscillator C1 = C2 = 15 pF | [Note 2] | | 3.0 | 9.0 | mA |
| | I$_{DD2}$ | | HALT mode | | 600 | 1 800 | $\mu$A |
| | I$_{DD3}$ | 32.768 kHz Crystal oscillator | [Note 3] | | 100 | 300 | $\mu$A |
| | I$_{DD4}$ | | HALT mode | | 40 | 100 | $\mu$A |
| | I$_{DD5}$ | XT1 = 0 V | STOP mode | | 0.5 | 20 | $\mu$A |

**Note 1.** Does not include the current for the on-chip pull-down resistor (output circuit to S0 to S8, T0 to T9).

    **2.** When the processor clock control register (PCC) is set to 0011 and operated in high-speed mode.

    **3.** When the system clock control register (SCC) is set to 1001 to stop the main system clock, and when the sub-system clock is used.

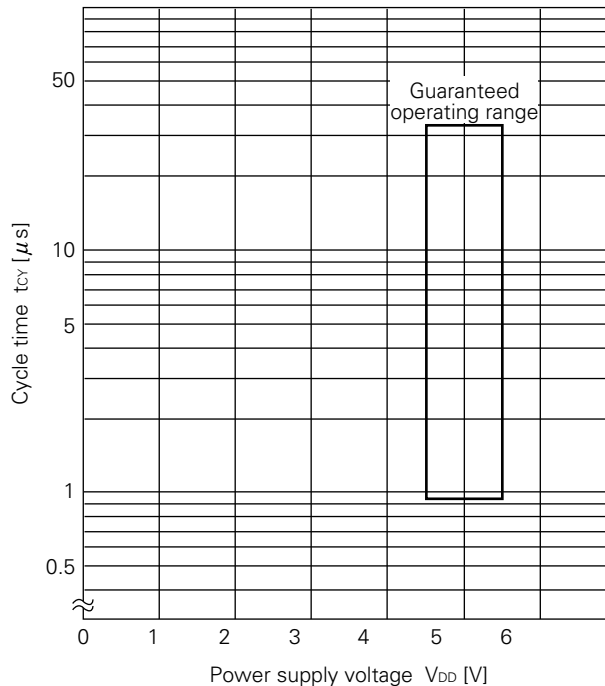**AC Characteristics (T$_a$ = –10 to +70 °C, V$_{DD}$ = +5 V $\pm$10%)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| CPU clock time [Note 1]<br>(minimum instruction<br>execution time = 1 machine cycle) | t$_{CY}$ | Main system clock | | 0.95 | | 32 | $\mu$s |
| | | Subsystem clock | | 114 | 122 | 125 | $\mu$s |
| TI0 input frequency | f$_{TI}$ | | | 0 | | 0.6 | MHz |
| TI0 input high- and low-level width | t$_{TIH}$, t$_{TIL}$ | | | 0.83 | | | $\mu$s |
| $\overline{SCK}$ cycle time | t$_{KCY}$ | | Input | 0.8 | | | $\mu$s |
| | | | Output | 0.95 | | | $\mu$s |
| $\overline{SCK}$ high- and low-level width | t$_{KH}$, t$_{KL}$ | | Input | 0.4 | | | $\mu$s |
| | | | Output | t$_{KCY}$/2-50 | | | ns |
| SI setup time (to $\overline{SCK}$ ↑) | t$_{SIK}$ | | | 100 | | | ns |
| SI hold time (to $\overline{SCK}$ ↑) | t$_{KSI}$ | | | 400 | | | ns |
| $\overline{SCK}$ ↓ → SO output delay time | t$_{KSO}$ | | | | | 300 | ns |
| Interrupt inputs<br>high- and low-level width | t$_{INTH}$,<br>t$_{INTL}$ | | INT0 | [Note 2] | | | $\mu$s |
| | | | INT1 | 2t$_{CY}$ | | | $\mu$s |
| | | | INT2, 4 | 10 | | | $\mu$s |
| $\overline{RESET}$ low-level width | t$_{RSL}$ | | | 10 | | | $\mu$s |

**Note 1.** The CPU clock (ø) cycle time is decided by the oscillation frequency of the resonator, system clock control register (SCC), and processor clock control register (PCC).
The figure to the right indicates cycle time (t$_{CY}$) characteristics for supply voltage V$_{DD}$ when using the main system clock.

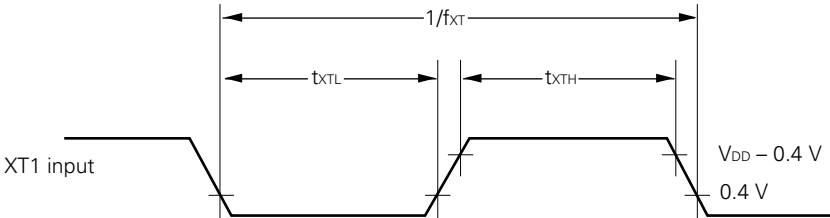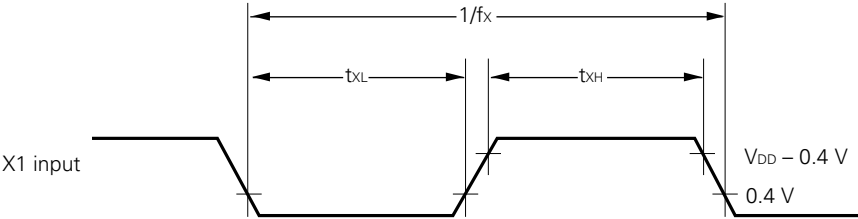**2.** This is 2t$_{CY}$ or 128/f$_{XX}$ according to the interrupt mode register setting (IM0).
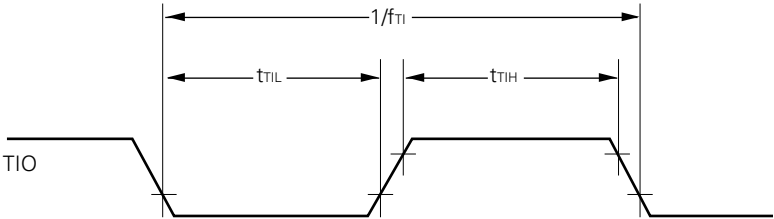
t$_{CY}$ vs V$_{DD}$ (Main system clock)
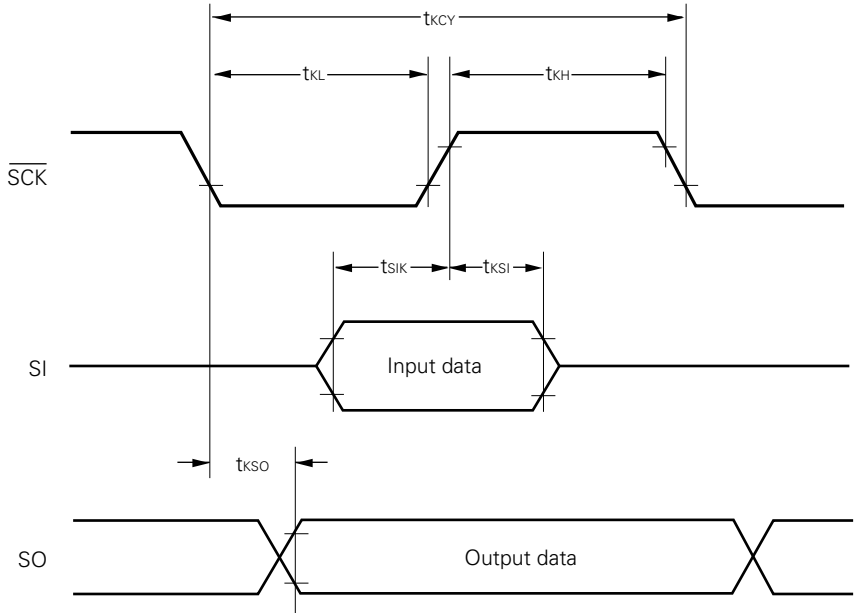
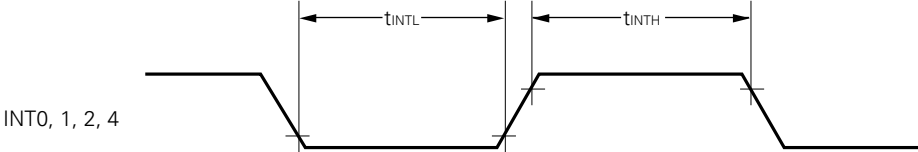**AC timing Test Point (Except X1, XT1)**
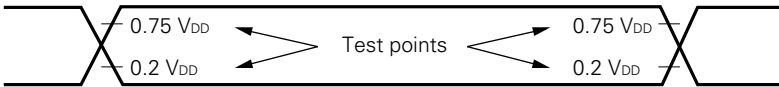


**Clock Timing**



**TIO Timing**

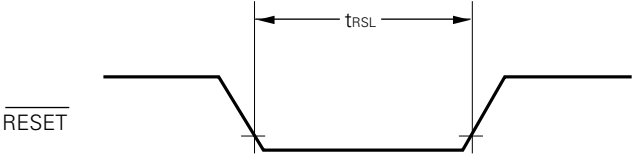**Serial Transfer Timing**



**Interrupt Input Timing**



**RESET Input Timing**

**Data Memory STOP Mode Low Voltage Data Retention Characteristics (T$_a$ = −10 to +70 °C)**

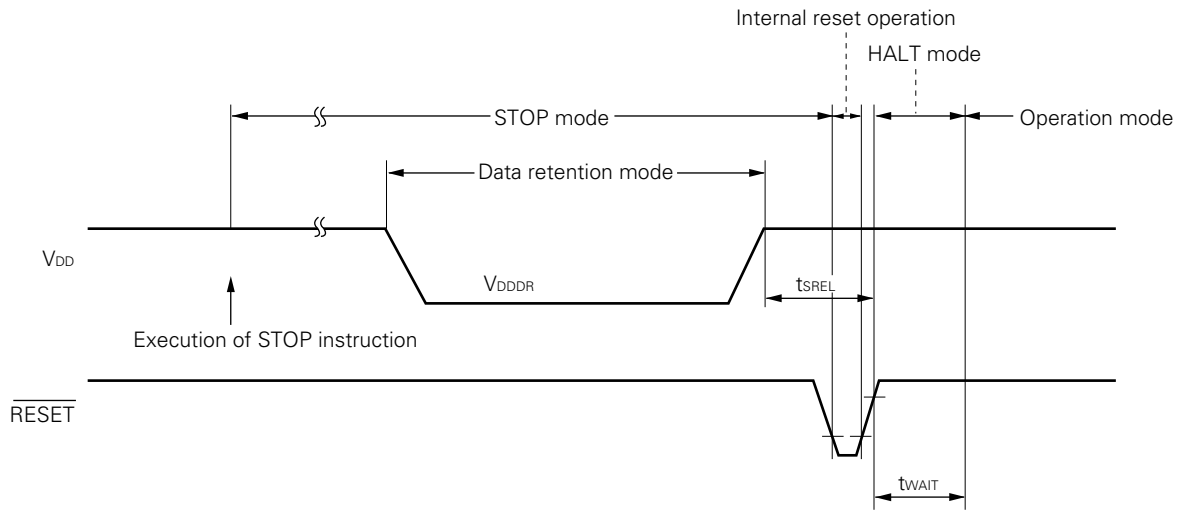| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention voltage | V$_{DDDR}$ | | 2.0 | | 5.5 | V |
| Data retention current | I$_{DDDR}$ | V$_{DDDR}$ = 2.0 V | | 0.1 | 10 | $\mu$A |
| Released signal SET time | t$_{SREL}$ | | 0 | | | $\mu$s |
| Oscillation stabilization time **Note 1** | t$_{WAIT}$ | Released by $\overline{RESET}$ input | | $2^{17}/f_x$ | | ms |
| | | Released by interrupt request | | **Note 2** | | ms |

**Note 1.** The oscillation stabilization wait time is a period during which the CPU is kept inactive in order to avoid unstable operation at the start of oscillation.

**2.** Depends on the setting of the basic interval time mode register (BTM) (see the following table).

| BTM3 | BTM2 | BTM1 | BTM0 | Wait time (    ): f$_{XX}$ = 4.19 MHz |
|---|---|---|---|---|
| — | 0 | 0 | 0 | $2^{20}/f_{XX}$ (approx. 250 ms) |
| — | 0 | 1 | 1 | $2^{17}/f_{XX}$ (approx. 31.3 ms) |
| — | 1 | 0 | 1 | $2^{15}/f_{XX}$ (approx. 7.82 ms) |
| — | 1 | 1 | 1 | $2^{13}/f_{XX}$ (approx. 1.95 ms) |

Data Retention Timing (STOP mode is released by $\overline{RESET}$ input)



Data Retention Timing (Standby release signal: STOP mode is released by interrupt signal)
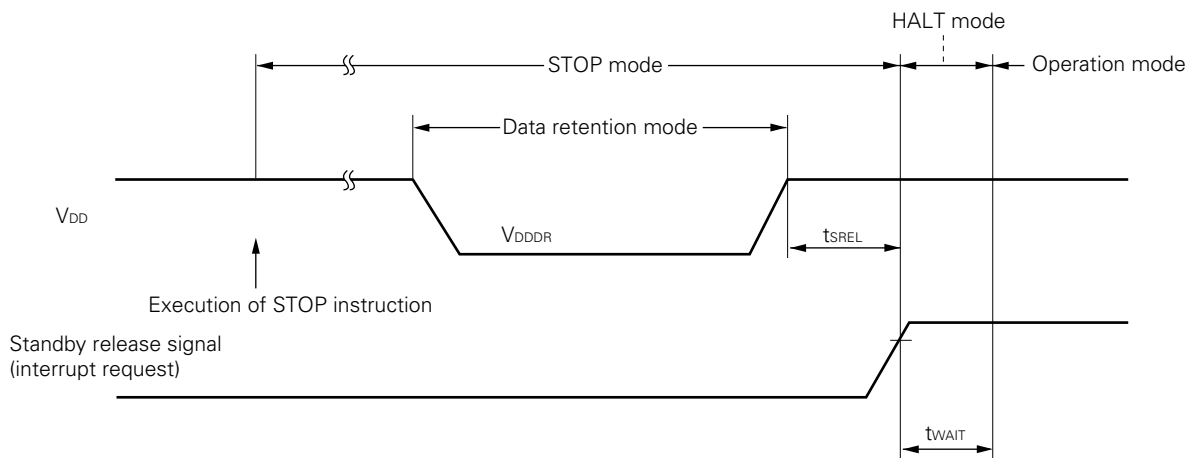
**DC Programming Characteristics (T$_a$ = 25 ± 5 °C, V$_{DD}$ = 6.0 ± 0.25 V, V$_{PP}$ = 12.5 ± 0.3 V, V$_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| High-level input voltage | V$_{IH1}$ | All except X1, X2 | 0.7 V$_{DD}$ | | V$_{DD}$ | V |
| | V$_{IH2}$ | X1, X2 | V$_{DD}$–0.5 | | V$_{DD}$ | V |
| Low-level input voltage | V$_{IL1}$ | All except X1, X2 | 0 | | 0.3 V$_{DD}$ | V |
| | V$_{IL2}$ | X1, X2 | 0 | | 0.4 | V |
| Input leakage current | I$_{L1}$ | V$_{IN}$ = V$_{IL}$ or V$_{IH}$ | | | 10 | μA |
| High-level output voltage | V$_{OH}$ | I$_{OH}$ = –1 mA | V$_{DD}$–1.0 | | | V |
| Low-level output voltage | V$_{OL}$ | I$_{OL}$ = 1.6 mA | | | 0.4 | V |
| V$_{DD}$ power supply current | I$_{DD}$ | | | | 30 | mA |
| V$_{PP}$ power supply current | I$_{PP}$ | MD0 = V$_{IL}$, MD1 = V$_{IH}$ | | | 30 | mA |

**Note 1.** V$_{PP}$ should not exceed +22 V (including overshoot).
    **2.** V$_{DD}$ should be applied before V$_{PP}$ and turned off after V$_{PP}$.

**AC Programming Characteristics (T$_a$ = 25 ± 5 °C, V$_{DD}$ = 6.0 ± 0.25 V, V$_{PP}$ = 12.5 ± 0.3 V, V$_{SS}$ = 0 V)**

| Parameter | Symbol | Note 1 | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Address setup time [Note 2] (toMD0↓) | t$_{AS}$ | t$_{AS}$ | | 2 | | | μs |
| MD1 setup time (to MD0↓) | t$_{MIS}$ | t$_{OES}$ | | 2 | | | μs |
| Data setup time (to MD0↓) | t$_{DS}$ | t$_{DS}$ | | 2 | | | μs |
| Address hold time [Note 2] (from MD0↑) | t$_{AH}$ | t$_{AH}$ | | 2 | | | μs |
| Data hold time (from MD0↑) | t$_{DH}$ | t$_{DH}$ | | 2 | | | μs |
| MD0 ↑ → data output float delay time | t$_{DF}$ | t$_{DF}$ | | 0 | | 130 | ns |
| V$_{PP}$ setup time (to MD3↑) | t$_{VPS}$ | t$_{VPS}$ | | 2 | | | μs |
| V$_{DD}$ setup time (to MD3↑) | t$_{VDS}$ | t$_{VCS}$ | | 2 | | | μs |
| Initialized program pulse width | t$_{PW}$ | t$_{PW}$ | | 0.95 | 1.0 | 1.05 | ms |
| Additional program pulse width | t$_{OPW}$ | t$_{OPW}$ | | 0.95 | | 21.0 | ms |
| MD0 setup time (to MD1↑) | t$_{MOS}$ | t$_{CES}$ | | 2 | | | μs |
| MD0 ↓ → data output delay time | t$_{DV}$ | t$_{DV}$ | MD0 = MD1 = V$_{IL}$ | | | 1 | μs |
| MD1 hold time (from MD0↑) | t$_{MIH}$ | t$_{OEH}$ | t$_{MIH}$ + t$_{MIR}$ ≥ 50 μs | 2 | | | μs |
| MD1 recovery time (to MD0↓) | t$_{MIR}$ | t$_{OR}$ | | 2 | | | μs |
| Program counter reset time | t$_{PCR}$ | — | | 10 | | | μs |
| X1 input high- and low-level width | t$_{XH}$, t$_{XL}$ | — | | 0.125 | | | μs |
| X1 input frequency | f$_X$ | — | | | | 4.19 | MHz |
| Initial mode set time | t$_I$ | — | | 2 | | | μs |
| MD3 setup time (to MD1↑) | t$_{M3S}$ | — | | 2 | | | μs |
| MD3 hold time (from MD1↓) | t$_{M3H}$ | — | | 2 | | | μs |
| MD3 setup time (to MD0↓) | t$_{M3SR}$ | — | During program read cycle | 2 | | | μs |
| Address [Note 2] → Data output delay time | t$_{DAD}$ | t$_{ACC}$ | During program read cycle | 2 | | | μs |
| Address [Note 2] → Data output hold time | t$_{HAD}$ | t$_{OH}$ | During program resd cycle | 0 | | 130 | ns |
| MD3 hold time (from MD0↑) | t$_{M3HR}$ | — | During program read cycle | 2 | | | μs |
| MD3 ↓ → data output float delay time | t$_{DFR}$ | — | During program read cycle | 2 | | | μs |

**Note 1.** Symbol of corresponding μPD27C256.
    **2.** Internal address is incremented by 1 at the rising edge of the fourth X1 input. This address signal is not output to external pins.
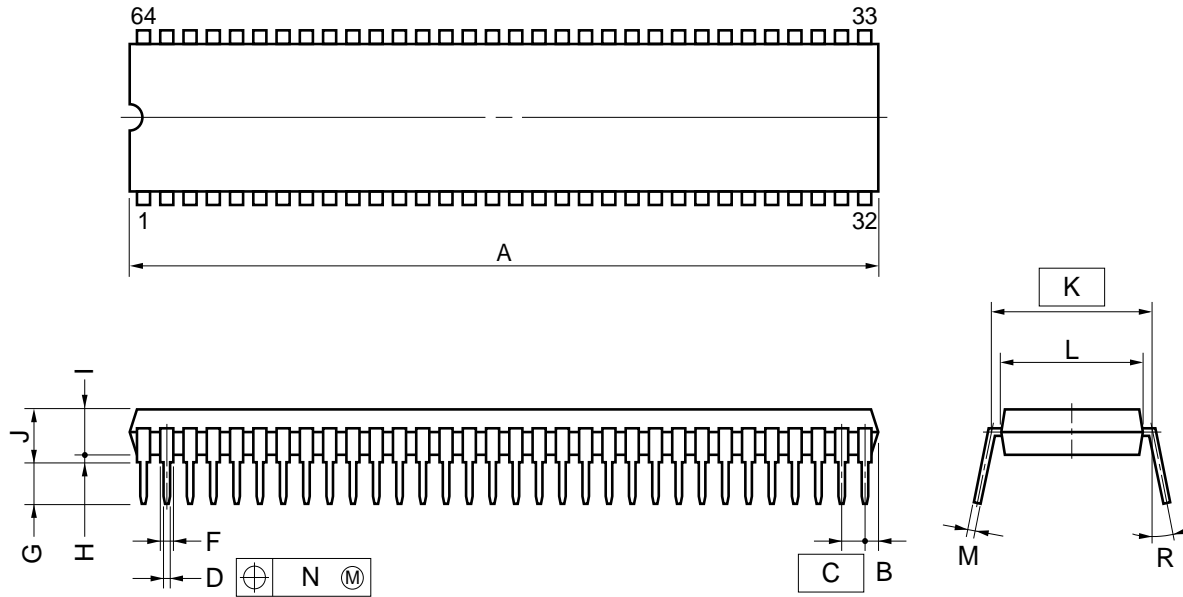
**Program Memory Write Timing**
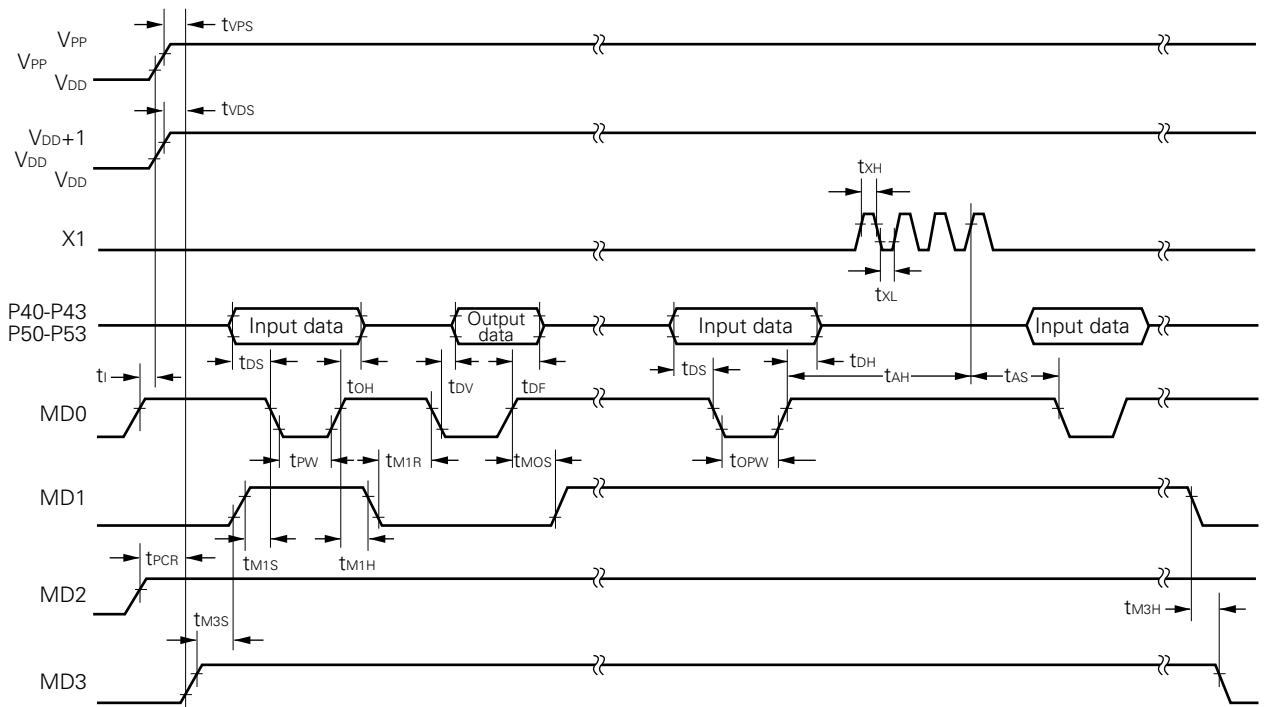


**Program Memory Read Timing**
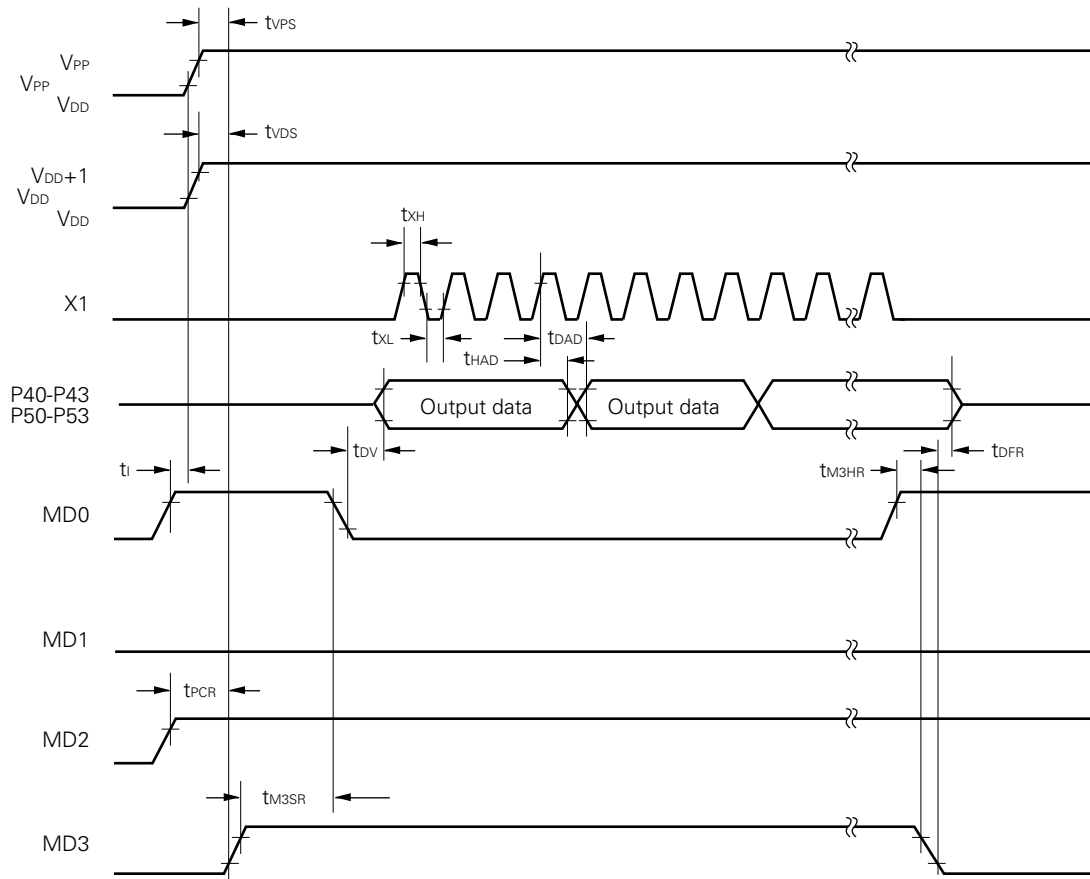
## 5. PACKAGE DRAWINGS

### 64 PIN PLASTIC SHRINK DIP (750 mil)



**NOTE**

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS | INCHES |
|------|-------------|--------|
| A | 58.68 MAX. | 2.311 MAX. |
| B | 1.78 MAX. | 0.070 MAX. |
| C | 1.778 (T.P.) | 0.070 (T.P.) |
| D | 0.50±0.10 | $0.020^{+0.004}_{-0.005}$ |
| F | 0.9 MIN. | 0.035 MIN. |
| G | 3.2±0.3 | 0.126±0.012 |
| H | 0.51 MIN. | 0.020 MIN. |
| I | 4.31 MAX. | 0.170 MAX. |
| J | 5.08 MAX. | 0.200 MAX. |
| K | 19.05 (T.P.) | 0.750 (T.P.) |
| L | 17.0 | 0.669 |
| M | $0.25^{+0.10}_{-0.05}$ | $0.010^{+0.004}_{-0.003}$ |
| N | 0.17 | 0.007 |
| R | 0~15° | 0~15° |

**P64C-70-750A,C-1**

### 6. RECOMMENDED SOLDERING CONDITIONS                                    ★

The following conditions must be met when soldering this product.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207)**.

Please consult with our sales offices in case other soldering process is used, or in case other soldering is done under different conditions.

**Table 6-1   Type of Through Hole Device**

$\mu$**PD75P216ACW: 64-pin plastic shrink DIP (750 mil)**

| Soldering process | Soldering conditions |
|---|---|
| Wave soldering (only lead part) | Solder temperature: 260 °C or lower, Flow time: 10 seconds or less |
| Partial heating method | Pin temperature: 260 °C or lower, Time: 10 seconds or less |

**Caution   This wave soldering should be applied only to lead part, and don't jet molten solder on the surface of package.**

★   **APPENDIX DEVELOPMENT TOOLS**

The following development tools are provided for the development of a system which employs the $\mu$PD75P216A.

**Language processor**

<table>
<tr><td rowspan="4">RA75X relocatable assembler</td><td colspan="3">Host machine</td><td rowspan="2">Part number</td></tr>
<tr><td></td><td>OS</td><td>Distribution media</td></tr>
<tr><td>PC-9800 series</td><td rowspan="2">MS-DOS™<br>Ver. 3.10<br>to<br>Ver. 3.30C</td><td>3.5-inch 2HD</td><td>$\mu$S5A13RA75X</td></tr>
<tr><td></td><td>5-inch 2HD</td><td>$\mu$S5A10RA75X</td></tr>
<tr><td></td><td>IBM PC series</td><td>PC DOS™<br>(Ver. 3.1)</td><td>5-inch 2HC</td><td>$\mu$S7B10RA75X</td></tr>
</table>

**PROM programming tools**

<table>
<tr><td rowspan="6">Hardware</td><td>PG-1500</td><td colspan="4">The PG-1500 PROM programmer is used together with an accessory board and optional programmer adapter. It allows the user to program a single chip microcomputer containing PROM from a standalone terminal or a host machine. The PG-1500 can be used to program typical 256K-bit to 4M-bit PROMs.</td></tr>
<tr><td>PA-75P216ACW</td><td colspan="4">PROM programmer adapter dedicated to $\mu$PD75P216ACW.<br>Connect the programmer adapter to PG-1500 for use.</td></tr>
<tr><td>AF-9703<br>AF-9704</td><td colspan="4">PROM programmer produced by Ando Electric Corp.</td></tr>
<tr><td>AF-9789</td><td colspan="4">Programmer adapter dedicated to the $\mu$PD75P216ACW<br>Connect to AF-9703, AF-9704 for use</td></tr>
<tr><td>UNISITE<br>2900<br>3900</td><td colspan="4">PROM programmer produced by Data I/O Japan Corp.</td></tr>
<tr><td>PPI-0601</td><td colspan="4">Programmer adapter dedicated to the $\mu$PD75P216ACW<br>Connect to UNISITE, 2900, 3900 for use</td></tr>
<tr><td rowspan="6">Software</td><td rowspan="6">PG-1500 controller</td><td colspan="4">This program enables the host machine to control the PG-1500 through the serial and parallel interfaces.</td></tr>
<tr><td colspan="3">Host machine</td><td>Part number</td></tr>
<tr><td></td><td>OS</td><td>Distribution media</td><td></td></tr>
<tr><td>PC-9800 series</td><td rowspan="2">MS-DOS<br>Ver. 3.10<br>to<br>Ver. 3.30C</td><td>3.5-inch 2HD</td><td>$\mu$S5A13PG1500</td></tr>
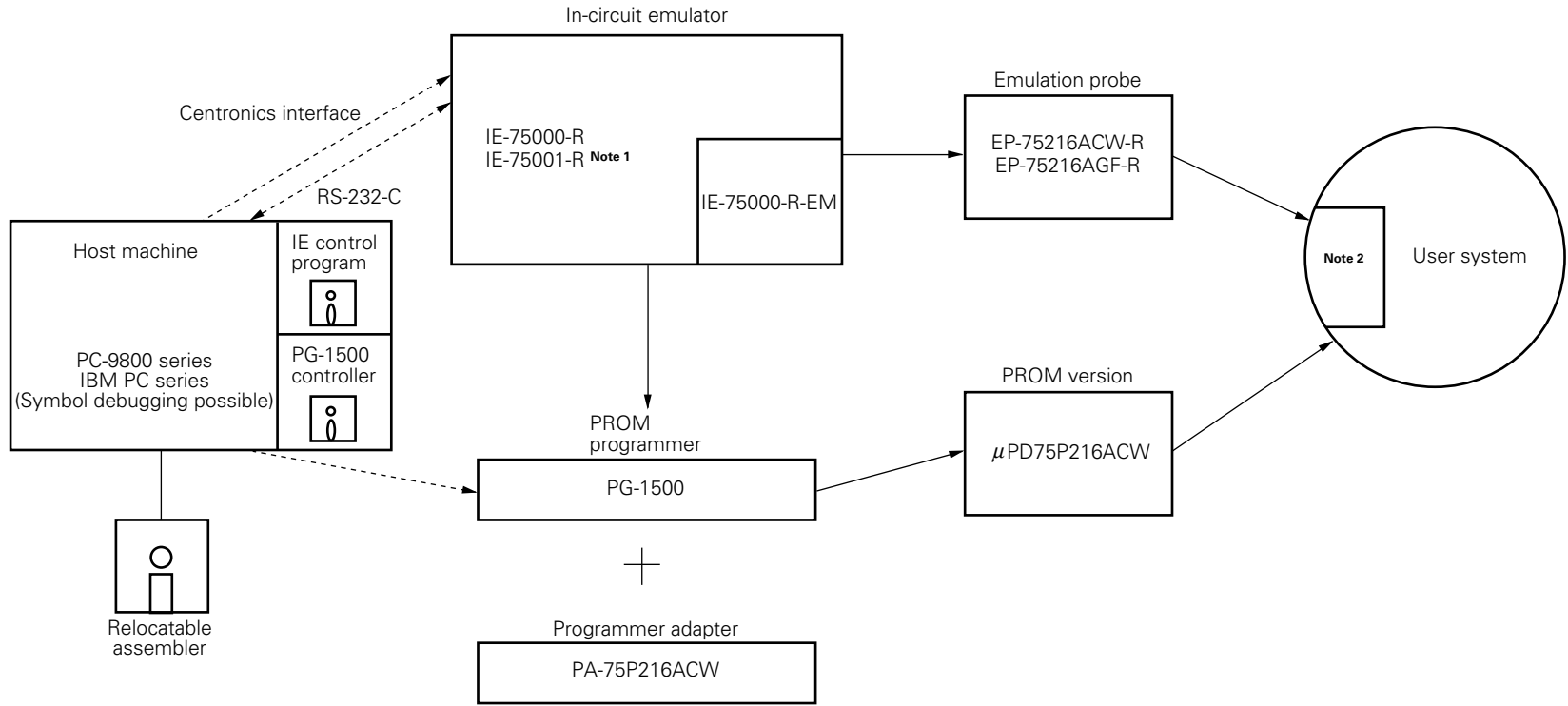<tr><td></td><td>5-inch 2HD</td><td>$\mu$S5A10PG1500</td></tr>
<tr><td>IBM PC series</td><td>PC DOS<br>(Ver. 3.1)</td><td>5-inch 2HC</td><td>$\mu$S7B10PG1500</td></tr>
</table>

**Debugging tools**

| | | |
|---|---|---|
| Hardware | IE-75000-R **Note** | The IE-75000-R is an in-circuit emulator to debug the hardware and software at developing application system for 75X series.<br>This emulator is used together with the emulation probe. For efficient debugging, the emulator is connected to the host machine and PROM programmer. |
| | IE-75000-R-EM | The IE-75000-R-EM is an emulation board for the IE-75000-R and IE-75001-R. The IE-75000-R contains the emulation board. The emulation board is used together with the IE-75000-R or IE-75001-R to evaluate the $\mu$PD75P048. |
| | IE-75001-R | The IE-75001-R is an in-circuit emulator to debug the hardware and software at developing application system for 75X series.<br>This emulator is used together with the IE-75000-R-EM emulation board (option) and emulation probe. For efficient debugging, the emulator is connected to the host machine and PROM programmer. |
| | EP-75216ACW-R | Emulation probe for the $\mu$PD75P216ACW.<br>Connect this probe to the IE-75000-R or IE-75001-R and the IE-75000-R-EM for use. |
| Software | IE control program | This program enables the host machine to control the IE-75000-R or IE-75001-R on the host machine through the RS-232-C interface. |

| Host machine | | | Part number |
|---|---|---|---|
| | OS | Distribution media | |
| PC-9800 series | MS-DOS<br>Ver. 3.10<br>to<br>Ver. 3.30C | 3.5-inch 2HD | $\mu$S5A13IE75X |
| | | 5-inch 2HD | $\mu$S5A10IE75X |
| IBM PC series | PC DOS<br>(Ver. 3.1) | 5-inch 2HC | $\mu$S7B10IE75X |

**Notes**   Provided only for maintenance purposes.

**Remark**   NEC is not responsible for the IE control program operation unless it runs on any host machine with the operation system listed above.

**Configuration of Development Tools**

In-circuit emulator

Emulation probe

Centronics interface

IE-75000-R
IE-75001-R **Note 1**

EP-75216ACW-R
EP-75216AGF-R

IE-75000-R-EM

RS-232-C

**Note 2** User system

Host machine

IE control
program

PC-9800 series
IBM PC series
(Symbol debugging possible)

PG-1500
controller

PROM
programmer

PROM version

PG-1500

μPD75P216ACW

Relocatable
assembler

＋

Programmer adapter

PA-75P216ACW

**Notes 1.** IE-75001-R is not provided with IE-75000-R-EM (option)
　　　　**2.** EV-9200GC-64

# NOTES FOR CMOS DEVICES

## ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:**
**Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.**

## ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:**
**No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.**

## ③ STATUS BEFORE INITIAIZATION OF MOS DEVICES

**Note:**
**Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.**

"$\mu$PD75216A USER'S MANUAL" (IEM-988F) is also prepared for this product (option).