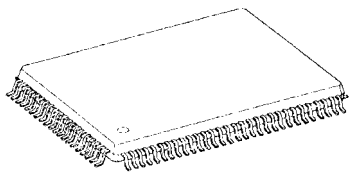
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9457F

Firmware Built In Digital Servo

The TC9457F is a firmware incorporating CD digital servo system. In addition to an LCD/LED driver, 4-channel 6-bit AD converters, and 2-wire/3-wire serial interface, it has a buzzer function, interrupt function, and 8-bit timer/counter. The CPU allows selection of the operating clock from three types of crystal oscillators (16.9344 MHz, 4.5 MHz, and 75 kHz), making interfacing with a CD easy. The CD digital servo incorporates various functions and circuits required for CD systems. These include sync separation protection and interpolation, EFM demodulation, error correction, digital equalizer for servoing, and a servo control circuit. Furthermore, it contains a 1-bit DA converter, so that when combined with the digital servo head amp TA2109F, it allows you to create a maintenance-free, extremely simple CD player system.



QFP100-P-1420-0.65A

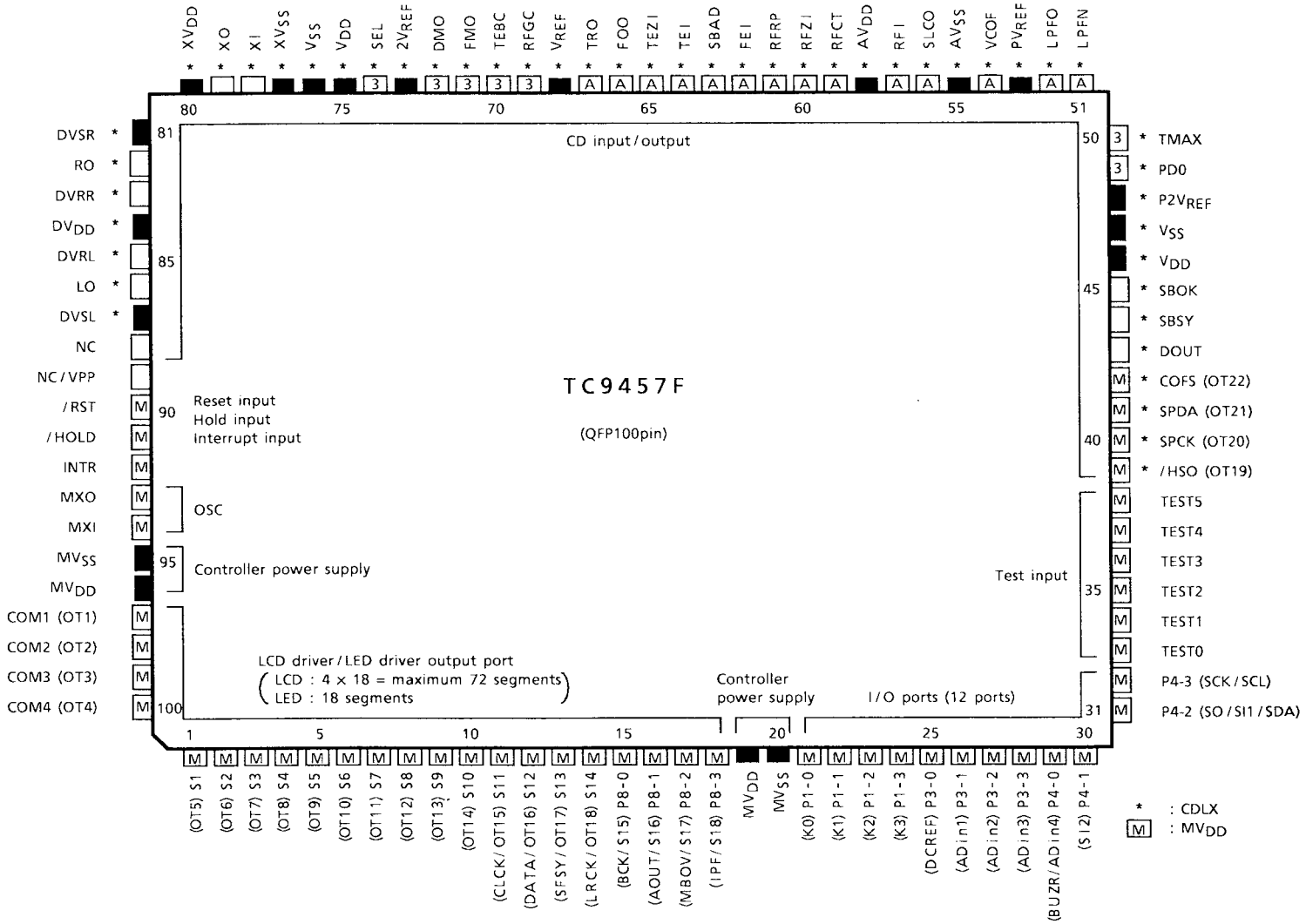
Weight: 1.6 g (typ.)

Features

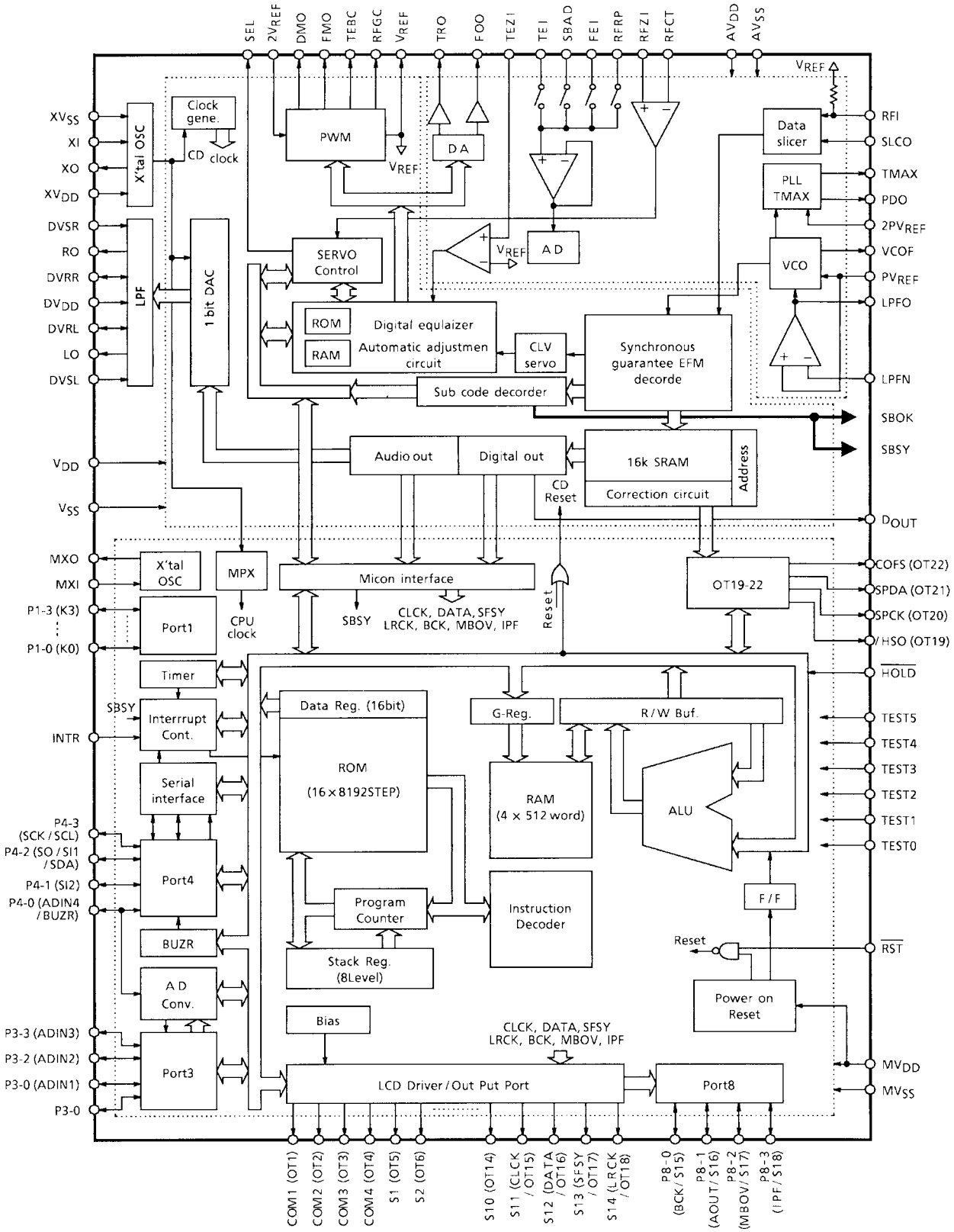
- CMOS−technology DTS microcontroller LSI incorporating a CD digital servo and LCD/LED driver
- Operating supply voltage:
  When CD is operating, V_{DD} = 4.5 to 5.5 V (5.0 V typ.)
  When CD is turned off, V_{DD} = 2.7 to 5.5 V (CPU operating)
- Current consumption:
  When CD is operating, I_{DD} = 55 mA (typ.)
  When CD is turned off, I_{DD} = 2 mA (typ.) (using 4.5 MHz crystal; CPU operating)
  When CD is turned off, I_{DD} = 0.1 mA (using 75 kHz crystal; CPU operating)
- Operating temperature range: Ta = −40 to 85 °C
- Firmware
  - Instruction execution time: 1.89/1.78/107 μs
  - Crystal oscillator frequency: 16.9344 MHz/4.5 MHz/75 kHz
  - AD converter: 6 bits, 4 channels
  - LCD driver: 1/4 duty, 1/2 biased, maximum 72 segments
  - LED driver: 4 digits × maximum 14 segments (shared with LCD driver in software)
  - Timer/counter: 8 bits (timer clock selectable from INTR1, INTR2, instruction cycle, or 1 kHz)
  - Serial interface: 3-wire/2-wire interface (data length: 4 or 8 bits)
  - Buzzer: 0.625 to 3 kHz (8 types) ; 4 modes available-continuous, single, 10 Hz intermittent, and 10 Hz intermittent at 1 Hz interval
  - Interrupt: 1 external, 3 internal (CD subing synchronous, serial interface, 8 bits timer)

- CD digital servo system
  - Capable of decoding text data.
  - Sure and reliable sync pattern detection, sync signal protection, and interpolation.
  - Contains EFM demodulator circuit and subcode demodulator circuit.
  - CIRC logical equations to provide high correction capability:
    dual C1 correction and quadruple C2 correction.
  - Supports variable-speed playback.
  - Jitter absorbing capability of +6 frames.
  - Contains 16 KB RAM.
  - Contains Digital OUT circuit.
  - Contains L/R independent digital attenuators.
  - Audio output responds to bilingual function.
  - Subcode Q data is free of read timing and can be output synchronously with audio data.
    (LCD/OT pin switchable by a program)
  - Contains data slice and analog PLL (using adjustment-free VOC) circuits.
  - Loop gain, offset, and balance in focus and tracking servos can be automatically adjusted.
  - Contains RF gain automatic adjusting circuit.
  - Contains phase-correcting digital equalizer.
  - Contains coefficient RAM for digital equalizer, thus supporting various types of pickup.
  - Contains focus and tracking servo control circuit.
  - Servo control is possible in every mode available, providing fast and stable search.
  - Speed control method is adopted for lens and feed kick.
  - Contains AFC and APC circuits for disc motor CLV servo.
  - Contains defect and shock corrective circuit.
  - Contains 8 times oversampling digital filter and 1-bit DA converter.
  - 100 pin flat package.

Pin Connection Diagram



Block Diagram



Description Of Pin Function

Pin No.	Symbol	Pin Name	Function And Operation	Remarks
1~10	S1/OT5 ~ S10/OT14	LCD segment outputs /Output ports	Segment signal outputs to the LCD panel. Up to 72 segments in a matrix with COM1 to COM4 can be displayed. All of the S1 to S18 pins can be switched for output ports by a program (Note 1). Also, the S15 to S18 pins each can be switched for I/O ports individually. When set for I/O ports, these pins become Nch open-drain outputs. Furthermore, the S11 to S14 and the P8-0 to P8-3 pins can be switched for use as CD signal (CLCK to IPF) input/output pins by a program. • CLCK : Subcodes P thru W data readout clock input/output. Selected between input and output by a command. • DATA : Subcodes P thru W data output. • SFSY : Playback system frame sync signal output. • LRCK : Channel clock (44.1 kHz) output. It outputs a low for L channel and a high for R channel. Polarity can be inverted by a command. • BCK : Bit clock (1,4112 MHz) output. • AOUT : Audio data output. • MBOV : Buffer memory-over signal output. It outputs a high when buffer overflows. • IPF : Correction flag output. When AOUT is C2 correction output, it outputs a high indicating that correction is impossible. For CD signal output, set parameters OT for output and LEDon = 1. Furthermore, when set for output ports, the buffer capability can be increased by setting the LEDon bit to 1, so that it can be used as an LED driver. These pins normally are used for LED segment outputs. Since the output ports can increment OT1 through OT18 by an instruction, data in external RAM/ROM can be accessed easily. Note 1: After a system reset, the output port shared pins are set for LCD output and the I/O port shared pins are set for I/O port input.	—
11	S11/OT15 /CLCK	LCD segment outputs /Output ports /CD signals		—
12	S12/OT16 /DATA			—
13	S13/OT17 /SFSY			—
14	S14/OT18 /LRCK			—
15	S8-0/S15 /BCK	I/O ports /LCD segment outputs /CD signals		—
16	P8-1/S16 /AOUT			—
17	P8-2/S17 /MBOV			—
18	P8-3/S18 /IPF			—
21~24	P1-0~P1-3 /K0~K3	I/O port 1 /Key input ports	4-bit CMOS I/O ports. These ports can be set for input or output bit for bit by a program. These pins can be pulled up to V_{DD} or down to GND by a program. Therefore, they can be used as key input pins. Also, when they are set for I/O port input, a change of state in this input can be used to clear the clock stop or wait mode.	—

Pin No.	Symbol	Pin Name	Function And Operation	Remarks
25 26~28 29	P3-0/DCREF P3-1/ADIN1 ~ P3-3/ADIN3 P4-0/ADIN4/ BUZR	I/O port 3 /AD analog reference voltage input I/O port 3 /AD analog voltage input I/O port 4 /AD analog voltage inputs /Buzzer output	5-bit CMOS I/O ports. These ports can be set for input or output bit for bit by a program. The P3-0 to P4-0 pins serve dual purposes as analog inputs for the internal 6-bit 4-channel AD converters. The internal AD converters can complete conversion in 6 instruction cycles using a successive approximation method. The required pins can be set for AD analog input bit for bit by a program. P3-0 can be set for reference voltage input, and the internal power supply (MV_{DD}) can be used for this reference voltage. The P4-0 pin serves dual purposes as a buzzer output pin. The buzzer output can be selected from 8 frequencies, 0.625 to 3 kHz. Each selected frequency can be output in one of four modes: continuous, single, 10 Hz intermittent, and 10 Hz intermittent at 1 Hz interval. Whether or not to use and how to control the AD converter and buzzer all can be set by a program. Note 2: If P3-0 is set for reference voltage input, note that although normally in a high-impedance state, this input during AD conversion becomes a 10 kΩ load, typ. Therefore, pay careful attention to the output impedance that is input to this pin.	—
30 31 32	P4-1/S12 P4-2/S0/SI1 /SDA P4-3/SCK /SCL	I/O port 4 /Serial data input /Serial data input /output /Serial clock input /output	3-bit CMOS I/O ports. These ports can be set for input or output bit for bit by a program. These pins serve dual purposes as input or output pins for the serial interface circuit (SI0). The SI0 is a 2-wire/3-wire compatible serial interface. 4 or 8 bits of serial data, beginning with the MSB or LSB, are serially output from the SO/SDA pin at each clock edge on the SCK/SCL pin, and the data on SI1 or SI2 pin is serially input to the device. The serial clock (SCK/SCL) allows selection between the internal (450/225/150/75 kHz) and external sources and a selection of the active edge, rise or fall. Moreover, since the clock and data can be output via Nch open-drain outputs, various device controls and communication between controllers can be greatly facilitated. When an SI0 interrupt is enabled, an interrupt is generated at completion of SI0 execution and the program jumps to address 4. This is effective when high-speed serial communication is desired. All inputs to SI0 contain a Schmitt trigger circuit. Whether or not to use SI0 and how to control it all can be set by a program.	—
33~38	TEST0 ~ TEST5	Test mode control inputs	Test mode control input pins. The test mode is selected when these pins are set high and normal operation is selected when they are low. These pins normally must be held low or left open (NC) when used for this purpose. (Pulldown resistors are built-in).	—
39~42	/HSO/OT19 SPCK/OT20 SPDA/OT21 COFS/OT22	CD control signal outputs /output ports	CD control output pins. • /HSO : Playback speed mode output. High = normal speed; Low = double speed. • SPCK : Processor status signal readout clock output (176.4 kHz) • SPDA : Processor status signal output. • COFS : Correction system frame clock output (7.35 kHz). These pins can be switched for output ports by a program.	—
43	DOUT	CD control input/outputs	Digital output pin.	—
44	SBSY		Subcode block sync output pin. It outputs a high at the S1 position when subcode sync is detected.	—

Pin No.	Symbol	Pin Name	Function And Operation	Remarks
45	SBOK	CD control input/outputs	Subcode Q data CRCC determination result output pin. It outputs a high when CRCC check is found OK.	—
46, 75	V_{DD}		CD unit's digital block power supply pins. Normally, apply 5 V to V_{DD}. When not using a CD (CD off), this power supply can be turned off, with only the controller power supply kept active, so that the controller alone is operating. In this case, the CDoff bit must be set to 1. When this bit is set to 1, pins 11 through 18 and pins 39 through 42 all are changed for output ports if they have been set for CD control signal input/output pins.	—
47, 76	V_{SS}			—
48	$P2V_{REF}$		PLL block-2 V_{REF} pin.	—
49	PDO		This pin outputs a phase error between EFM and PLCK signals.	—
50	TMAX		TMAX detection result output pin. Selected by command bit TMPS. Longer than preset period : Outputs $P2V_{REF}$. Shorter than preset period : Low level (V_{SS}). Within preset period : High impedance.	—
51	LPFN		Inverted input of low-pass filter amp.	Analog input
52	LPFO		Output of low-pass filter amp.	Analog output
53	PVREF		PLL block V_{REF} pin.	—
54	VCOF		VCO filter pin.	Analog output
55	AV_{SS}		Analog block ground pin.	—
56	SLCO		DAC output pin for data slice level generation.	Analog output
57	RFI		RF signal input pin.	Analog input (Zin : command select)
58	AV_{DD}		Analog block power supply pin.	—
59	RFCT		RFRP signal center level input pin.	Analog input (Zin = 50 kΩ)
60	RFZI		RFRP zero-cross input pin.	Analog input
61	RFRP		RF ripple signal input pin.	Analog input
62	FEI		Focus error signal input pin.	Analog input
63	SBAD		Subbeam add signal input pin.	Analog input
64	TEI		Tracking error input pin. This input is read when tracking servo is on.	Analog input
65	TEZI		Tracking error zero-cross input pin.	Analog input (Zin = 10 kΩ)
66	FOO		Focus equalizer output pin.	Analog output ($2V_{REF}$ to AV_{SS})
67	TRO		Tracking equalizer output pin.	Analog output ($2V_{REF}$ to AV_{SS})
68	V_{REF}		Analog reference power supply pin.	—
69	RFGC		RF amplitude adjusting control signal output pin. It outputs 3-level PWM signals. (PWM carrier = 88.2 kHz)	—
70	TEBC		Tracking balance control signal output pin. It outputs 3-level PWM signals. (PWM carrier = 88.2 kHz)	—
71	FMO		Focus equalizer output pin. It outputs 3-level PWM signals. (PWM carrier = 88.2 kHz)	—
72	DMO		Disc equalizer output pin. It outputs 3-level PWM signals. (PWM carrier = DSP block 88.2 kHz, synchronized to PXO)	—
73	$2V_{REF}$		Analog reference power supply pin. ($2 \times V_{REF}$)	—

Pin No.	Symbol	Pin Name	Function And Operation	Remarks
74	SEL	CD control input/outputs	APC circuit on/off signal output pin. When laser is on, this pin goes to a high-impedance state when UHS = low and outputs a high when UHS = high.	—
77	XV_{SS}		CD's crystal oscillator power supply pins. Normally, connect these pins to the power supply lines that are used in common for the V_{DD} and V_{SS} pins.	—
80	XV_{DD}			—
78	XI		CD's crystal oscillator input/output pins. Normally, connect 16.9344 MHz here. This clock is used as the system clock for the CD. After a system reset, it also is used as the system clock on the controller side. Therefore, all of the CD power supplies must be fed with power after a reset.	—
79	XO			—
81	DVSR		R-channel DA converter unit ground pin.	—
82	RO		R-channel data forward output pin.	—
83	DVRR		R-channel reference voltage pin.	—
84	DV_{DD}		DA converter unit power supply pin.	—
85	DVRL		L-channel reference voltage pin.	—
86	LO		L-channel data forward output pin.	—
87	DVSL		L-channel DA converter unit ground pin.	—
88, 89	NC		NC pins. Normally, connect these pins to ground or leave them open. Pin 89 serves dual purposes as the V_{pp} pin of an E^2PROM product. Therefore, when this pin is left open, it can be shared with an E^2PROM product.	—
90	$\overline{RESET}$	Reset input	Device's system reset signal input pin. The device remains reset while $\overline{RESET}$ is held low and when $\overline{RESET}$ is released back high, the CD unit becomes operational and the program starts from address 0. Normally, a system reset is asserted when a voltage of 2.7 V or more is applied to V_{DD} when it is at 0 V (power-on reset). Therefore, this pin must be pulled high when used for this purpose.	—
91	$\overline{HOLD}$	Hold mode control input	This pin is used to input a signal that requests or clears the hold mode. Normally, use this pin for CD mode select signal input or battery detection signal input. There are two hold modes : clock stop mode (crystal oscillator turned off) and a wait mode (CPU stopped). These modes are entered by executing the CKSTP and WAIT instructions, respectively. The clock stop mode can be requested by a programmed input: low level detection on $\overline{HOLD}$ pin or forced execution, and can be cleared by detecting a high on the $\overline{HOLD}$ pin or a change of state in its input signal. When the CKSTP instruction is executed, the clock generator and the CPU stop operating and the device is placed in a memory backup state. During this state, the device's current consumption is reduced to 1μA or less. At the same time, the display output and CMOS output ports are automatically set low, and the Nch open-drain outputs are turned off. The wait mode is executed regardless of the input state on the $\overline{HOLD}$ pin, with the device's current consumption reduced. In this mode, the user can choose to keep only the crystal oscillator operating or have the CPU paused by programming. If the former is selected, all display outputs are set low and other pins retain their state ; if the latter is selected, all states are retained except that the CPU is temporarily stopped. This mode is cleared by a change of state in the $\overline{HOLD}$ input.	—

Pin No.	Symbol	Pin Name	Function And Operation	Remarks
92	INTR	External interrupt input	External interrupt input pin. When the interrupt facility is enabled and a pulse of 1.11 to 2.22 μs in duration is applied to this pin, an interrupt is generated and the program jumps to address 1. Input logic and the active edge (rise or fall) can be selected for each interrupt input. Also, the internal 8-bit timer clock can be chosen for this interrupt input, in which case it is possible to count pulses or generate an interrupt at a given pulse count (address 3). Since this pin is a Schmitt trigger type, it can be used as an input port for receiving remote control signals, etc.	—
93	MXO	Controller's crystal oscillator pins	Crystal oscillator pins for the controller. The oscillator clock is used as the timebase for the clock facility or as the controller's system clock. Connect a 4.5 MHz or 75 kHz crystal resonator to the MXO and MXI pins. Since these pins do not contain internal feedback resistors, etc, an amp resistor or output resistor must be added external to the chip. • 75 kHz··· ROUT = 100 kΩ, Rf = 10 MΩ Ci = Co = 15 pF (typ.) • 4.5 MHz··· ROUT = 0 Ω, Rf = 1 MΩ Ci = Co = 15 pF (typ.) When using the clock generated by the CD unit's crystal oscillator for clocking the entire device operation, fix the MXI pin to the GND level. Oscillation is stopped by executing a CKSTP instruction. Select the crystal oscillator and control its operation by a program. Note 3: When after turning on the CD unit's power supply, the controller system clock is switched from the crystal oscillator on the controller side to that on the CD side, provide an allowance time of several 10 ms for the CD unit's crystal oscillator to stabilize after it is powered on. This is necessary to prevent the controller from operating erratically.	—
94	MXI			—
19, 96	MV_{DD}	Controller unit power supply pins	Power supply pins. Normally, apply a voltage of 4.5 to 5.5 V to V_{DD}. In a backup state (when the CKSTP instruction executed), the device's current consumption is reduced to 1 μA or less, allowing for the supply voltage to be lowered to 2.0 V. The device is reset and the program starts from address 0 when a voltage of 2.7 V or more is applied to this pin when it is at 0 V (power-on reset). Note 4: For reason of this power-on reset, make sure the device's power supply rise time is between 10 to 100 ms.	—
20, 95	MV_{SS}			—
97	COM1/OT1	LCD common outputs /Output ports	Common signal outputs to the LCD panel. Up to 72 segments in a matrix with S1 to S18 can be displayed. Three voltage levels MV_{DD}, V_{EE} (1/2 MV_{DD}), and GND are output for 83 Hz period at 2 ms intervals. After a system reset and after deassertion of a clock stop instruction, the V_{EE} voltage is output and the DISP OFF bit is set to 0 before common signals are output. These pins can be switched for output ports by a program (Note1). In this case, the buffer capacity can be increased by setting the LEDon bit to 1, so that it can be used as an LED driver. These four pins normally are used for LED digit outputs.	—
98	COM2/OT2			—
99	COM3/OT3			—
100	COM4/OT4			—

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3~6.0	V
Input voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	1400	mW
Operating temperature	T_{opr}	−40~85	°C
Storage temperature	T_{stg}	−65~150	°C

Electrical Characteristics (Ta = 25°C, V_{DD} = MV_{DD} = AV_{DD} = DV_{DD} = XV_{DD} = 5 V, $2V_{REF}$ = $P2V_{REF}$ = 4.2 V, V_{REF} = PV_{REF} = 2.1 V, unless otherwise specified)

MV_{DD} (CPU unit power supply)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating supply voltage	MV_{DD1}	—	When CPU and CD operating. However, $MV_{DD} \geq V_{DD}$ (Note 5)	4.5	5.0	5.5	V
	MV_{DD2}	—	When CPU operating (CD powered off, 4.5 MHz crystal connected) (Note 5)	4.5	5.0	5.5	
	MV_{DD3}	—	When CPU operating (CD powered off, 75 kHz crystal connected) (Note 5)	2.7	5.0	5.5	
Memory retention voltage range	MVHD	—	When crystal oscillator stopped (CKSTP instruction executed) (Note 5)	2.0	~	5.5	V
Operating supply current	MV_{DD1}	—	When CPU operating (XI = 16.9344 MHz crystal connected)	—	1.0	2.0	mA
	MV_{DD2}	—	When CPU operating(MXI = 4.5 MHz crystal connected)	—	2.0	4.0	
	MV_{DD3}	—	When CPU operating (MXI = 75 kHz crystal connected)	—	0.75	2.0	
	MV_{DD4}	—	Standby mode (only crystal oscillating, 4.5 MHz or 75 kHz crystal connected)	—	0.5	15	
Memory retention current	MIHD	—	When crystal oscillator stopped (CKSTP instruction executed)	—	0.1	1.0	μA
Crystal oscillation frequency	f MXT1	—	Rf = 1 MΩ, Rout = 0 Ω, Ci = Co = 30 pF (Note 5, 6)	—	4.5	—	MHz
	f MXT2	—	Rf = 10 MΩ, Rout = 100 kΩ, Ci = Co = 15 pF, MV_{DD} = 2.7~5.5 V (Note 5, 6)	—	75	—	kHz
Crystal oscillation start time	tst	—	Crystal oscillation fmxt = 75 kHz	—	—	1.0	s

Note 5: Guaranteed at V_{DD} = MV_{DD} = 4.5 to 5.5 V and Ta = −40 to 85°C

Note 6: Consider the crystal resonator used in your system when determining constants, etc.

V_{DD} (CD unit power supply)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating supply voltage	V_{DD}	—	$MV_{DD} \geq V_{DD}$ (Note 5)	4.5	5.0	5.5	V
Operating supply current	I_{DD}	—	When 16.9344 MHz crystal connected	—	50	60	mA
Crystal oscillation frequency	f_{XT}	—	Rout = 0 Ω, Ci = Co = 15 pF (Note 5, 6)	—	16.9344	—	MHz

Note 5: Guaranteed at $V_{DD} = MV_{DD} = 4.5$ to 5.5 V and Ta = −40 to 85°C

Note 6: Consider the crystal resonator used in your system when determining constants, etc.

LCD Common Output (COM1/OT1 to COM4/OT4)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	High level	I_{OH2}	—	V_{OH} = 4.5 V (When LCD output, settings OT output, LEDon = 0)	−0.1	−0.2	—	mA
		I_{OH5}	—	V_{OH} = 4.5 V (Settings OT output, LEDon = 1)	−20	−40	—	
	Low level	I_{OL2}	—	V_{OL} = 0.5 V (When LCD output, settings OT output, LEDon = 0)	0.1	0.2	—	
		I_{OL5}	—	V_{OL} = 0.5 V (Settings OT output, LEDon = 1)	4	10	—	
Output voltage 1/2 level		V_{BS}	—	Nonloaded (when LCD output)	2.1	2.3	2.5	V

Segment Output (S1/OT4 to S10/OT14, S11/OT15 to P8-0/S14 to P8-3/S18)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	High level	I_{OH1}	—	V_{OH} = 4.5 V (When LCD output, settings OT output, LEDon = 0)	−0.05	−0.1	—	mA
		I_{OH4}	—	V_{OH} = 4.5 V (Settings OT output, LEDon = 1, I/O port)	−2	−4	—	
	Low level	I_{OL1}	—	V_{OL} = 0.5 V (When LCD output, settings OT output, LEDon = 0)	0.05	0.1	—	
		I_{OL5}	—	V_{OL} = 0.5 V (Settings OT output, LEDon = 1, I/O port)	5	10	—	
Input leakage current		I_{LI}	—	V_{IH} = 5.0 V, V_{IL} = 0 V (P8-0 to P8-3)	—	—	±1.0	μA
Input voltage	High level	V_{IH}	—	(P8-0 to P8-3)	MV_{DD} × 0.8	~	MV_{DD}	V
	Low level	V_{IL}	—	(P8-0 to P8-3)	0	~	MV_{DD} × 0.2	

I/O Ports (P1-0 to P4-3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	High level	I_{OH3}	—	V_{OH} = 4.5 V	−1	−2	—	mA
	Low level	I_{OL3}	—	V_{OL} = 0.5 V (exclude P4-1, 2, 3 pin)	1.5	3.0	—	
		I_{OL5}	—	V_{OL} = 0.5 V (P4-1, 2, 3 pin)	4	10	—	
Input leakage current		I_{LI}	—	V_{IH} = 5.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	High level	V_{IH}	—	—	MV_{DD} × 0.8	~	MV_{DD}	V
	Low level	V_{IL}	—	—	0	~	MV_{DD} × 0.2	
Input pullup/down resistance		R_{IN1}	—	(P1-0 to P1-3) When pulldown, pullup are set.	25	50	120	kΩ

$\overline{\text{HOLD}}$, INTR Input Port, $\overline{\text{RESET}}$ Input

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input leakage current		I_{LI}	—	V_{IH} = 5.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	High level	V_{IH3}	—	—	MV_{DD} × 0.8	~	MV_{DD}	V
	Low level	V_{IL3}	—	—	0	~	MV_{DD} × 0.2	

A/D Converter (AD_{IN1} to AD_{IN4})

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog input voltage range	V_{AD}	—	AD_{IN} to AD_{IN4}	0	~	MV_{DD}	V
Resolution	V_{RES}	—	—	—	6	—	bit
Overall conversion error	—	—	—	—	±0.5	±4.0	LSB
Analog input leakage	I_{LI}	—	V_{IH} = 5.0 V, V_{IL} = 0 V (AD_{IN1} to AD_{IN4})	—	—	±1.0	μA

DATA, SFSY, LRCK, BCK, AOUT, MBOV, IPF Outputs and CLCK Input/Output

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	High level	I_{OH4}	—	V_{OH} = 4.5 V (Settings OT for output, LEDon = 0)	−2.0	−4.0	—	mA
	Low level	I_{OL5}	—	V_{OL} = 0.5 V (Settings OT for output, LEDon = 0)	5	10	—	
Input leakage current		I_{LI}	—	V_{IH} = 5.0 V, V_{IL} = 0 V (CLCK)	—	—	±1.0	μA
Input voltage	High level	V_{IH}	—	(CLCK)	MV_{DD} × 0.8	~	MV_{DD}	V
	Low level	V_{IL}	—	(CLCK)	0	~	MV_{DD} × 0.2	

DOUT, SBSY, SBOK, SEL, HSO, SPCK, SPDA, COFS Outputs

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output voltage	High level	I_{OH4}	—	V_{OH} = 4.5 V	−2	−4	—	mA
	Low level	I_{OL4}	—	V_{OL} = 0.5 V	2	4	—	

PDO, TMAX, RFGC, TEBC, DMO Outputs

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output voltage	High level	I_{OH6}	—	V_{OH} = 3.8 V	−1.0	−2.0	—	mA
	Low level	I_{OL4}	—	V_{OL} = 0.5 V	3.0	6.0	—	

Propagation Delay Time (AOUT, SPDA, DATA, SBSY, SBOK)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time	High level	t_{pLH}	—	—	—	10	—	ns
	Low level	t_{pHL}	—	—	—	10	—	

1bit DA Converter

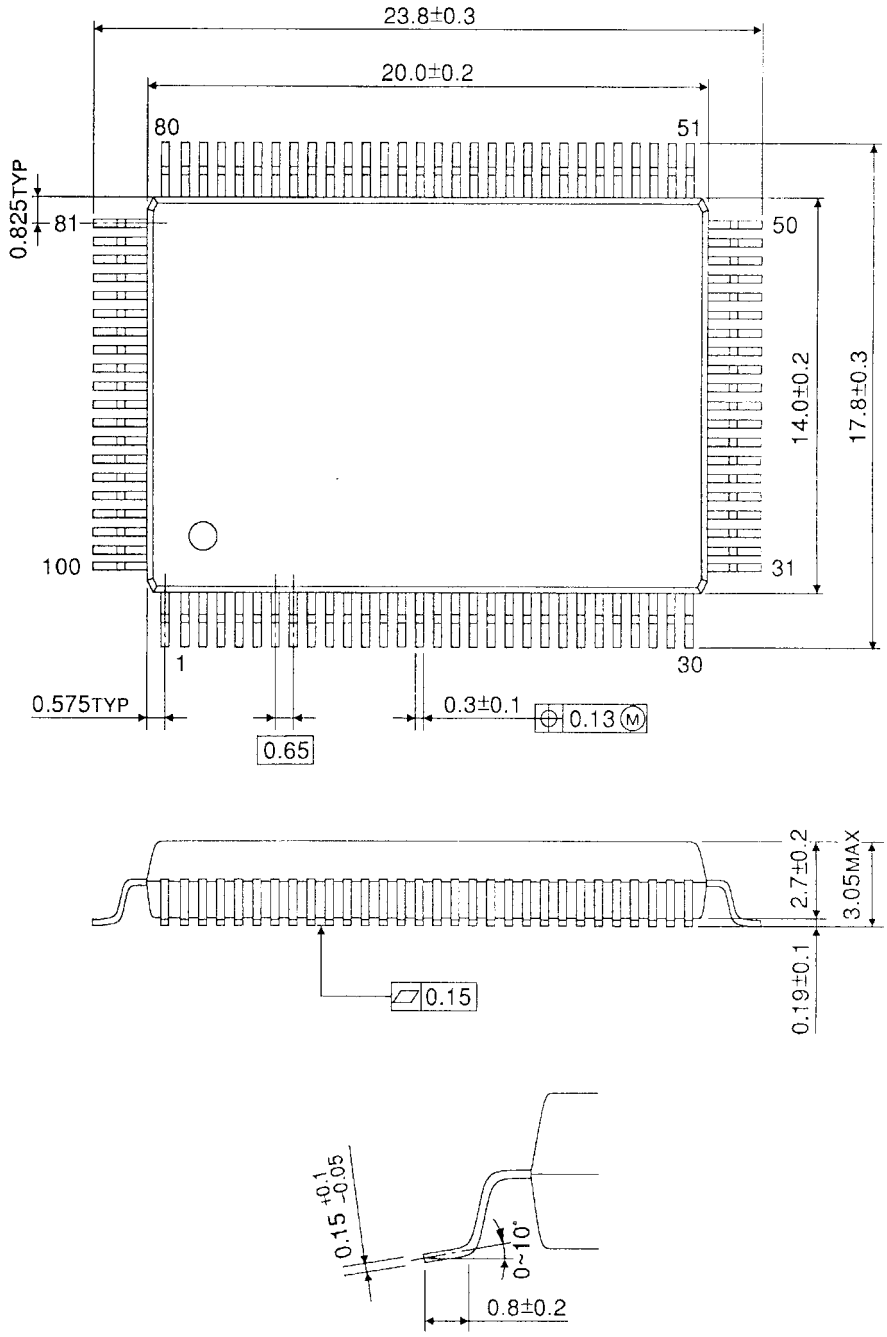
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Noise distortion	THD + N	—	1 kHz sine-wave, full-scale input	—	−85	−78	dB
S/N ratio	S/N	—	—	90	98	—	dB
Dynamic range	DR	—	1 kHz sine-wave, −60 dB input conversion	85	90	—	dB
Crosstalk	CT	—	1 kHz sine-wave, full-scale input	—	−90	−85	dB
Analog output level	DACout	—	1 kHz sine-wave, full-scale input	1200	1250	1300	mVrms

Other

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input pulldown resistance	R_{IN2}	—	(TEST0 to TEST5)	—	10	—	kΩ
XI amp feedback resistance	R_{fXT}	—	(XI−XO)	1	2	4	MΩ

Package Dimensions

QFP100-P-1420-0.65A Unit : mm



Weight: 1.6 g (typ.)

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