DATA SHEET

DAC-08 SERIES
8-bit high-speed multiplying D/A converter

Philips
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8-bit high-speed multiplying D/A converter

DAC-08 Series

DESCRIPTION

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 70 ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 20-to-1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All DAC-08 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range. Device performance is essentially unchanged over the ±4.5 V to ±18 V power supply range, with 37 mW power consumption attainable at ±5 V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military aerospace applications.

FEATURES

- Fast settling output current—70 ns

- Full-scale current prematched to ±1 LSB

- Direct interface to TTL, CMOS, ECL, HTL, PMOS

- Relative accuracy to 0.1% maximum over temperature range

- High output compliance -10 V to $+18$ V

- True and complemented outputs

- Wide range multiplying capability

- Low FS current drift — ±10ppm/°C

- Wide power supply range—±4.5 V to ±18 V

- Low power consumption—37 mW at ±5 V

APPLICATIONS

- 8-bit, 1 μs A-to-D converters

- Servo-motor and pen drivers

- Waveform generators

- Audio encoders and attenuators

- Analog meter drivers

- Programmable power supplies

- CRT display drivers

- High-speed modems

- Other applications where low cost, high speed and complete input/output versatility are required

- Programmable gain and attenuation

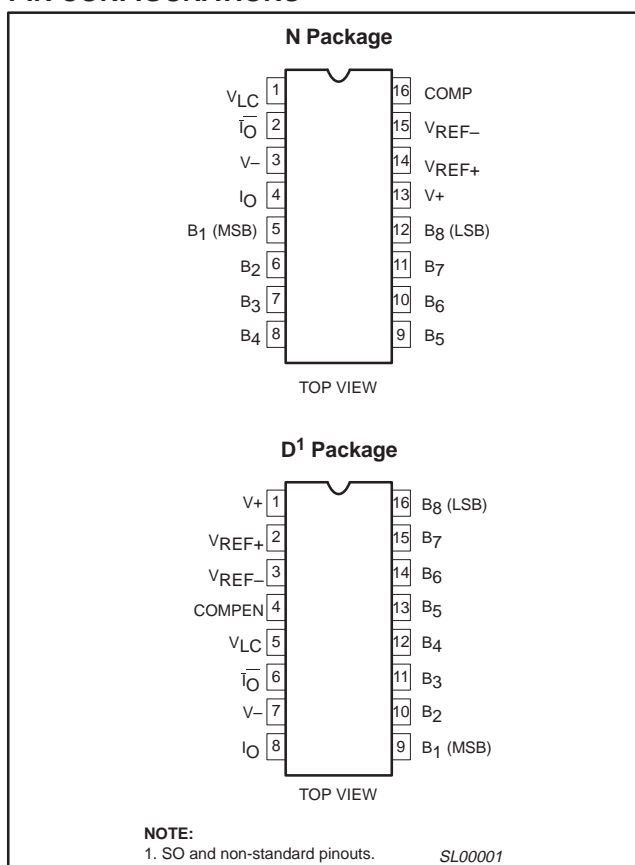- Analog-Digital multiplication

PIN CONFIGURATIONS

N Package

Pin		Pin	
V_{LC}	1	16	COMP
$\overline{I_O}$	2	15	V_{REF-}
$V-$	3	14	V_{REF+}
I_O	4	13	$V+$
B_1 (MSB)	5	12	B_8 (LSB)
B_2	6	11	B_7
B_3	7	10	B_6
B_4	8	9	B_5

TOP VIEW

D[1] Package

Pin		Pin	
$V+$	1	16	B_8 (LSB)
V_{REF+}	2	15	B_7
V_{REF-}	3	14	B_6
COMPEN	4	13	B_5
V_{LC}	5	12	B_4
$\overline{I_O}$	6	11	B_3
$V-$	7	10	B_2
I_O	8	9	B_1 (MSB)

TOP VIEW

NOTE:
1. SO and non-standard pinouts.

SL00001

Figure 1. Pin Configuration

ORDERING INFORMATION

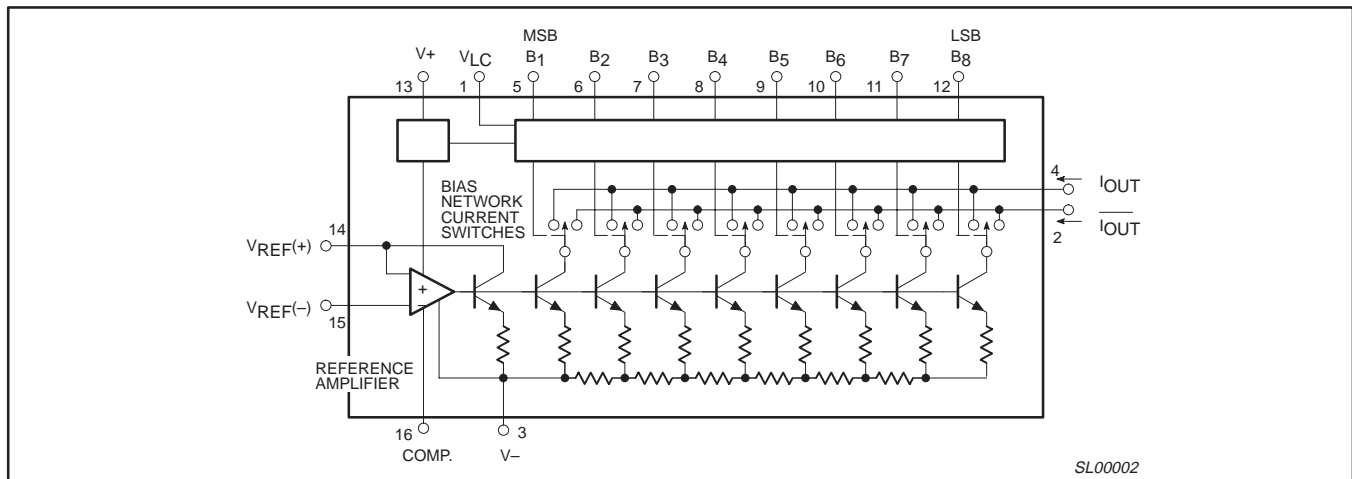| DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	DAC-08CN	SOT38-4
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	DAC-08EN	SOT38-4
16-Pin Plastic Small Outline (SO) Package	0 to +70°C	DAC-08ED	SOT109-1
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	DAC-08HN	SOT38-4

BLOCK DIAGRAM

Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V+ to V–	Power supply voltage	36	V
V_5–V_{12}	Digital input voltage	V– to V– plus 36 V	
V_{LC}	Logic threshold control	V– to V+	
V_0	Applied output voltage	V– to +18	V
I_{14}	Reference current	5.0	mA
V_{14}, V_{15}	Reference amplifier inputs	V_{EE} to V_{CC}	
P_D	Maximum power dissipation T_{amb} = 25 °C (still-air)[1] N package D package	 1450 1090	 mW mW
T_{SOLD}	Lead soldering temperature (10 sec max)	230	°C
T_{amb}	Operating temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTE:
1. Derate above 25 °C, at the following rates:
    N package at 11.6mW/°C
    D package at 8.7mW/°C

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DC ELECTRICAL CHARACTERISTICS

Pin 3 must be at least 3 V more negative than the potential to which R_{15} is returned. $V_{CC} = \pm15V$, $I_{REF} = 2.0$ mA.
Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$ unless otherwise noted. $T_{amb} = 0$ °C to 70 °C.

SYMBOL	PARAMETER	TEST CONDITIONS	DAC-08C			DAC-08E			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy	Over temperature range			±0.39			±0.19	%FS
	Differential non-linearity				±0.78			±0.39	%FS
TCI_{FS}	Full-scale tempco			±10			±10		ppm/°C
V_{OC}	Output voltage compliance	Full-scale current change< 1/2LSB	−10		+18	−10		+18	V
I_{FS4}	Full-scale current	$V_{REF} = 10.000V$; $R_{14}, R_{15} = 5.000$ kΩ	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full-scale symmetry	I_{FS4}-I_{FS2}		±2.0	±16		±1.0	±8.0	µA
I_{ZS}	Zero-scale current			0.2	4.0		0.2	2.0	µA
I_{FSR}	Full-scale output current range	$R_{14}, R_{15} = 5.000$ kΩ $V_{REF} = +15.0$ V, V− = −10 V $V_{REF} = +25.0$ V, V− = −12 V	2.1 4.2			2.1 4.2			mA mA
V_{IL} V_{IH}	Logic input levels Low High	$V_{LC} = 0$ V	2.0		0.8	2.0		0.8	V V
I_{IL} I_{IH}	Logic input current Low High	$V_{LC} = 0$ V $V_{IN} = −10$ V to +0.8 V $V_{IN} = 2.0$ V to 18 V		−2.0 0.002	−10 10		−2.0 0.002	−10 10	µA µA
V_{IS}	Logic input swing	V− = −15 V	−10		+18	−10		+18	V
V_{THR}	Logic threshold range	$V_S = \pm15$ V	−10		+13.5	−10		+13.5	V
I_{15}	Reference bias current			−1.0	−3.0		−1.0	−3.0	µA
dI/dt	Reference input slew rate		4.0	8.0		4.0	8.0		mA/µs
$PSSI_{FS+}$ $PSI_{FS−}$	Power supply sensitivity Positive Negative	$I_{REF} = 1$ mA V+ = 4.5 to 5.5 V, V− = −15 V; V+ = 13.5 to 16.5 V, V− = −15 V V− = −4.5 to −5.5 V, V+ = +15 V; V− = −13.5 to −16.5 V, V+ = +15 V		0.0003 0.002	0.01 0.01		0.0003 0.002	0.01 0.01	%FS/%VS %FS/%VS
I+ I−	Power supply current Positive Negative	$V_S = \pm5$ V, $I_{REF} = 1.0$ mA		3.1 −4.3	3.8 −5.8		3.1 −4.3	3.8 −5.8	mA mA
I+ I−	Positive Negative	$V_S = +5$ V, −15 V, $I_{REF} = 2.0$ mA		3.1 −7.1	3.8 −7.8		3.1 −7.1	3.8 −7.8	mA mA
I+ I−	Positive Negative	$V_S = \pm15$ V, $I_{REF} = 2.0$ mA		3.2 −7.2	3.8 −7.8		3.2 −7.2	3.8 −7.8	mA mA
P_D	Power dissipation	±5 V, $I_{REF} = 1.0$ mA +5 V, −15 V, $I_{REF} = 2.0$ mA ±15 V, $I_{REF} = 2.0$ mA		37 122 156	48 136 174		37 122 156	48 136 174	mW mW mW

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DC ELECTRICAL CHARACTERISTICS (Continued)

Pin 3 must be at least 3 V more negative than the potential to which R_{15} is returned. V_{CC} = +15 V, I_{REF} = 2.0 mA.
Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$, unless otherwise noted. T_{amb} = 0 °C to 70 °C.

SYMBOL	PARAMETER	TEST CONDITIONS	DAC-08H			UNIT
			Min	Typ	Max	
	Resolution		8	8	8	Bits
	Monotonicity		8	8	8	Bits
	Relative accuracy	Over temperature range			±0.1	%FS
	Differential non-linearity				±0.19	%FS
TCI_{FS}	Full-scale tempco			±10	±50	ppm/°C
V_{OC}	Output voltage compliance	Full-scale current change 1/2LSB	−10		+18	V
I_{FS4}	Full-scale current	V_{REF} = 10.000 V, R_{14}, R_{15} = 5.000 kΩ	1.984	1.992	2.000	mA
I_{FSS}	Full-scale symmetry	I_{FS4}–I_{FS2}		±1.0	±4.0	μA
I_{ZS}	Zero-scale current			0.2	1.0	μA
I_{FSR}	Full-scale output current range	R_{14}, R_{15} = 5.000 kΩ				
		V_{REF} = +15.0 V, V− = −10 V	2.1			mA
		V_{REF}=+25.0V, V−=−12V	4.2			mA
	Logic input levels	V_{LC} = 0 V				
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
	Logic input current	V_{LC} = 0 V				
I_{IL}	Low	V_{IN} = −10 V to +0.8 V		−2.0	−10	μA
I_{IH}	High	V_{IN} = 2.0 V to 18 V		0.002	10	μA
V_{IS}	Logic input swing	V− = −15 V	−10		+18	V
V_{THR}	Logic threshold range	V_S = ±15 V	−10		+13.5	V
I_{15}	Reference bias current			−1.0	−3.0	μA
dI/dt	Reference input slew rate		4.0	8.0		mA/μs
	Power supply sensitivity	I_{REF} = 1 mA				
$PSSI_{FS+}$	Positive	V+ = 4.5 to 5.5 V, V− = −15 V; V+ = 13.5 to 16.5 V, V− = −15 V		0.0003	0.01	%FS/%VS
$PSI_{FS−}$	Negative	V− = −4.5 to −5.5 V, V+ = +15 V; V− = −13.5 to −16.5 V, V+ = +15 V		0.002	0.01	%FS/%VS
	Power supply current					
I+	Positive	V_S = ±5 V, I_{REF} = 1.0 mA		3.1	3.8	mA
I−	Negative			−4.3	−5.8	mA
I+	Positive	V_S = +5 V, −15 V, I_{REF} = 2.0 mA		3.1	3.8	mA
I−	Negative			−7.1	−7.8	mA
I+	Positive	V_S = ±15 V, I_{REF} = 2.0 mA		3.2	3.8	mA
I−	Negative			−7.2	−7.8	mA
P_D	Power dissipation	±5 V, I_{REF} = 1.0 mA		37	48	mW
		+5 V, −15 V, I_{REF} = 2.0 mA		122	136	mW
		±15 V, I_{REF} = 2.0 mA		156	174	mW

AC ELECTRICAL CHARACTERISTICS

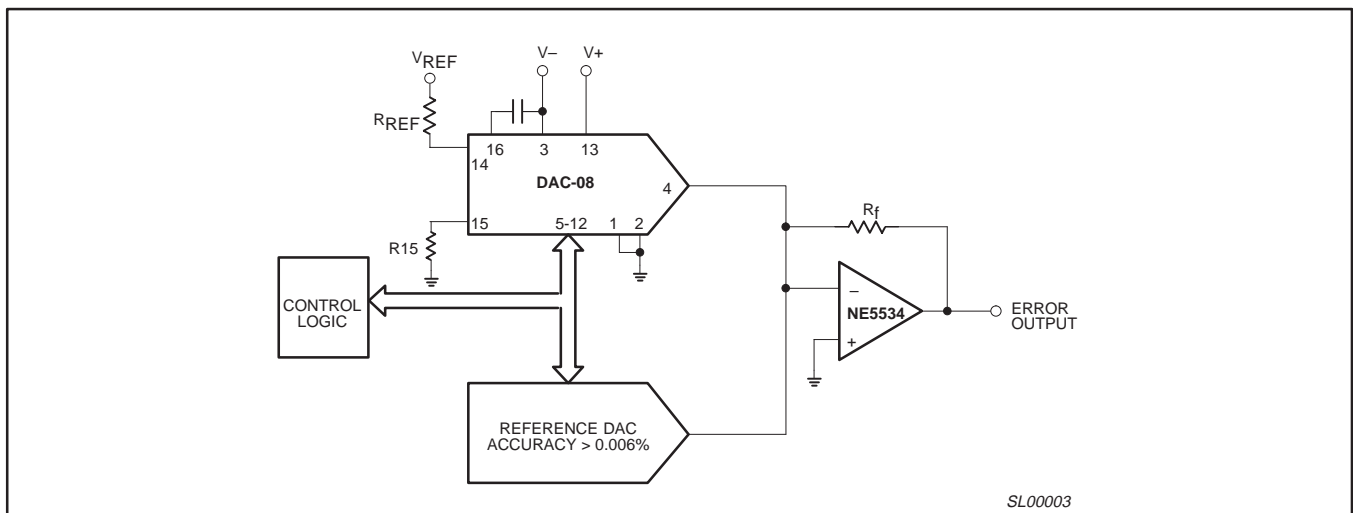| SYMBOL	PARAMETER	TEST CONDITIONS	DAC-08C			DAC-08E			DAC-08H			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_S	Settling time	To ± 1/2LSB, all bits switched on or off, T_{amb} = 25 °C		70	135		70	135		70	135	ns
t_{PLH}	Propagation delay Low-to-High	T_{amb} = 25 °C, each bit.										ns
t_{PHL}	High-to-Low	All bits switched		35	60		35	60		35	60	

TEST CIRCUITS

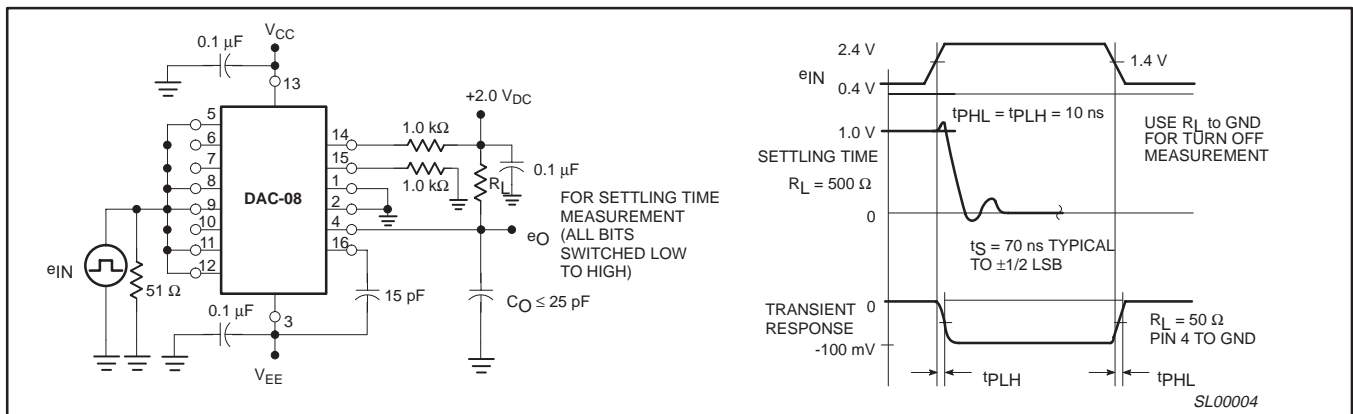**Figure 3. Relative Accuracy Test Circuit**

Figure 4. Transient Response and Settling Time

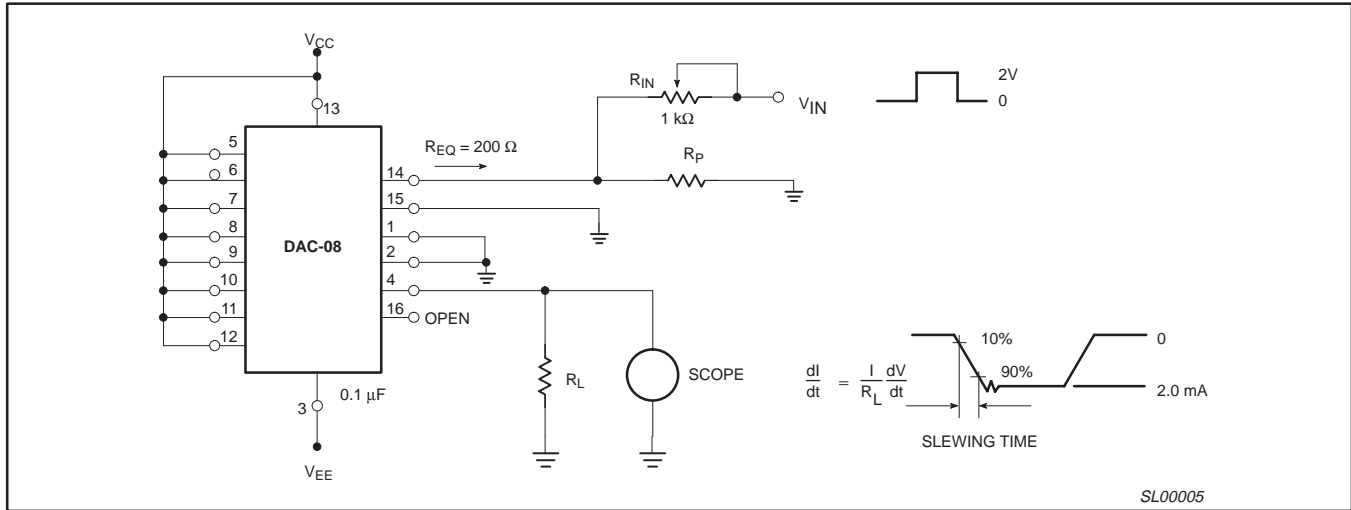# 8-bit high-speed multiplying D/A converter

DAC-08 Series

TEST CIRCUITS (Continued)
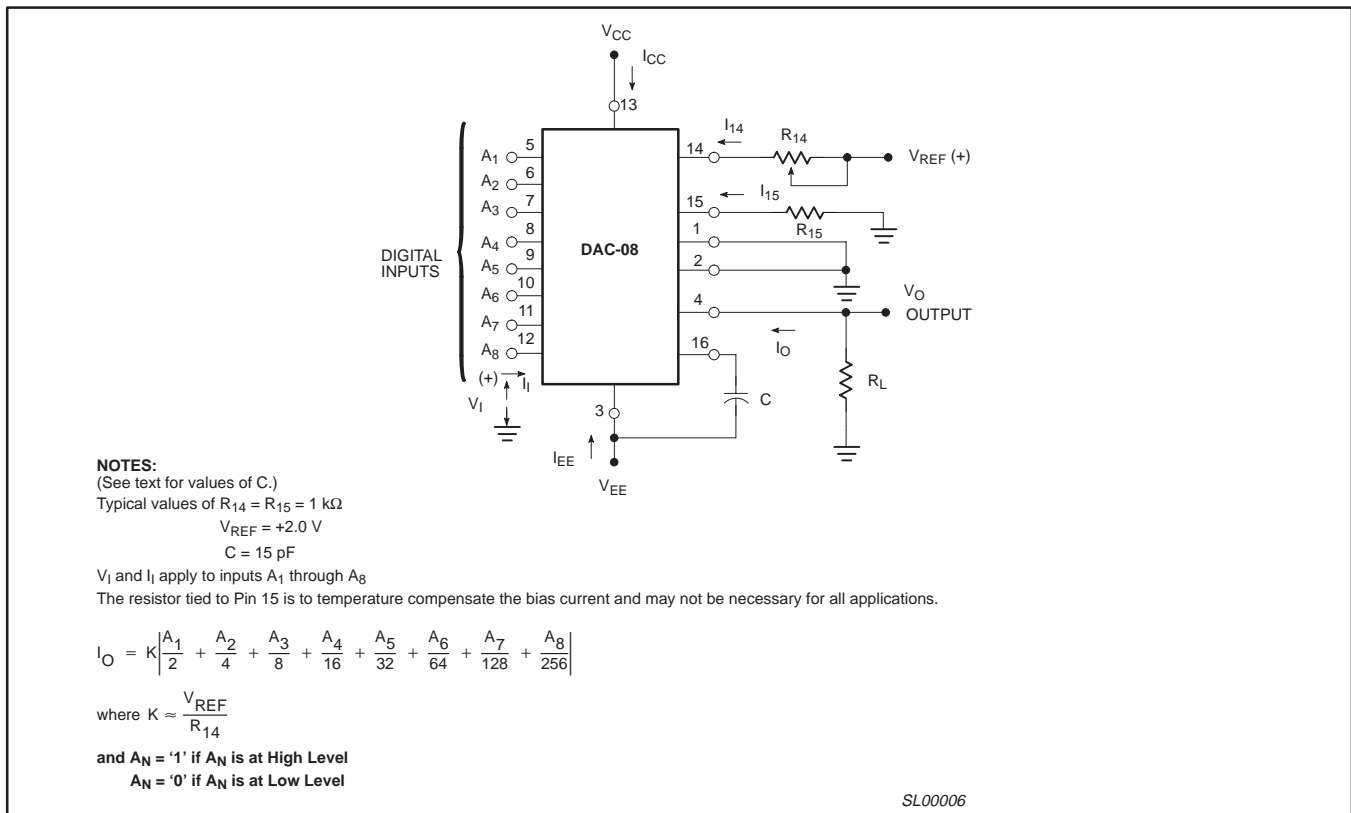

Figure 5. Reference Current Slew Rate Measurement

NOTES:
(See text for values of C.)
Typical values of $R_{14} = R_{15} = 1 k\Omega$
$V_{REF} = +2.0 V$
$C = 15 pF$
V_I and I_I apply to inputs A_1 through A_8
The resistor tied to Pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K \left| \frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right|$$

where $K \approx \dfrac{V_{REF}}{R_{14}}$

and A_N = '1' if A_N is at High Level
A_N = '0' if A_N is at Low Level

SL00006

Figure 6. Notation Definitions

8-bit high-speed multiplying D/A converter
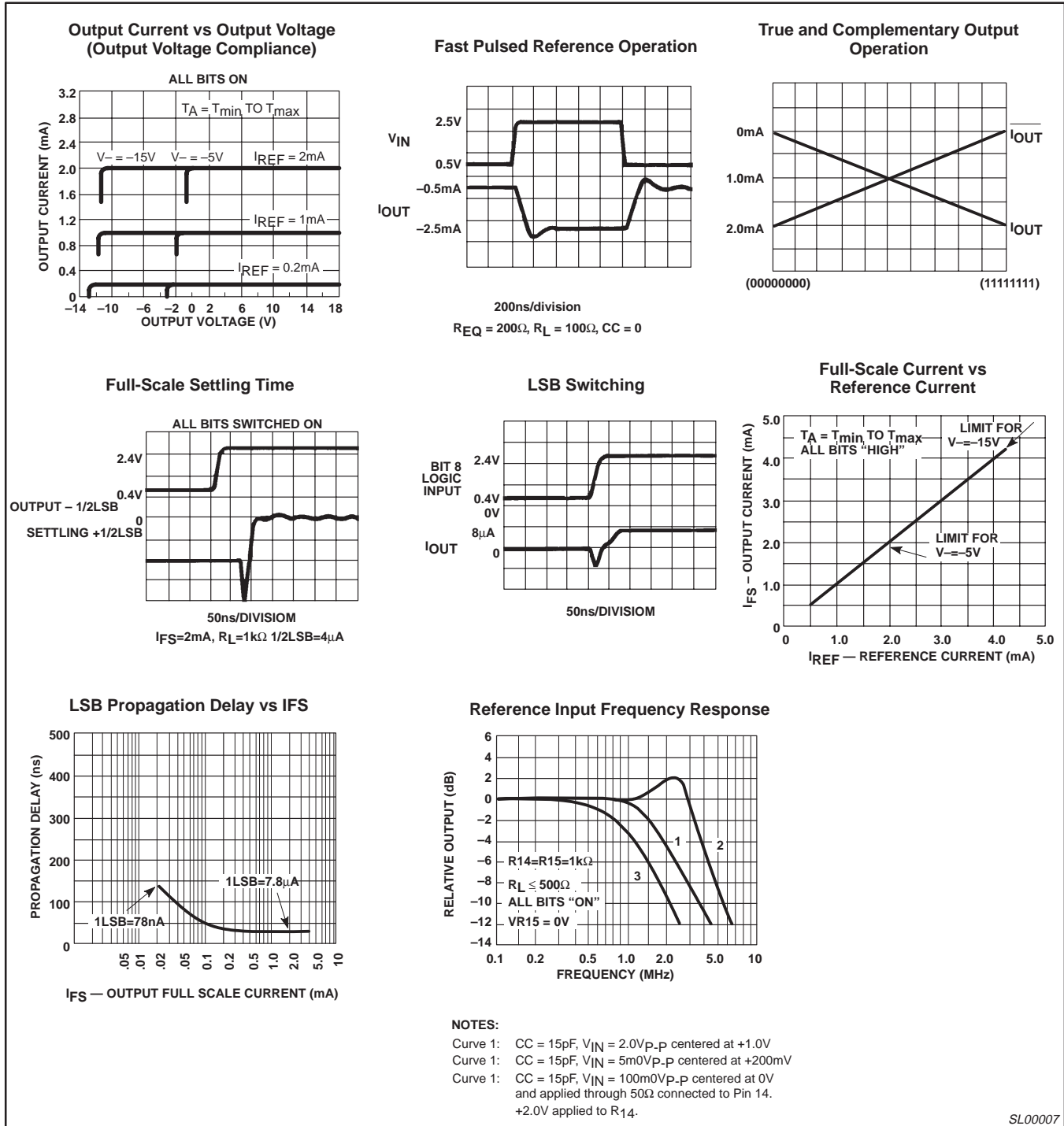
DAC-08 Series

TYPICAL PERFORMANCE CHARACTERISTICS

Output Current vs Output Voltage (Output Voltage Compliance)

Fast Pulsed Reference Operation

True and Complementary Output Operation

Full-Scale Settling Time

LSB Switching

Full-Scale Current vs Reference Current

LSB Propagation Delay vs IFS

Reference Input Frequency Response

NOTES:
Curve 1: CC = 15pF, V_{IN} = 2.0V$_{P-P}$ centered at +1.0V
Curve 1: CC = 15pF, V_{IN} = 5m0V$_{P-P}$ centered at +200mV
Curve 1: CC = 15pF, V_{IN} = 100m0V$_{P-P}$ centered at 0V
and applied through 50Ω connected to Pin 14.
+2.0V applied to R_{14}.

SL00007

Figure 7. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

**Reference AMP Common-Mode Range
All Bits On**

Logic Input Current vs Input Voltage

$V_{TH} - V_{LC}$ vs Temperature

**Output Voltage Compliance
vs Temperature**

Shaded area indicates
permissible output voltage
range for V– = -15V, $I_{REF} \leq 2.0$mA
For other V– or I_{REF}
See "Output Current vs Output
Voltage" curve on previous page

Bit Transfer Characteristics

Power Supply Current vs V+

NOTES:

B_1 through B_8 have identical transfer characteristics.
Bits are fully switched, with less than 1/2LSB error, at
less than ±100mV from actual threshold. These
switching points are guaranteed to lie between 0.8 and
2.0V over the operating temperature range
($V_{LC} = 0.0$V).

Power Supply Current vs V–

Power Supply Current vs Temperature

**Maximum Reference Input Frequency
vs Compensation Capacitor Value**

SL00008

Figure 8. Typical Performance Characteristics (cont.)

TYPICAL APPLICATION

Pulsed Referenced Operation   SL00009

NOTES:
REQ = $R_{IN} \| R_P$
Typical Values
R_{IN} = 5kΩ
+V_{IN} = 10V

Figure 9. Typical Application

FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier input current must always flow into Pin 14 regardless of the setup method or reference supply voltage polarity.

Connections for a positive reference voltage are shown in Figure 3. The reference voltage source supplies the full reference current. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. R_{15} may be eliminated with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased as R_{14} value is increased. This is in order to maintain proper phase margin. For R_{14} values of 1.0, 2.5, and 5.0 kΩ, minimum capacitor values are 15, 37, and 75 pF, respectively. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection. (Fluctuations in the negative supply have more effect on accuracy than do any changes in the positive supply.)

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3.0 V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at Pin 15.

When using a DC reference voltage, capacitive bypass to ground is recommended. The 5.0 V logic supply is not recommended as a reference voltage, but if a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be formed of two series resistors with the junction of the two resistors bypassed with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods applies and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage at Pin 4 must always be at least 4.5 V more positive than the voltage of the negative supply (Pin 3) when the reference current is 2 mA or less, and at least 8 V more positive than the negative supply when the reference current is between 2 mA and 4 mA. This is necessary to avoid saturation of the output transistors, which would cause serious accuracy degradation.

Output Current Range

Any time the full-scale current exceeds 2 mA, the negative supply must be at least 8 V more negative than the output voltage. This is due to the increased internal voltage drops between the negative supply and the outputs with higher reference currents.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy, full-scale accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current after zero-scale current has been nulled out. The relative accuracy of the DAC-08 series is essentially constant over the operating temperature range due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC-08 series has a very low full-scale current drift over the operating temperature range.

The DAC-08 series is guaranteed accurate to within $\pm$ LSB at +25 $^\circ$C at a full-scale output current of 1.992 mA. The relative accuracy test circuit is shown in Figure 3. The 12-bit converter is calibrated to a full-scale output current of 1.99219 mA, then the DAC-08 full-scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on the oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total of $\pm$ part in 65,536, or $\pm$0.00076%, which is much more accurate than the $\pm$0.19% specification of the DAC-08 series.

Monotonicity

A monotonic converter is one which always provides analog output greater than or equal to the preceding value for a corresponding increment in the digital input code. The DAC-08 series is monotonic for all values of reference current above 0.5 mA. The recommended range for operation is a DC reference current between 0.5 mA and 4.0 mA.

Settling Time

The worst-case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all input bits. This time is typically 70 ns for settling to within LSB for 8-bit accuracy. This time applies when R_L<500 Ω and C_O<25 pF. The slowest single switch is the least significant bit, which typically turns on and settles in 65 ns. In applications where the DAC functions in a positive-going ramp mode, the worst-case condition does not occur and settling times less than 70 ns may be realized.

Extra care must be taken in board layout since this usually is the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, minimum scope lead length, and avoidance of ground loops are all mandatory.

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SETTLING TIME AND PROPAGATION DELAY

NOTES:
D_1, D_2 = IN6263 or equivalent
D_3 = IN914 or equivalent
C_1 = 0.01μF
C_2, C_3 = 0.1μF
Q_1 = 2N3904
C_4, C_5 = 15pF and includes all probe and fixturing capacitance.

SL00010

Figure 10. Settling Time and Propagation Delay

BASIC DAC-08 CONFIGURATION

NOTES:

$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256} \; ; \; I_O + \overline{I}_O = I_{FS} \text{ for all logic states}$$

SL00011

Figure 11. Basic DAC-08 Configuration

RECOMMENDED FULL-SCALE AND ZERO-SCALE ADJUST

NOTES:
R_1 = low T.C.
$R_3 = R_1 + R_2$
$R_2 \approx 0.1\ R_1$ to minimize pot. contribution to full-scale drift

SL00012

Figure 12. Recommended Full-Scale and Zero-Scale Adjust

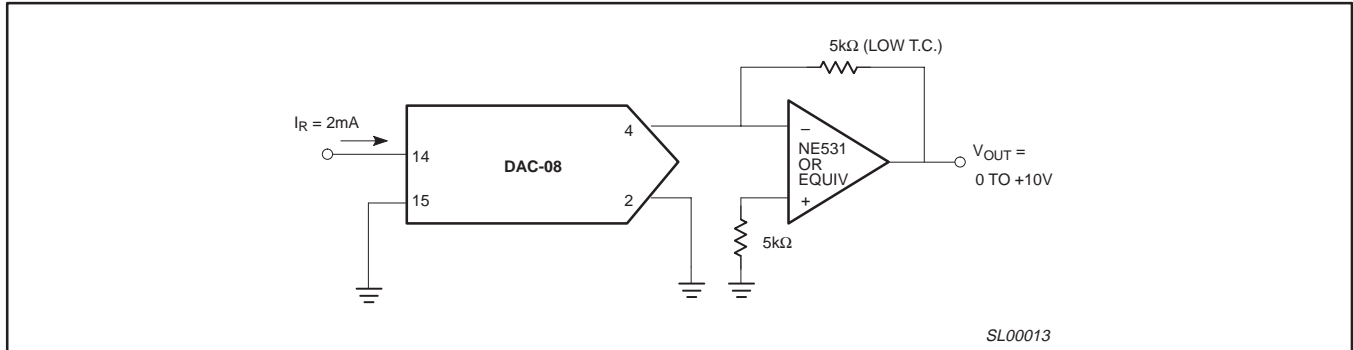## UNIPOLAR VOLTAGE OUTPUT FOR LOW IMPEDANCE OUTPUT

SL00013

Figure 13. Unipolar Voltage Output for Low Impedance Output

8-bit high-speed multiplying D/A converter

DAC-08 Series

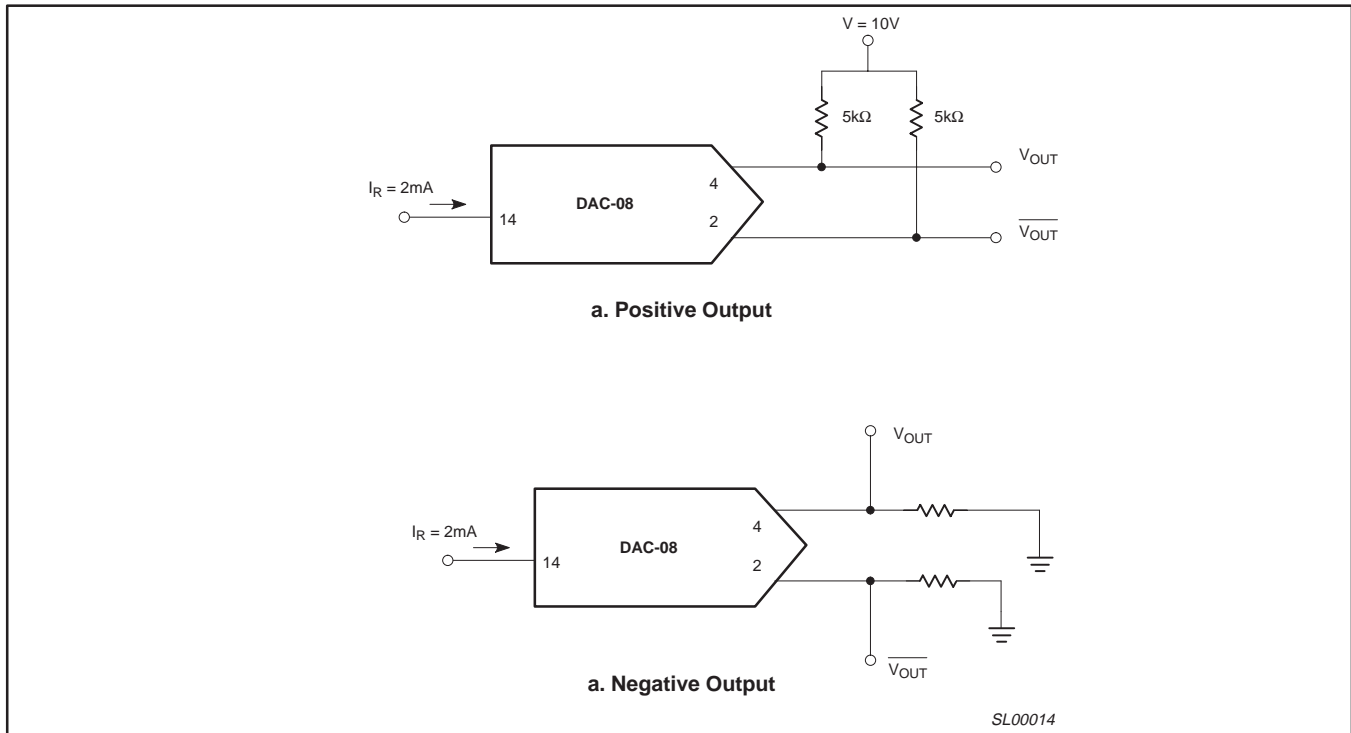**UNIPOLAR VOLTAGE OUTPUT FOR HIGH IMPEDANCE OUTPUT**

a. Positive Output

a. Negative Output

SL00014

Figure 14. Unipolar Voltage Output for High Impedance Output

BASIC BIPOLAR OUTPUT OPERATION (OFFSET BINARY)

	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	V_{OUT}	$\overline{V_{OUT}}$
Positive full-scale	1	1	1	1	1	1	1	1	−9.920V	+10.000
Positive FS – 1LSB	1	1	1	1	1	1	1	0	−9.840V	+9.920
+ Zero-scale + 1LSB	1	0	0	0	0	0	0	1	−0.080V	+0.160
Zero-scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero-scale – 1LSB	0	1	1	1	1	1	1	1	0.080	0.000
Negative full scale – 1LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Negative full scale	0	0	0	0	0	0	0	0	+10.000	−9.920

SL00015
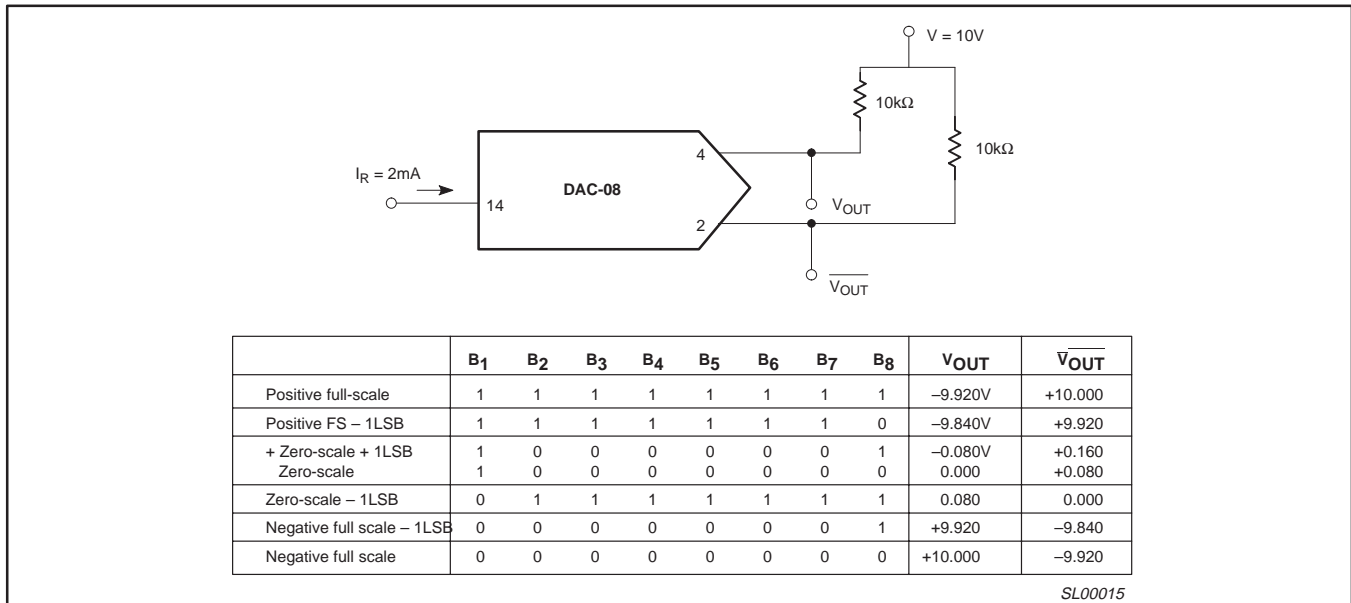
Figure 15. Basic Bipolar Output Operation (Offset Binary)

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

0   5   10 mm

scale
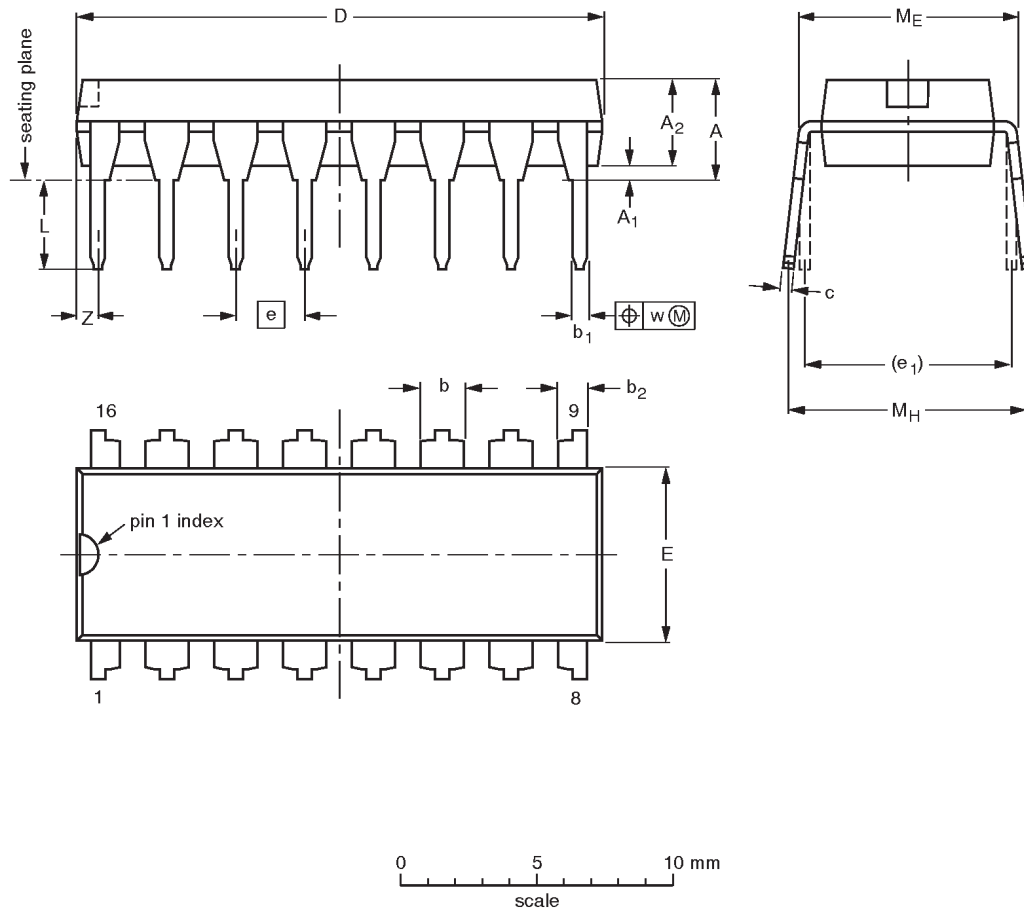
DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁ min.	A₂ max.	b	b₁	b₂	c	D $^{(1)}$	E $^{(1)}$	e	e₁	L	M_E	M_H	w	Z $^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

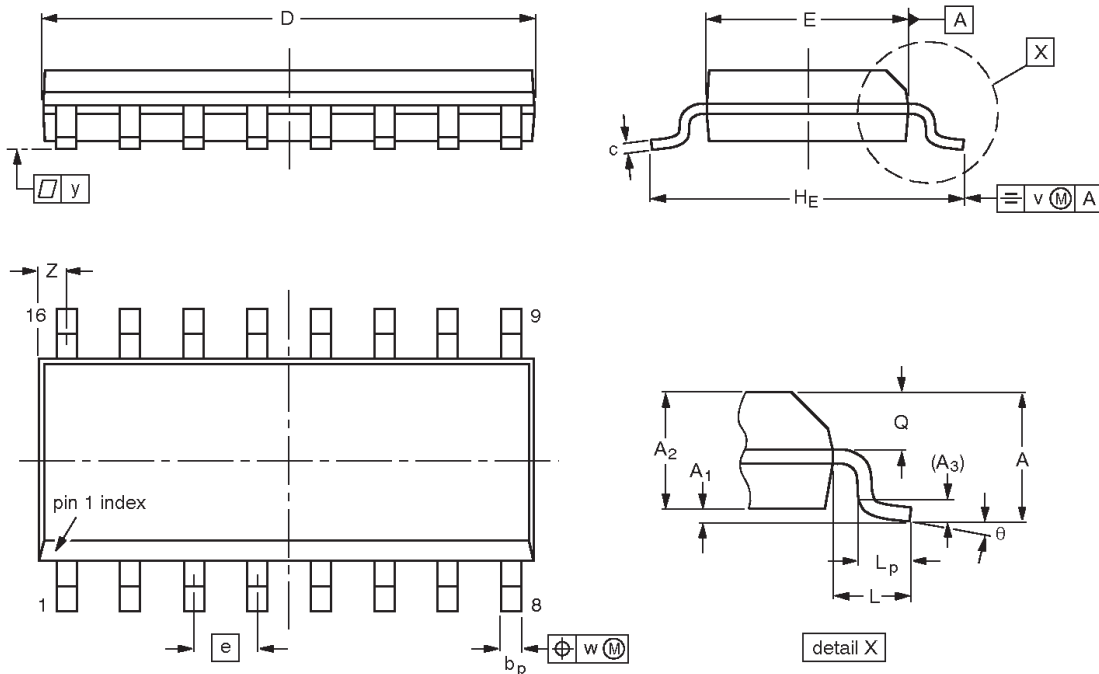1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

8-bit high-speed multiplying D/A converter

DAC-08 Series

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1


```
0        2.5       5 mm
|__|__|__|__|__|__|__|__|
        scale
```

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	E[1]	e	H_E	L	Lₚ	Q	v	w	y	Z[1]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	**JEDEC**	**EIAJ**			
SOT109-1	076E07	MS-012				~~97-05-22~~ 99-12-27

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1]   Please consult the most recently issued data sheet before initiating or completing a design.

[2]   The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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