Data Sheet | July 1999 | File Number 3141.2

Low Resistance, Single 8-Channel, and Differential 4-Channel, CMOS Analog Multiplexers

The HI-1818A and HI-1828A are monolithic, high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250Ω) assure optimum performance in low level or current mode applications.

The HI-1818A is a single-ended, 8-Channel multiplexer, while the HI-1828A is a differential 4-Channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

For MIL-STD-883 compliant parts, request the HI-1818A/883.

Features

- Signal Range . . . . . +15V
- "ON" Resistance 250Ω
- Input Leakage (Max) 50nA
- Access Time 350ns
- Power Consumption 5mW
- DTL/TTL Compatible Address
- Operation . . . . . -55^{o}C to 125^{o}C

Applications

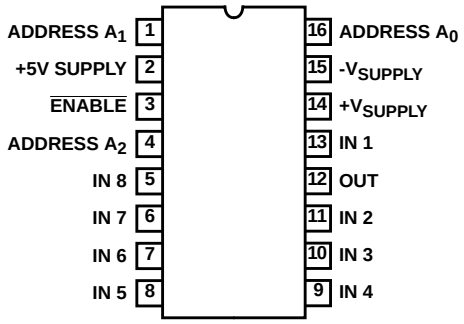
- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Ordering Information

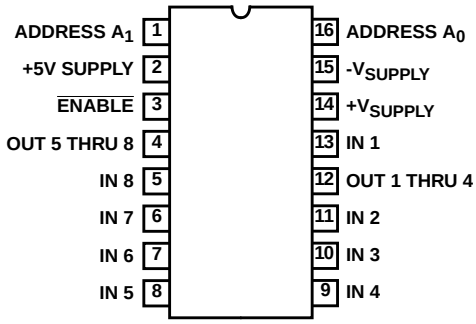
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI1-1818A-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-1818A-5	0 to 75	16 Ld CERDIP	F16.3
HI1-1828A-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-1828A-5	0 to 75	16 Ld PDIP	E16.3

Pinouts

HI-1818A (CERDIP)
TOP VIEW



HI-1828A (CERDIP, PDIP)
TOP VIEW



Truth Tables

HI-1818A TRUTH TABLE

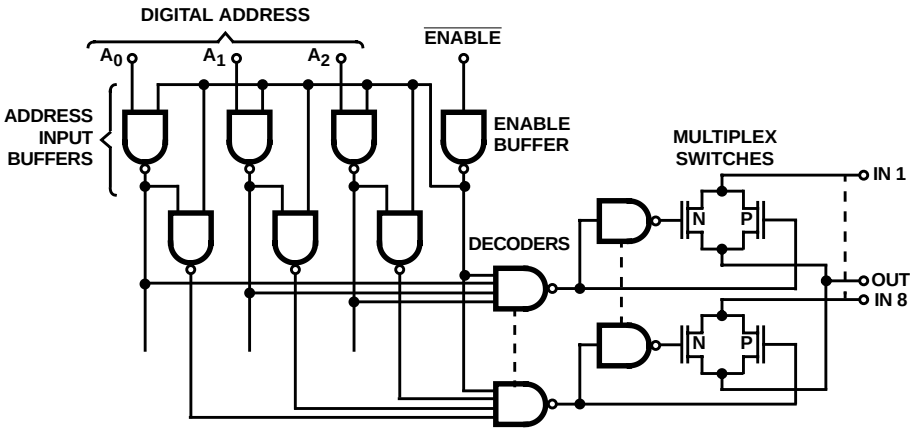
ADDRESS				
A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	None

HI-1828A TRUTH TABLE

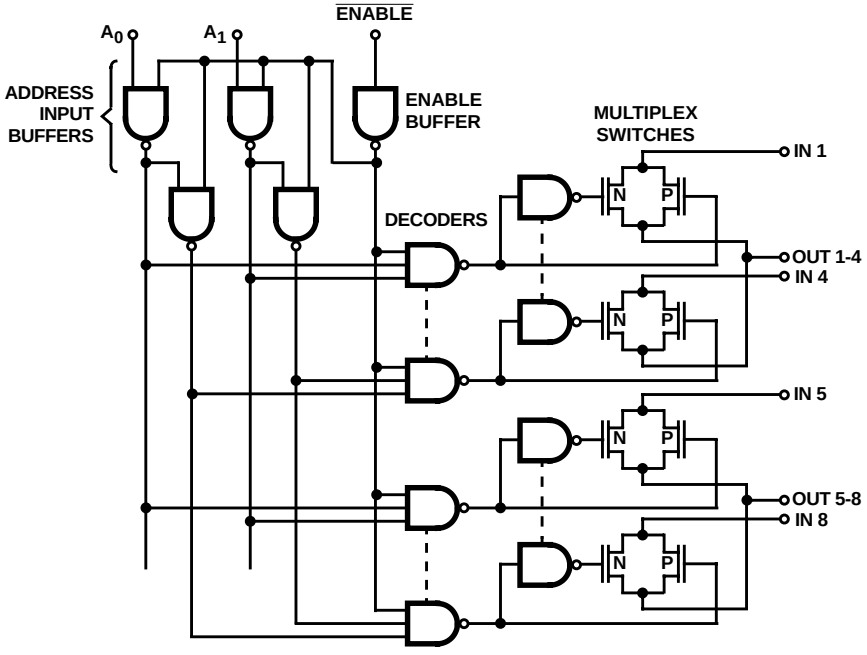
ADDRESS			
A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	None

Functional Block Diagrams

HI-1818A



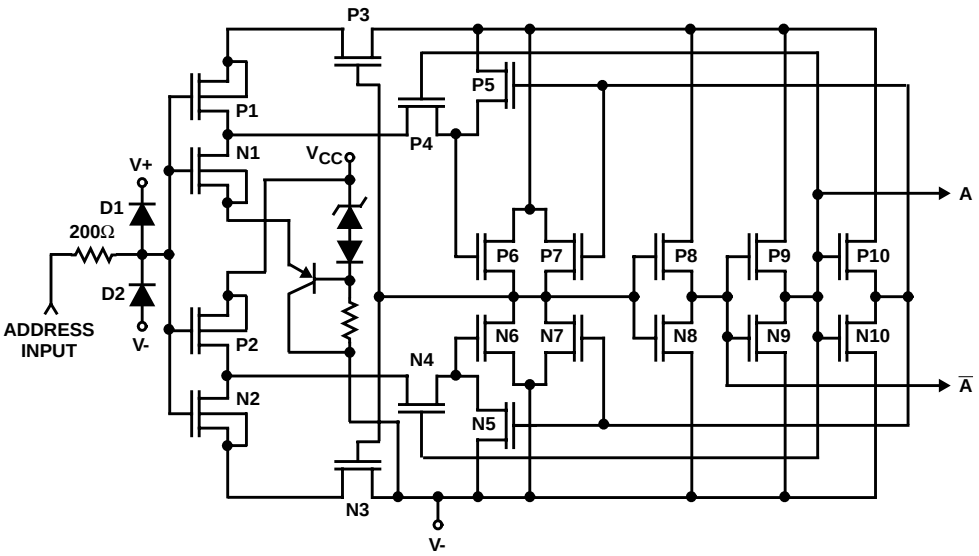
HI-1828A



Schematic Diagrams

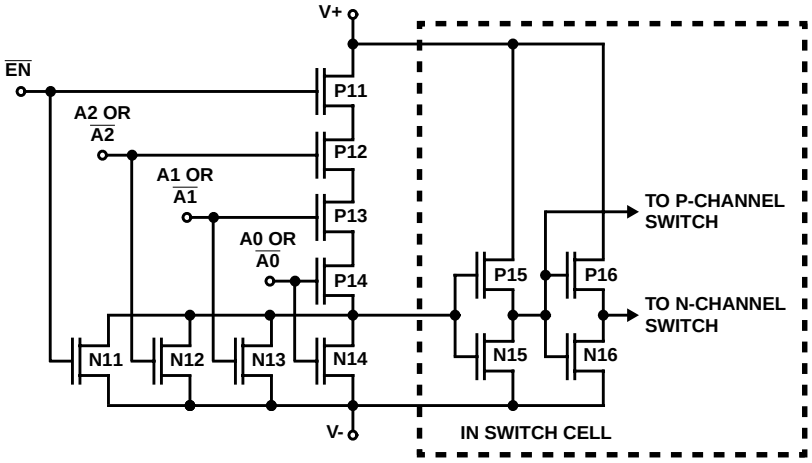
ADDRESS INPUT BUFFER

All N-Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Specified



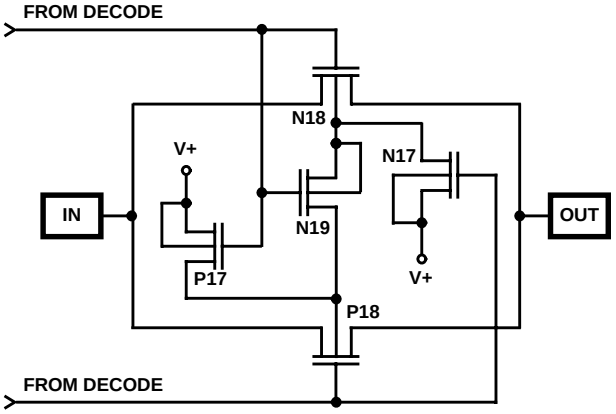
ADDRESS DECODER

All N-Channel Bodies to V-
All P-Channel Bodies to V+
A2 or $\overline{A2}$ not used for HI-1828A



MULTIPLEXER SWITCH

All N-Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Specified



Absolute Maximum Ratings

V+ to V- 40V
Logic Supply Voltage 30V
Analog Signal (V_{IN}, V_{OUT}) . . . . . (V-) -2V to (V+) +2V
Digital Input Voltage (V_{EN}, V_A) . . . . . (V-) to (V+)

Operating Conditions

Temperature Ranges
HI-1818A/HI-1828A-2 . . . . . -55^oC to 125^oC
HI-1818A/HI-1828A-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	85	32
PDIP Package	90	N/A

Maximum Junction Temperature
Ceramic Package . . . . . 175^oC
Plastic Package . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V, +5V; V_{AL} = 0.4V, V_{AH} = 4.0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	-2			-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC CHARACTERISTICS									
Access Time, t_A	Note 4	25	-	350	500	-	350	-	ns
		Full	-	-	1000	-	-	1000	ns
Break-Before-Make Delay, t_{OPEN}		25	-	25	-	-	100	-	ns
Enable Delay (ON), $t_{ON(EN)}$		25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$		25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Settling Time	To 0.1%	25	-	1.08	-	-	1.08	-	µs
	To 0.025%	25	-	2.8	-	-	2.8	-	µs
Channel Input Capacitance, $C_{S(OFF)}$		25	-	4	-	-	4	-	pF
Channel Output Capacitance, $C_{D(OFF)}$								-	
HI-1818A		25	-	20	-	-	20	-	pF
HI-1828A		25	-	10	-	-	10	-	pF
Input to Output Capacitance, $C_{DS(OFF)}$		25	-	0.6	-	-	0.6	-	pF
Digital Input Capacitance, C_A		25	-	5	-	-	5	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL}		Full	-	-	0.4	-	-	0.4	V
Input High Threshold, V_{AH}	Note 3	Full	4.0	-	-	4.0	-	-	V
Input Leakage Current, I_A		Full	-	-	1	-	-	1	µA
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_{IN}		Full	-15	-	+15	-15	-	+15	V
ON Resistance, r_{ON}	Note 2	25	-	250	400	-	250	400	Ω
		Full	-	-	500	-	-	500	Ω
OFF Input Leakage Current, $I_{S(OFF)}$		Full	-	-	50	-	-	50	nA
ON Channel Leakage Current, $I_{D(ON)}$									
HI-1818A		Full	-	-	250	-	-	250	nA
HI-1828A		Full	-	-	125	-	-	125	nA
OFF Output Leakage Current, $I_{D(OFF)}$									
HI-1818A		Full	-	-	250	-	-	250	nA
HI-1828A		Full	-	-	125	-	-	125	nA

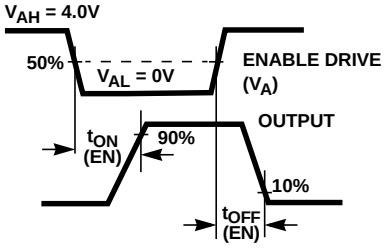
Electrical Specifications Supplies = +15V, -15V, +5V; V_{AL} = 0.4V, V_{AH} = 4.0V, Unless Otherwise Specified **(Continued)**

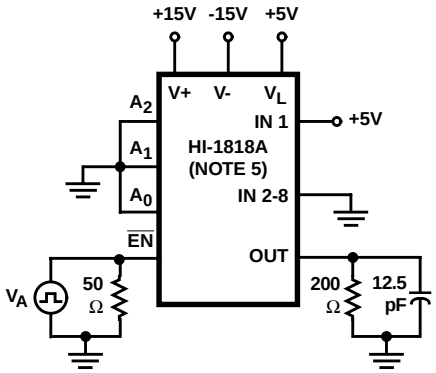
PARAMETER	TEST CONDITIONS	TEMP (^oC)	-2			-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS									
Power Dissipation, P_D		Full	-	-	27.5	-	-	27.5	mW
Current, I+		Full	-	-	0.5	-	-	0.5	mA
Current, I-		Full	-	-	1	-	-	1	mA
Current, I_L		Full	-	-	1	-	-	1	mA

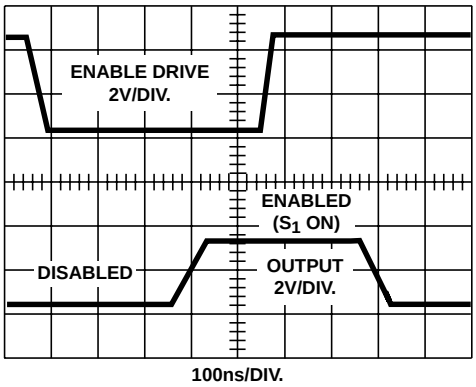
NOTES:

2. V_{OUT} = ±10V, I_{OUT} = ∓1mA.
3. To drive from DTL/TTL circuits, 1kΩ pull-up resistors to 5.0V supply are recommended.
4. Time measured to 90% of final output level; V_{OUT} = -5.0V to 5.0V, Digital Inputs = 0V to 4.0V.

Test Circuits and Waveforms





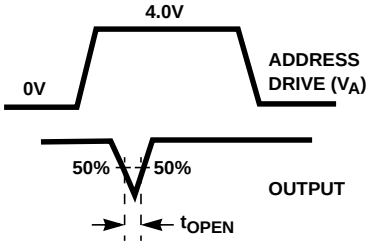


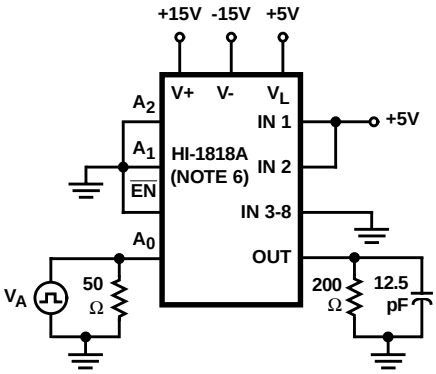
NOTE:

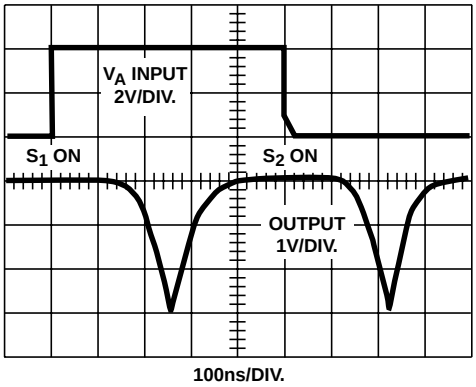
5. Similar connections for HI-1828A.

FIGURE 1A. MEASUREMENT POINTS **FIGURE 1B. TEST CIRCUIT** **FIGURE 1C. WAVEFORMS**

FIGURE 1. ENABLE DELAYS







NOTE:

6. Similar connections for HI-1828A.

FIGURE 2A. MEASUREMENT POINTS **FIGURE 2B. TEST CIRCUIT** **FIGURE 2C. WAVEFORMS**

FIGURE 2. BREAK-BEFORE-MAKE DELAY

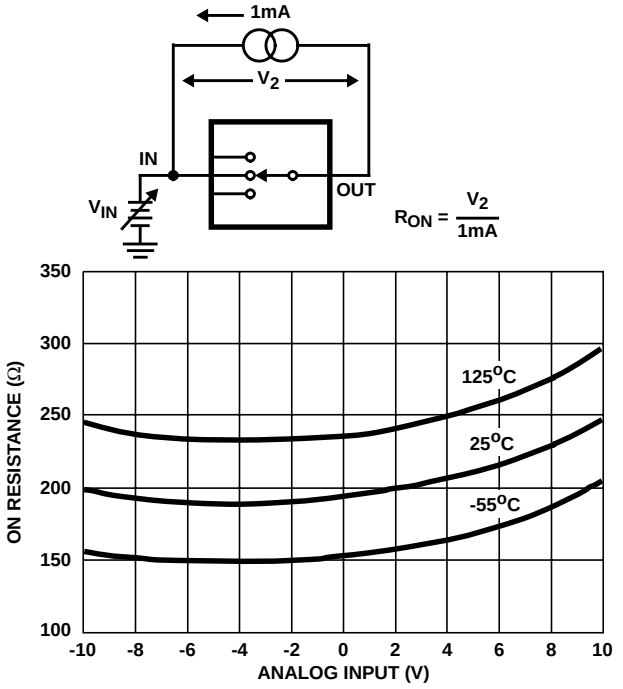


FIGURE 3. ON RESISTANCE vs ANALOG INPUT VOLTAGE

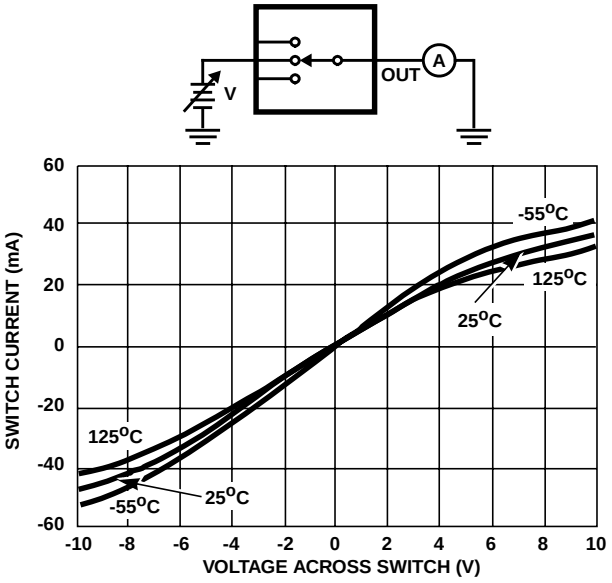
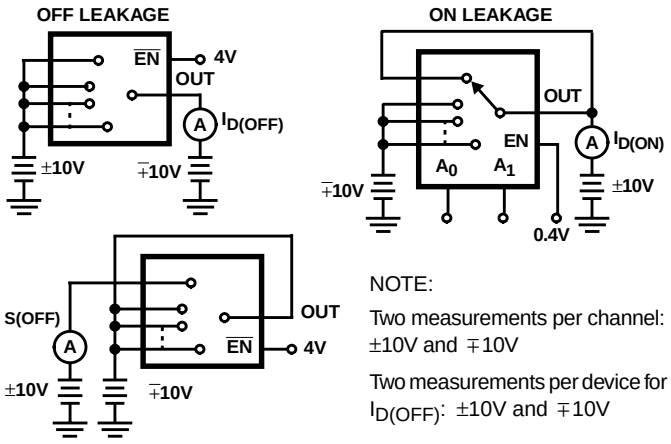


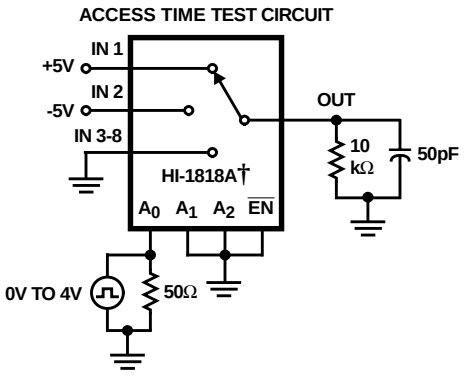
FIGURE 4. ON CHANNEL CURRENT vs VOLTAGE



NOTE:

Two measurements per channel: ±10V and ∓10V

Two measurements per device for $I_{D(OFF)}$: ±10V and ∓10V



† Similar connection for HI-1828A.

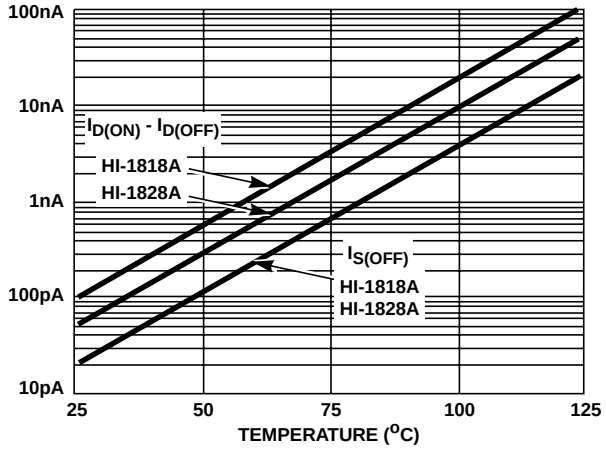


FIGURE 5. LEAKAGE CURRENTS vs TEMPERATURE

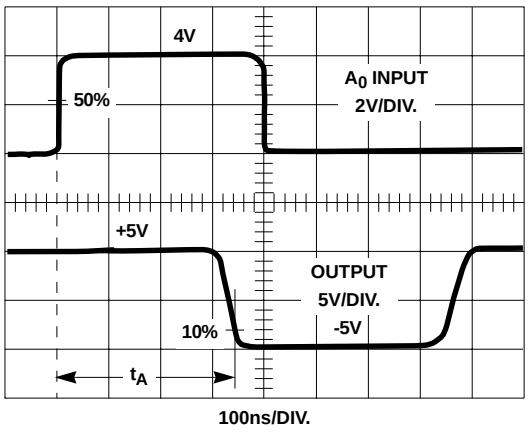


FIGURE 6. ACCESS TIME

Die Characteristics

DIE DIMENSIONS:

67.7 mils x 103.5 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

PASSIVATION:

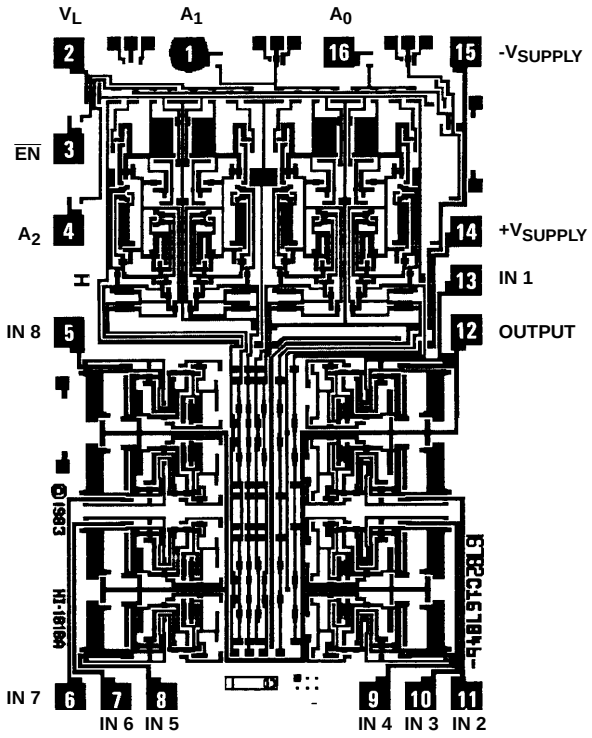
Type: Nitride/Silox
Thickness: Silox: 12kÅ ±2kÅ, Nitride: 3.5kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

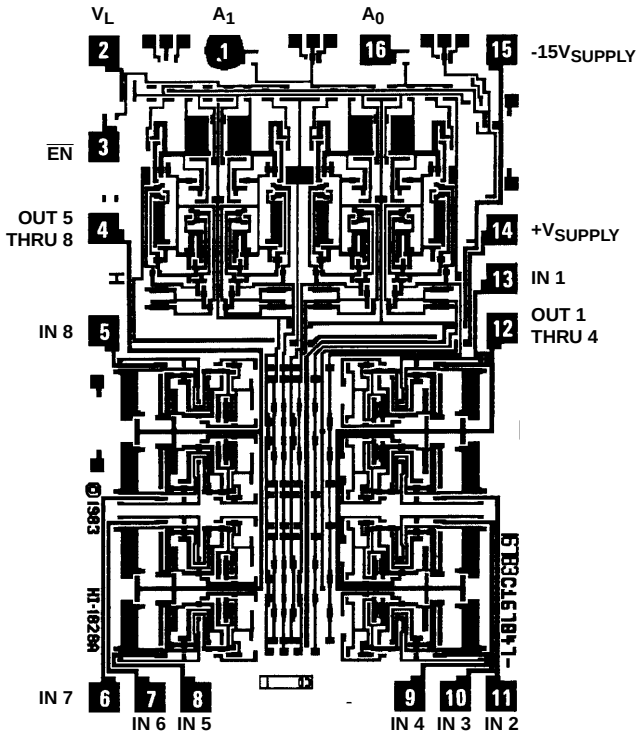
1.43×10^5 A/cm^2 at 25mA

Metallization Mask Layout

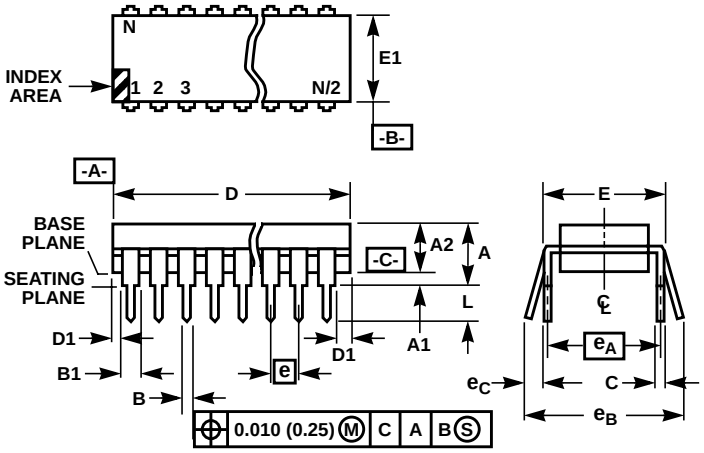
HI-1818A



HI-1828A



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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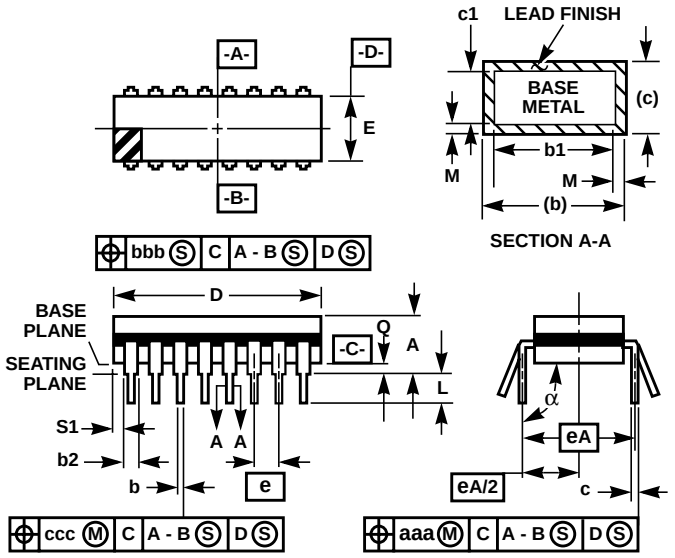
Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil Ltd.
8F-2, 96, Sec. 1, Chien-kuo North,
Taipei, Taiwan 104
Republic of China
TEL: 886-2-2515-8508
FAX: 886-2-2515-8369