

<b>SANYO</b>	No. 4881A	<b>LC75382E</b>
<b>Electronic Tone Controls for Car Stereo Systems</b>		



### Overview

The LC75382E is an electronic tone control IC that can implement, with minimal external components, the complete range of tone and volume controls required in a car stereo, including volume, balance, fader, bass and treble, input switching and input level controls.

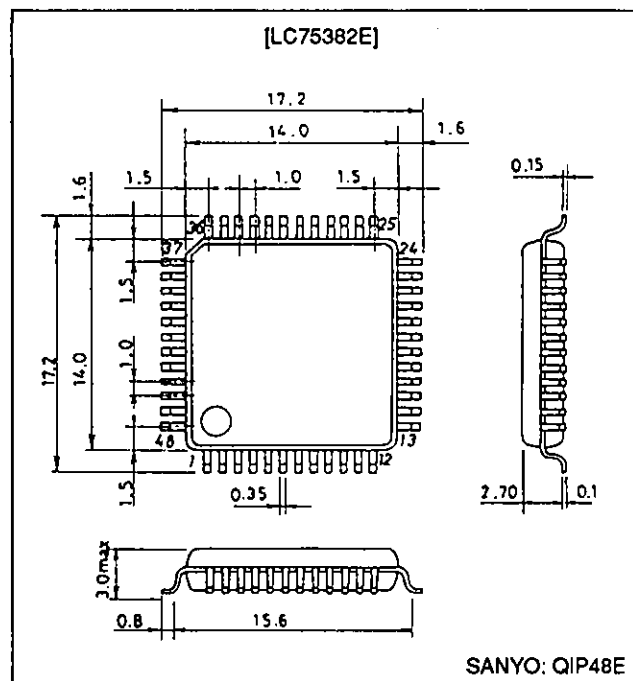
### Features

- **Volume:** Controls the left and right volume levels independently from 0 dB to -78 dB (in 2 dB steps) and -∞ dB (41 settings). Since the left and right levels are independent this circuit also functions as a balance control.
- **Fader:** Attenuates either the rear or front outputs over 16 levels, from 0 dB to -20 dB in 2 dB steps, from -20 dB to -25 dB in 5 dB step, from -25 dB to -45 dB in 10 dB steps and then to -60 dB and -∞ dB.
- **Bass/treble:** Implements 21 position bass and treble controls with the addition of external capacitors.
- **Input selector:** Selects one of four inputs for both the left and right channels. The selected input signal can be amplified by between 0 dB and +18 dB in 6 dB steps.
- The provision of on-chip operational amplifiers means that few external components are required.
- Fabricated in a silicon gate process for minimal switching noise.
- All functions can be controlled by serial data over a CCB interface.

### Package Dimensions

unit: mm

**3156-QFP48E**



• CCB is a trademark of SANYO ELECTRIC CO., LTD.  
 • CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

### Specifications

**Absolute Maximum Ratings at Ta = 25°C, V<sub>SS</sub> = 0 V**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD</sub> max	V <sub>DD</sub>	12	V
Maximum input voltage	V <sub>IN</sub> max	CL, DI, CE, LTIN, RTIN, L10dBIN, R10dBIN, L2dBIN, R2dBIN, LFIN, RFIN, L1 to L4, R1 to R4	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 85°C	310	mW
Operating temperature	T <sub>opr</sub>		-40 to +85	°C
Storage temperature	T <sub>stg</sub>		-50 to +125	°C

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Allowable Operating Ranges at Ta = 25°C, VSS = 0 V

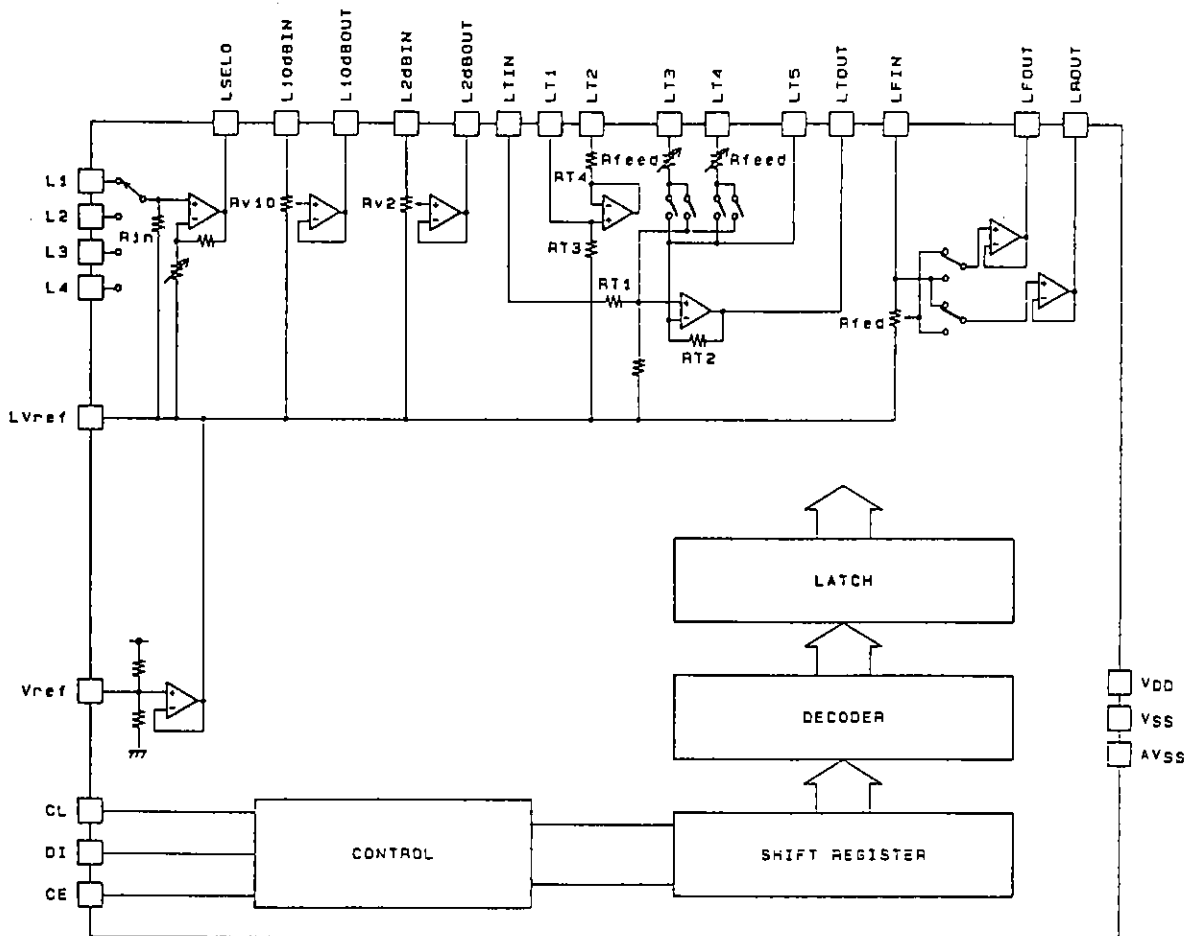
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V <sub>DD</sub>	V <sub>DD</sub>	6.0		11.0	V
Input high level voltage	V <sub>IH</sub>	CL, DI, CE	4.0		V <sub>DD</sub>	V
Input low level voltage	V <sub>IL</sub>	CL, DI, CE	V <sub>SS</sub>		1.0	V
Input voltage amplitude	V <sub>IN</sub>	LTIN, RTIN, L10dBIN, R10dBIN, L2dBIN, R2dBIN, LFIN, RFIN, L1 to L4, R1 to R4	V <sub>SS</sub>		V <sub>DD</sub>	Vp-p
Input pulse width	t <sub>pw</sub>	CL	1			μs
Setup time	t <sub>setup</sub>	CL, DI, CE	1			μs
Hold time	t <sub>hold</sub>	CL, DI, CE	1			μs
Operating frequency	f <sub>opg</sub>	CL			500	kHz

Electrical Characteristics at Ta = 25°C, V<sub>DD</sub> = 9 V, V<sub>SS</sub> = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
[Input Block]						
Input resistance	R <sub>in</sub>	L1 to L4, R1 to R4		1		MΩ
Clipping level	V <sub>cl</sub>	LSELO, RSELO: THD = 1.0%		2.35		V <sub>rms</sub>
Output load resistance	R <sub>L</sub>	LSELO, RSELO	10			kΩ
Minimum input gain	G <sub>in min</sub>		-2	0	+2	dB
Maximum input gain	G <sub>in max</sub>		+16.0	+18.0	+20.0	dB
Step resolution	G <sub>step</sub>			+6.0		dB
[Volume Block]						
Input resistance	R <sub>v10</sub>	L10dBIN, R10dBIN: 10 dB steps	21	35	49	kΩ
	R <sub>v2</sub>	L2dBIN, R2dBIN: 2 dB steps	6	10	14	kΩ
Step resolution	AT <sub>step</sub>			2		dB
Step error	AT <sub>err</sub>	step = 0 to -40 dB	-2	0	+2	dB
[Fader Volume Block]						
Input resistance	R <sub>fed</sub>	LFIN, RFIN	12	20	28	kΩ
Step resolution	AT <sub>step</sub>	step = 0 to -20 dB		2		dB
		step = -20 to -25 dB		5		dB
		step = -25 to -45 dB		10		dB
Step error	AT <sub>err</sub>	step = 0 to -40 dB, step = -40 to -60 dB	-2	0	+2	dB
Output load resistance	R <sub>L</sub>	LFOUT, LROUT, RFOUT, RROUT	10			kΩ
[Bass/Treble Control Block]						
Control range	G <sub>bass</sub> , G <sub>tre</sub>	Max. Boost/Cut	±15	±17	±19	dB
Step resolution	B <sub>step</sub>		0.7	1.7	2.7	dB
Internal feedback resistance	R <sub>feed</sub>		46	76	107	kΩ
[Overall Characteristics]						
Total harmonic distortion	THD (1)	V <sub>IN</sub> = 300 mV <sub>rms</sub> , f = 1 kHz, all controls flat overall		0.005	0.01	%
	THD (2)	V <sub>IN</sub> = 300 mV <sub>rms</sub> , f = 20 kHz, all controls flat overall		0.008	0.02	%
Crosstalk	CT	V <sub>IN</sub> = 1 V <sub>rms</sub> , f = 1 kHz, all controls flat overall, R <sub>g</sub> = 1 kΩ	60	84.5		dB
Output at maximum attenuation	V <sub>O min</sub>	V <sub>IN</sub> = 1 V <sub>rms</sub> , f = 1 kHz, Main volume at -∞	-65	-74.5		dB
Output noise voltage	V <sub>N</sub> (1)	All controls flat overall (IHF-A), R <sub>g</sub> = 1 kΩ		5.2	12	μV
	V <sub>N</sub> (2)	All controls flat overall (DIN-AUDIO), R <sub>g</sub> = 1 kΩ		7.2	16	μV
	V <sub>N</sub> (3)	All controls flat overall (NO-FILTER), R <sub>g</sub> = 1 kΩ		9.2	20	μV
	V <sub>N</sub> (4)	G <sub>v</sub> = +18dB (IHF-A), R <sub>g</sub> = 1 kΩ		23	50	μV
	V <sub>N</sub> (5)	Bass at maximum boost, treble at maximum boost (IHF-A), R <sub>g</sub> = 1 kΩ		48	120	μV
Current drain	I <sub>DD</sub>	V <sub>DD</sub> - V <sub>SS</sub> = 11 V		28	33	mA
Input high level current	I <sub>IH</sub>	CL, DI, CE: V <sub>IN</sub> = 9 V			10	μA
Input low level current	I <sub>IL</sub>	CL, DI, CE: V <sub>IN</sub> = 0 V	-10			μA

# LC75382E

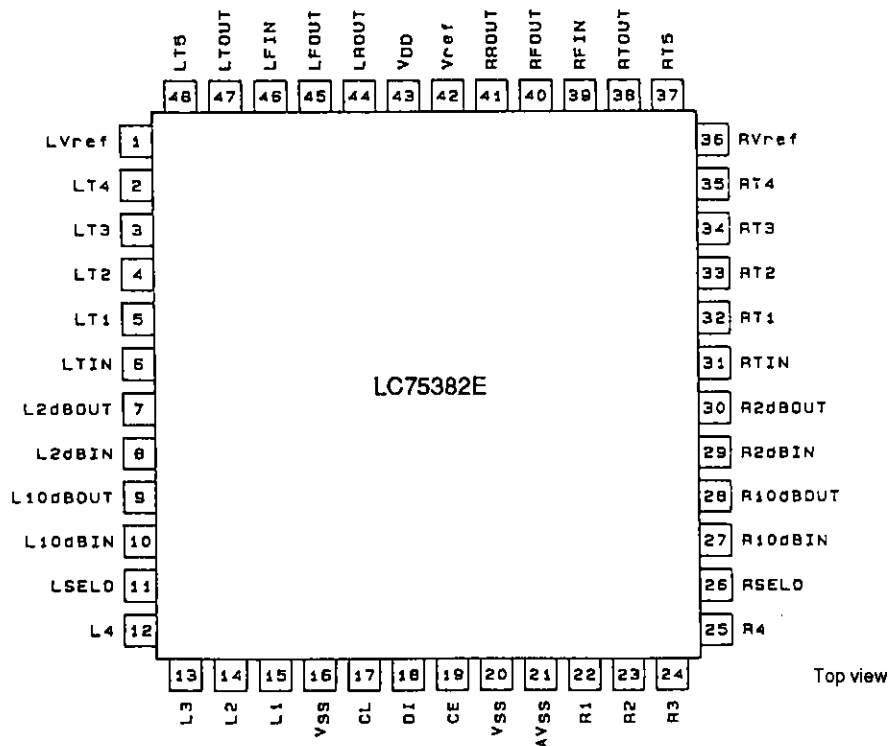
## Equivalent Circuit Block Diagram



Note: The right channel is identical.

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## Pin Assignment



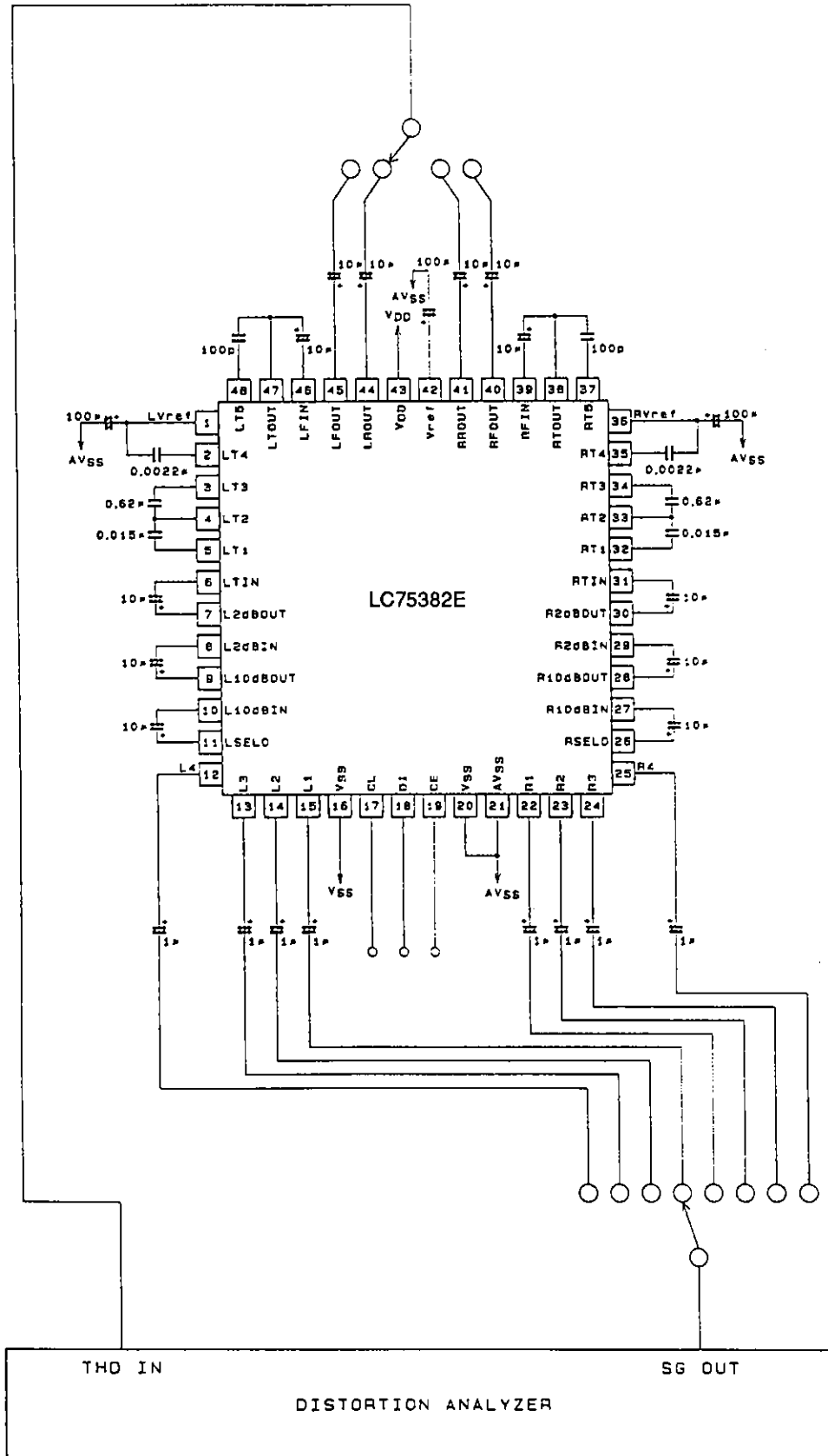
Top view

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# LC75382E

## Electrical Characteristics Test Circuit

### 1. Total harmonic distortion

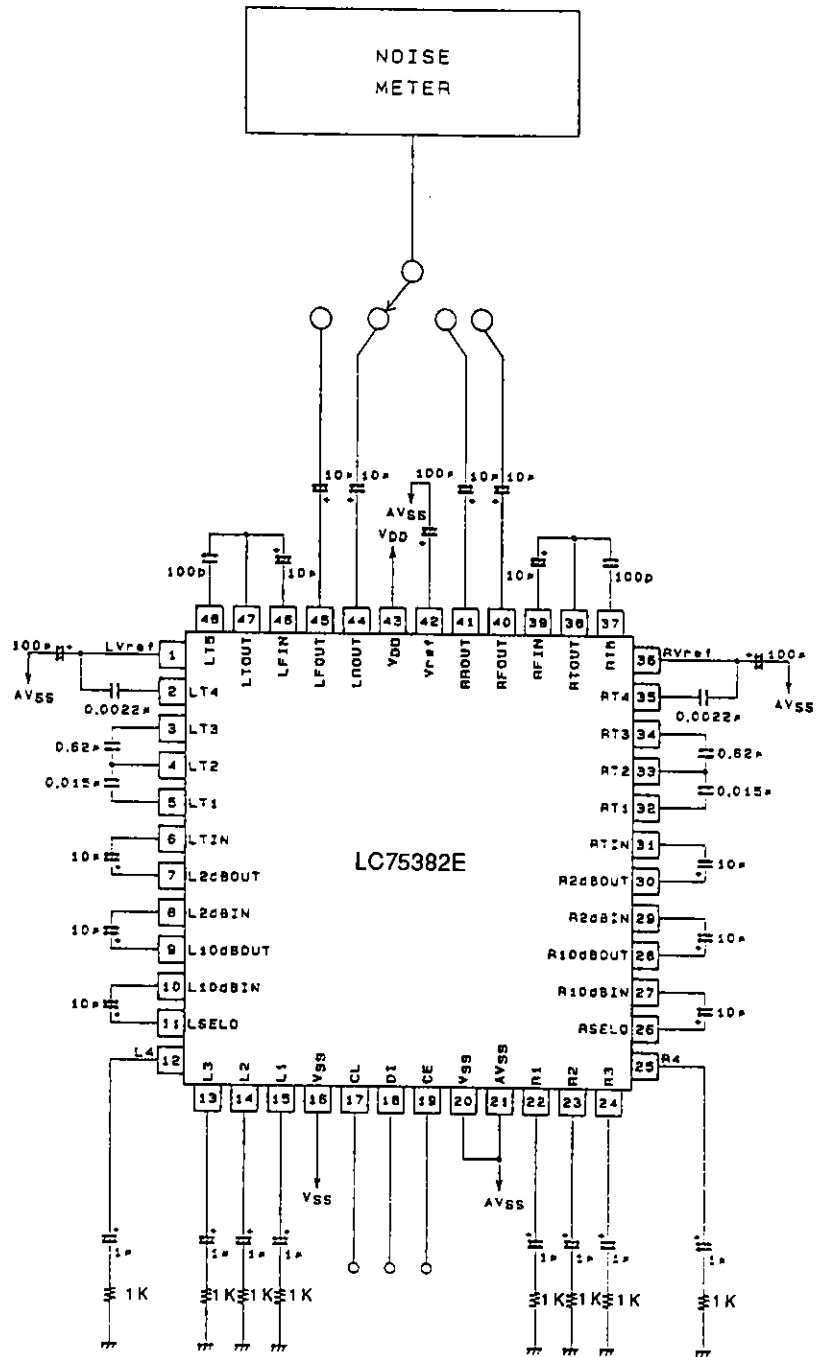


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Unit (capacitance: F)

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## 2. Output noise voltage

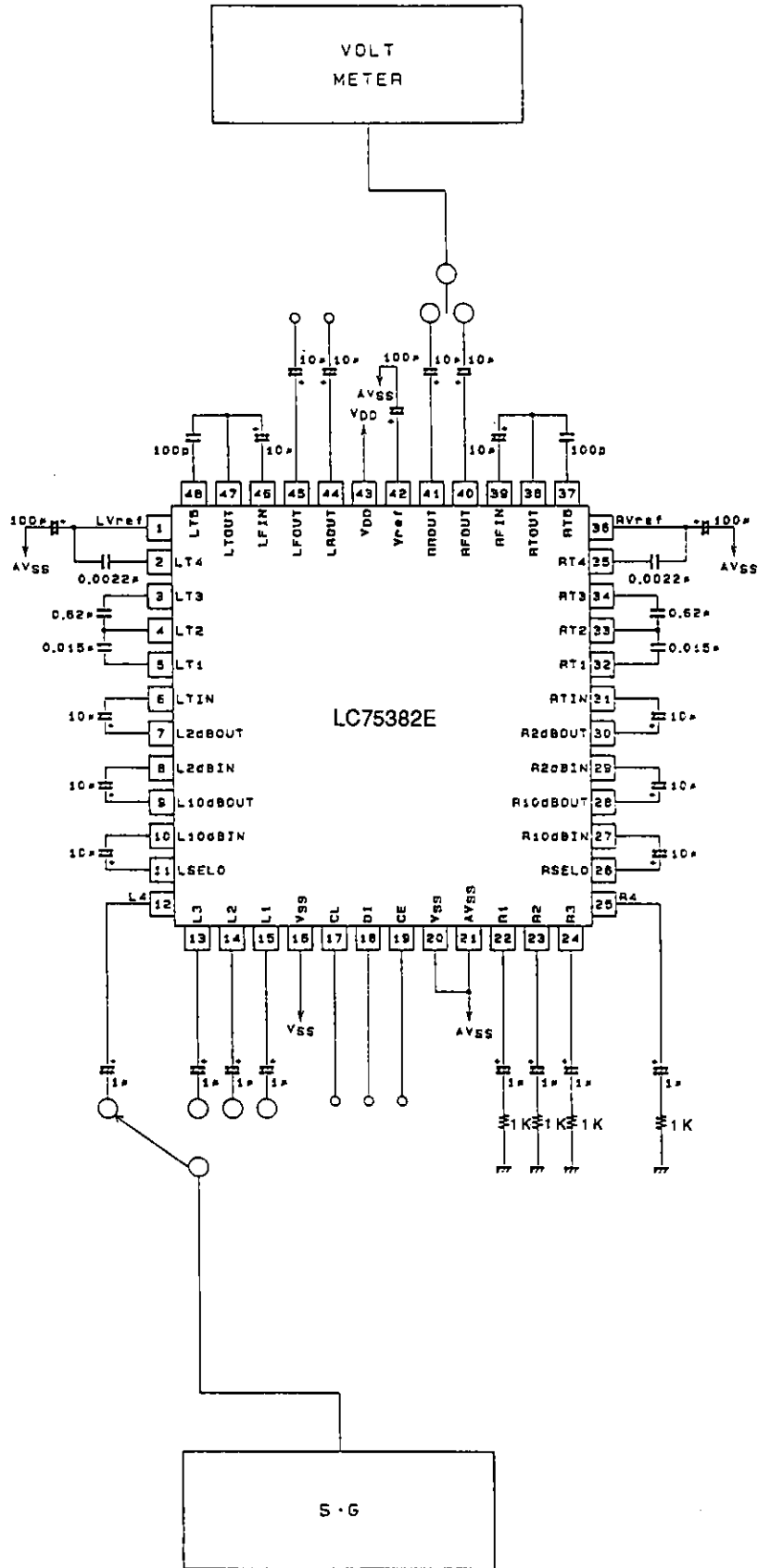


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Unit (resistance: Ω, capacitance: F)

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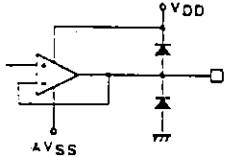
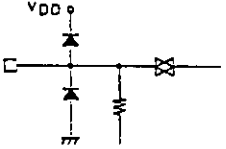
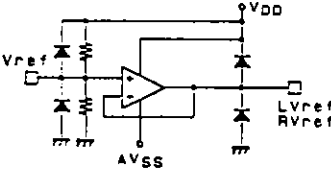
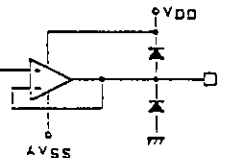
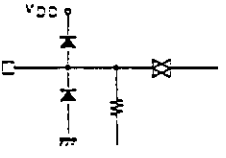
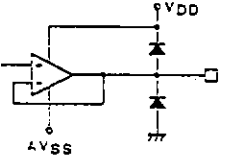
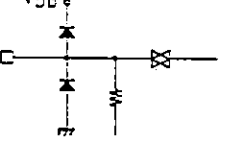
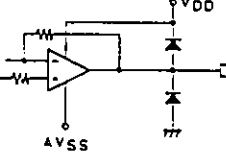
## 3. Crosstalk



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Unit (resistance: Ω, capacitance: F)

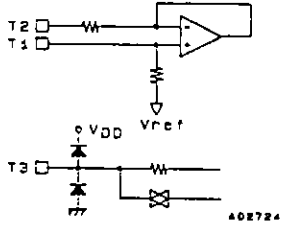
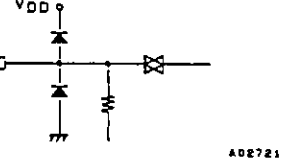
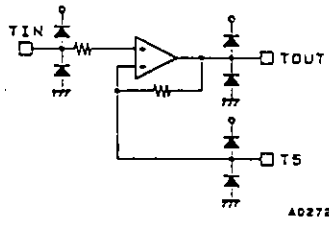
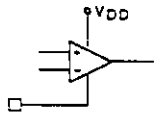
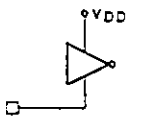
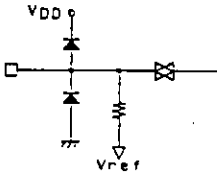
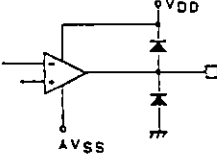
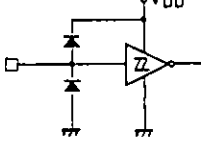
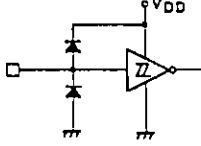
Pin Functions

Pin No.	Symbol	Function	Note
44 45 41 40	LROUT LFOUT RROUT RFOUT	Fader block output. Attenuates only the front or rear outputs. The left/right attenuation is identical. These are op amp outputs and thus are low impedance.	 A02720
46 39	LFIN RFIN	Fader block input Must be driven by low impedance outputs.	 A02721
1 36	LVref RVref	Common pins for the main volume, fader, tone and gain control blocks.	 A02722
42	Vref	V <sub>DD</sub> /2 voltage generation block. Connect a capacitor (about 100 μF) between Vref and AV <sub>SS</sub> to suppress power supply ripple.	
7 30	L2dBOUT R2dBOUT	Main volume 2 dB step attenuator outputs	 A02720
8 29	L2dBIN R2dBIN	Main volume 2 dB step attenuator inputs Must be driven by low impedance outputs	 A02721
9 28	L10dBOUT R10dBOUT	Main volume 10 dB step attenuator outputs	 A02720
10 27	L10dBIN R10dBIN	Main volume 10 dB step attenuator inputs Must be driven by low impedance outputs.	 A02721
47 38	LTOUT RTOUT	Tone control outputs	 A02723

Continued on next page.

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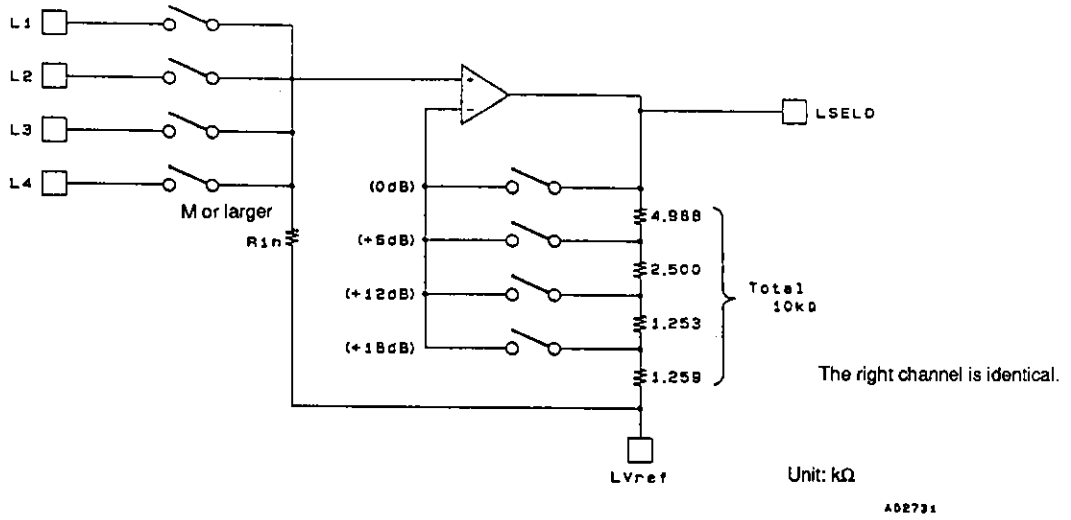
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Pin No.	Symbol	Function	Note
5 4 3 32 33 34	LT1 LT2 LT3 RT1 RT2 RT3	Tone circuit low band filter capacitor connections. Connect capacitors between the T1 and T2 pairs and between the T2 and T3 pairs.	 A02724
2 35	LT4 RT4	Tone circuit high band filter capacitor connections. Connect high band compensating capacitors between the T4 pins and Vref.	 A02721
48 37	LT5 RT5	Tone circuit filter op amp inverting inputs Out of band signals can be excluded by connecting capacitors with appropriate values between the T5 and TOUT pairs.	 A02725
6 31	LTIN RTIN	Tone control circuit inputs Must be driven by low impedance outputs.	
43	VDD	Power supply	
21	A. VSS	Internal op amp ground	 A02726
16, 20	VSS	Internal logic system ground	 A02727
15 14 13 12 22 23 24 25	L1 L2 L3 L4 R1 R2 R3 R4	Audio signal inputs	 A02728
11 26	LSELO RSELO	Input selector outputs	 A02729
19	CE	Chip enable. Data is written to the internal latch on the high to low transition of this signal. The analog switches operate at that point. Data transfer is enabled when this signal is high.	 A02730
18 17	DI CL	Serial data and clock connections for IC control.	 A02730

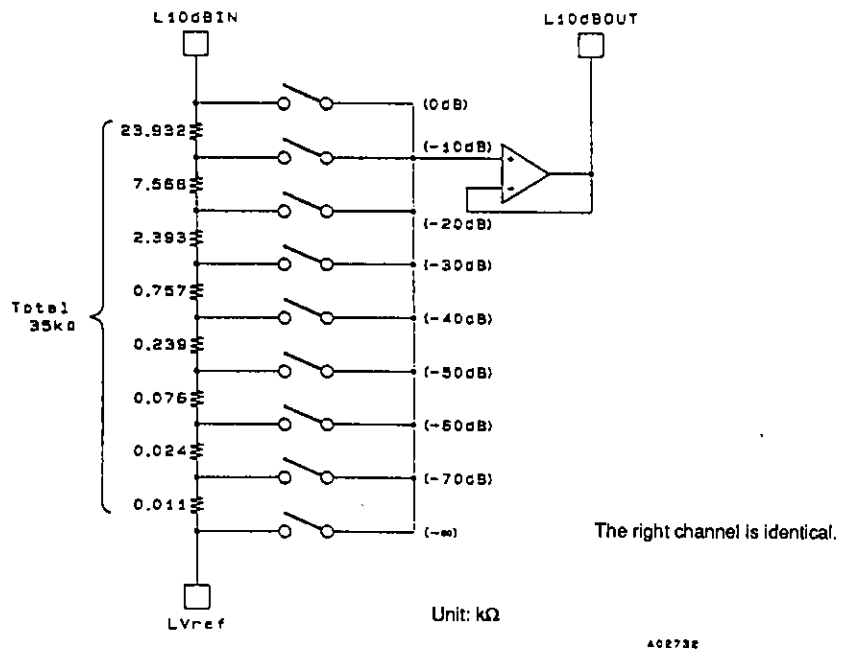


Internal Equivalent Circuit Details

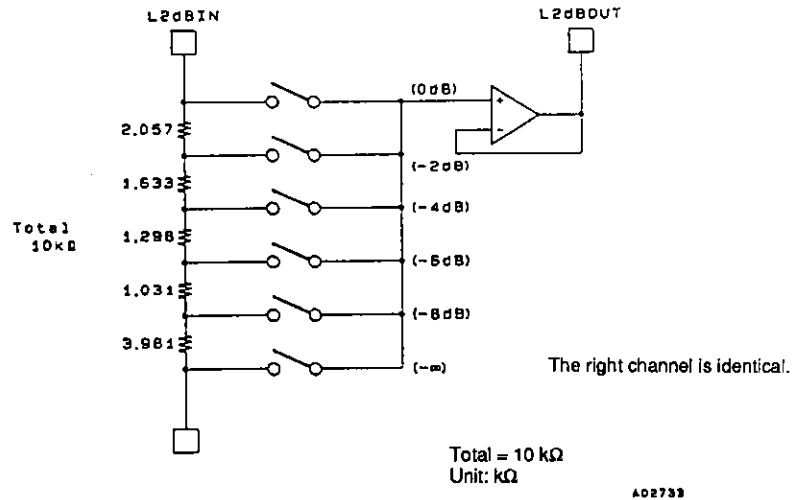
Input Block Equivalent Circuit



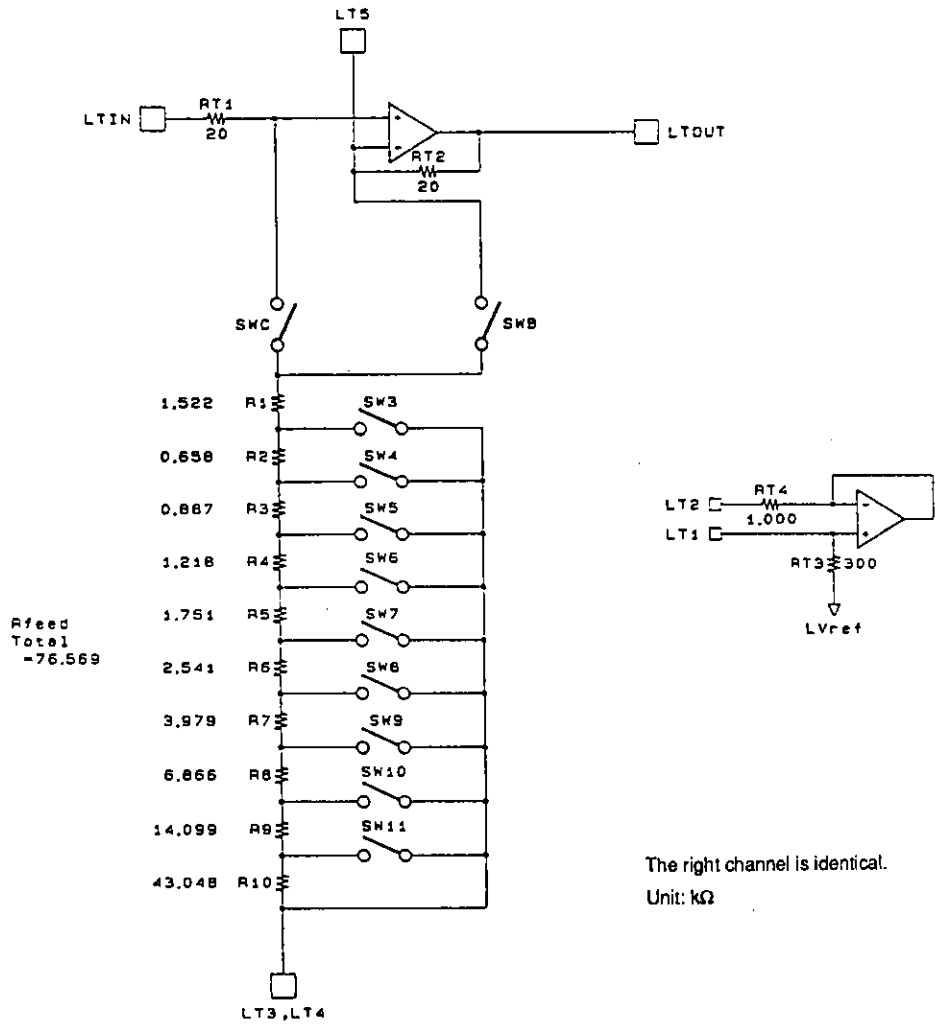
10 dB Step Volume Equivalent Circuit



2 dB Step Equivalent Circuit



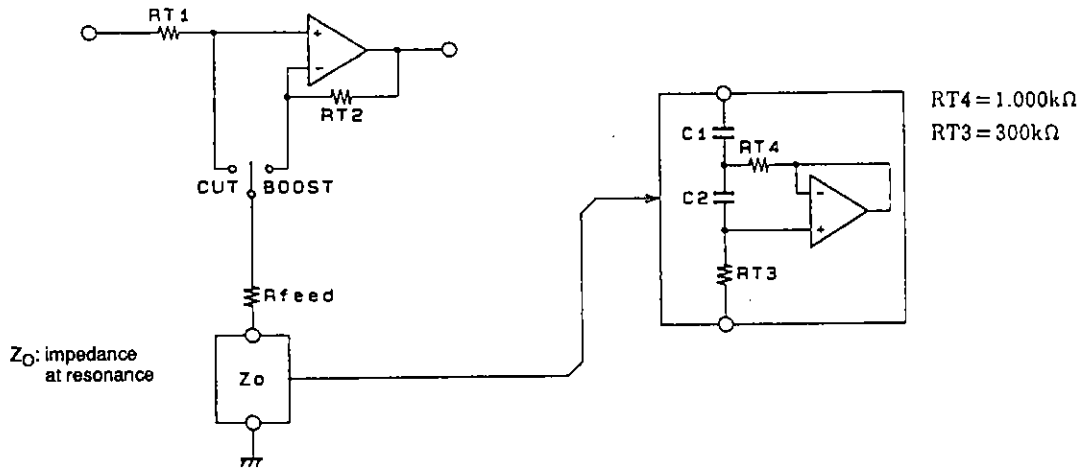
Tone Block Equivalent Circuit



**Tone Control Circuit External Capacitor Value Calculation Example**

The external capacitors used with the LC75382E are structural components of semiconductor inductors (simulated inductors). This section presents the equivalent circuits and formulas for acquiring the desired center frequencies.

**1. Semiconductor inductor equivalent circuit**



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**2. Sample calculation**

Specifications: 1. Center frequency  $F_O = 100$  Hz

2. Q at maximum boost:  $Q_{max} = 1.05$

① Derive the sharpness of the semiconductor inductor itself,  $Q_O$ .

$$Q_O = \frac{(RT4 + Rfeed)}{RT4} \times Q_{max} = 2.6481$$

② Derive C1.

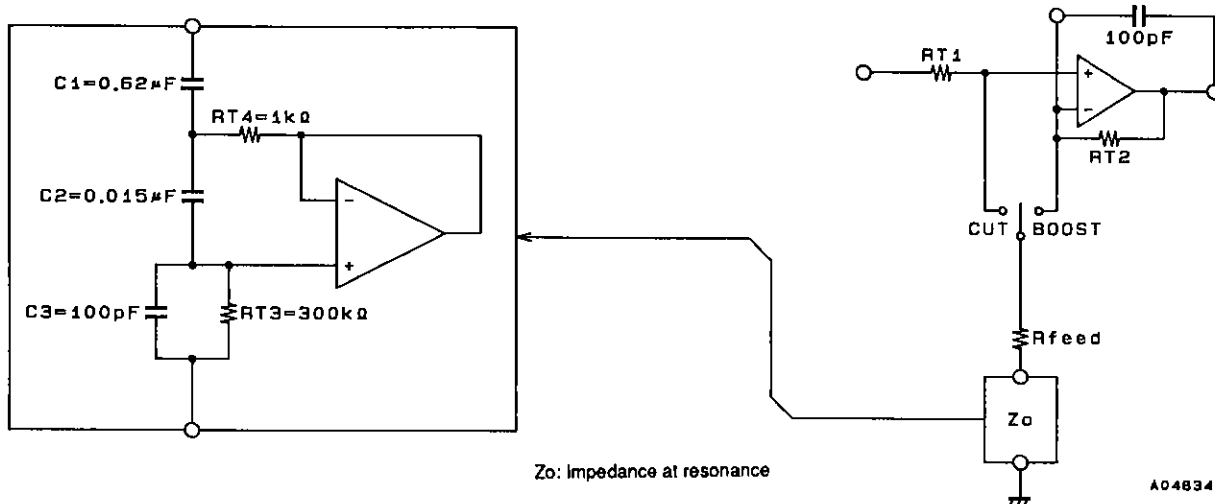
$$C1 = 1/2\pi F_O RT4 Q_O \approx 0.60 (\mu F)$$

② Derive C2.

$$C2 = Q_O / 2\pi F_O RT3 \approx 0.014 (\mu F)$$

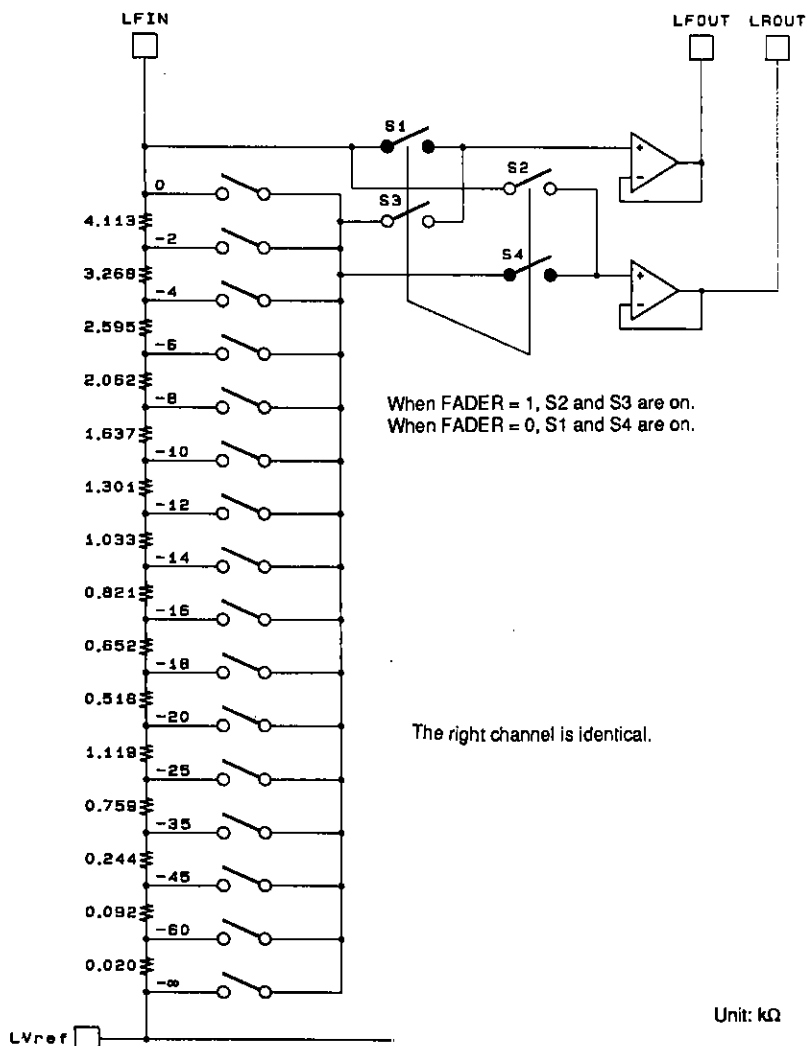
Note: See the tone block equivalent circuit diagram (page 10) for the internal resistance.

Technique for Reducing Noise in the Tone Circuit Output



The output noise can be improved by about 6 dB by providing an external impedance at resonance of Zo and adding the capacitor C3 with a value of about 100 pF. An even larger noise reduction effect can be acquired by using a low noise operational amplifier in the external circuit.

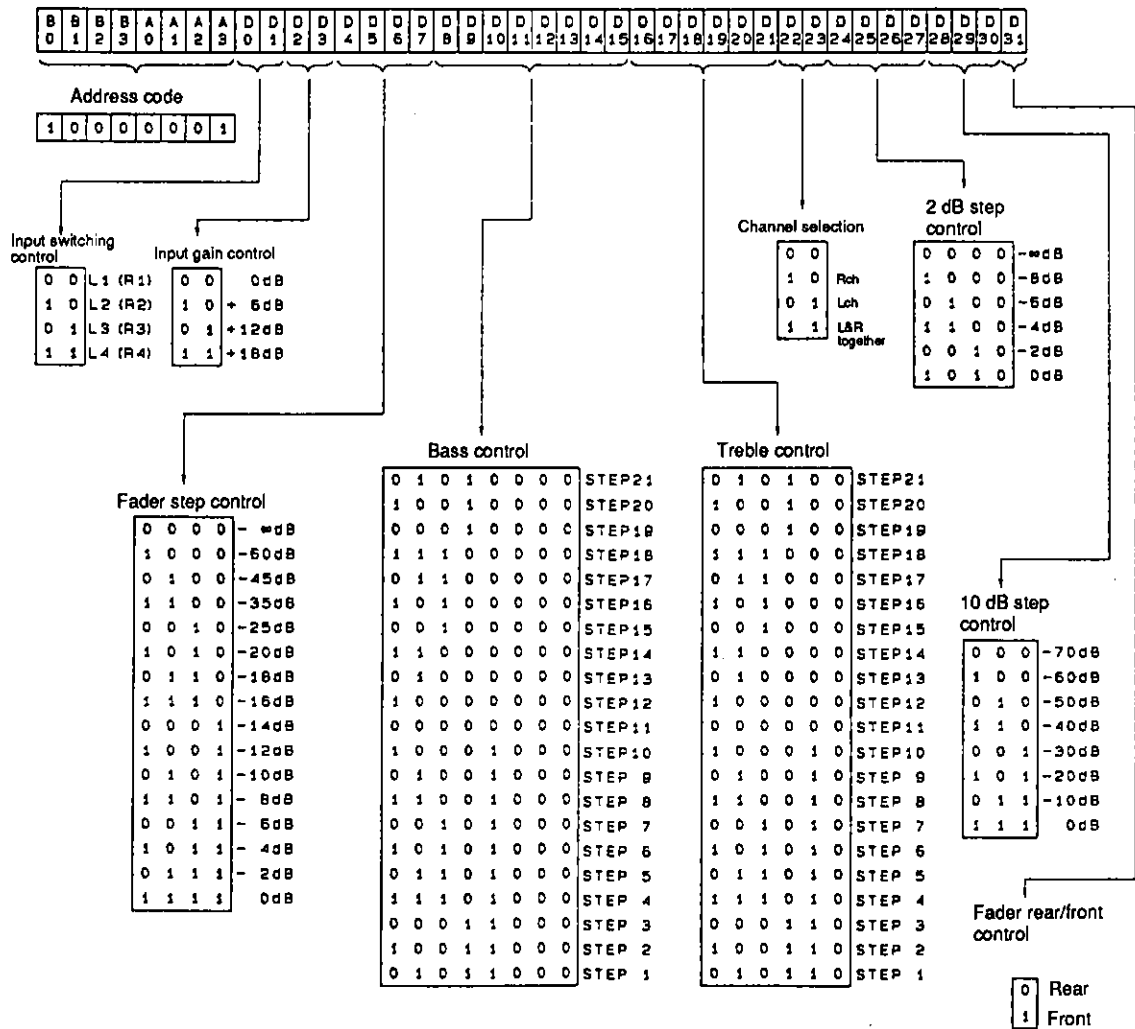
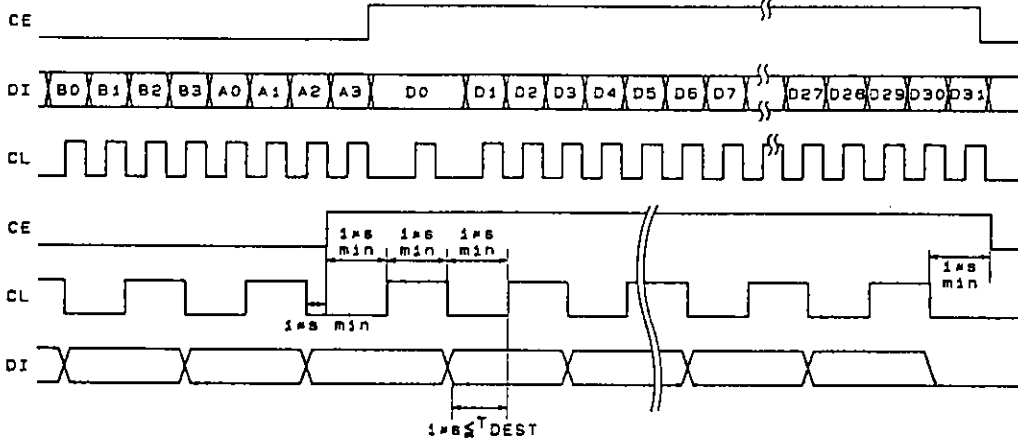
Fader Block Equivalent Circuit



When data specifying a  $-\infty$  attenuation in the 2 dB step main volume is issued, S1 and S2 will open and at the same time, S3 and S4 will turn on.

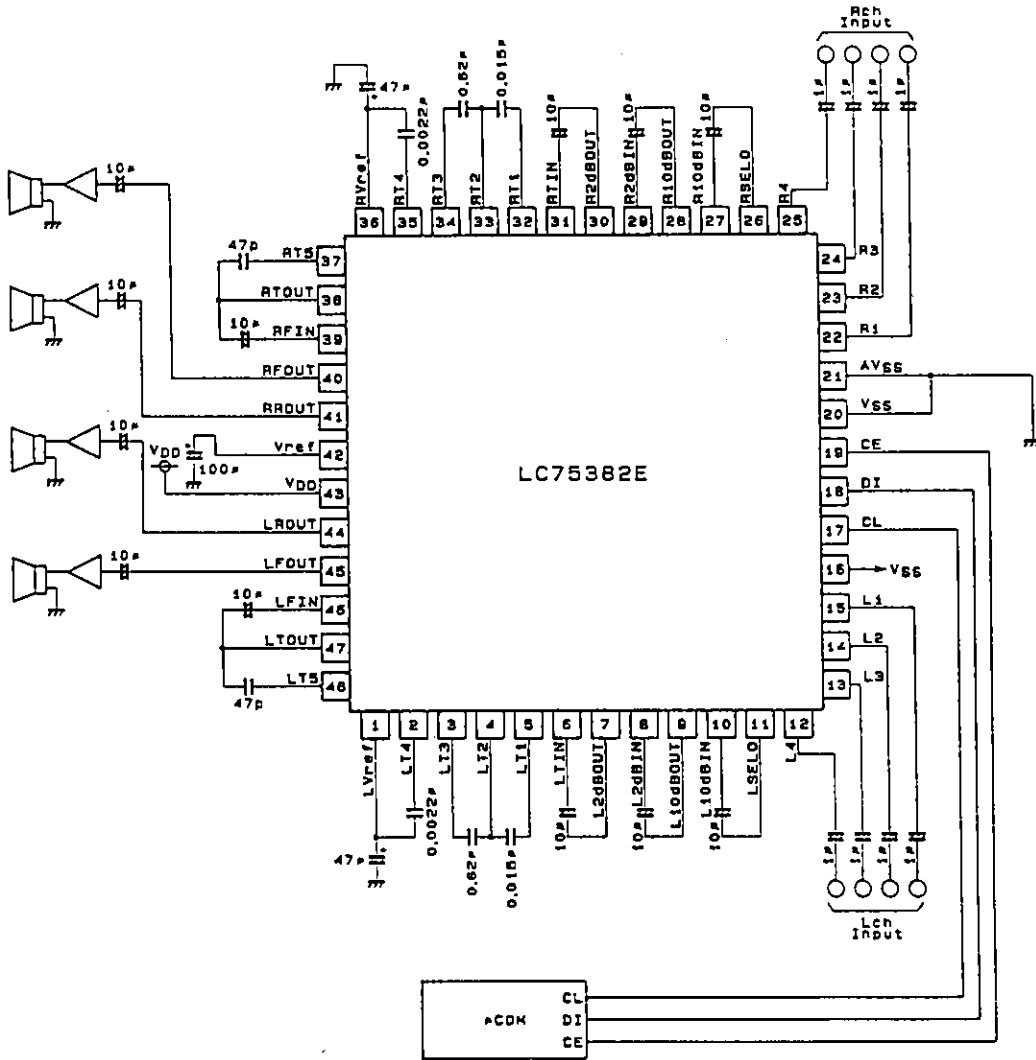
**Control System Timing and Data Format**

The prescribed data (signals) must be applied to the CE, CL and DI pins to control the LC75382. The data consists of a total of 40 bits, of which 8 bits are address and 32 bits are the actual control data.



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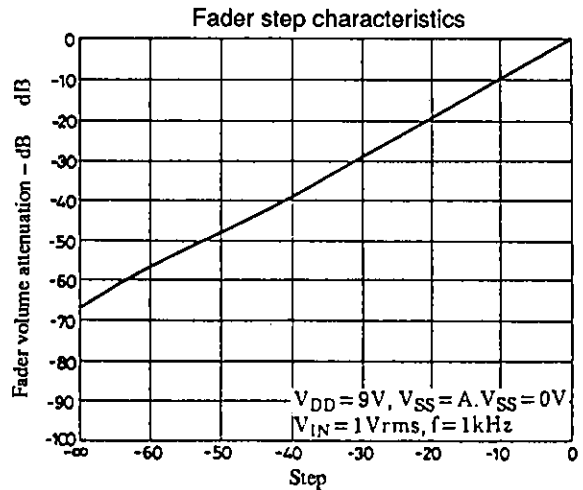
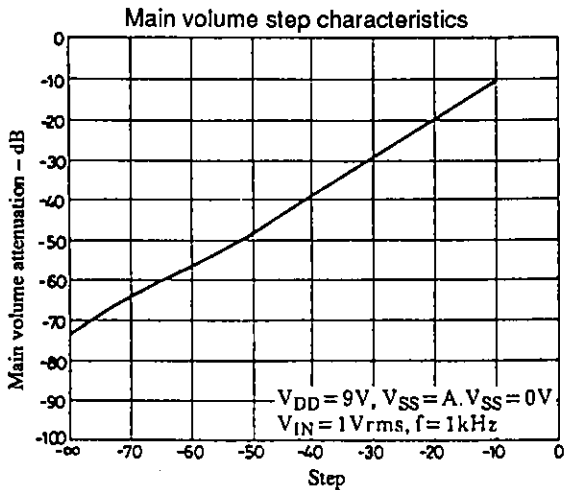
Sample Application Circuit



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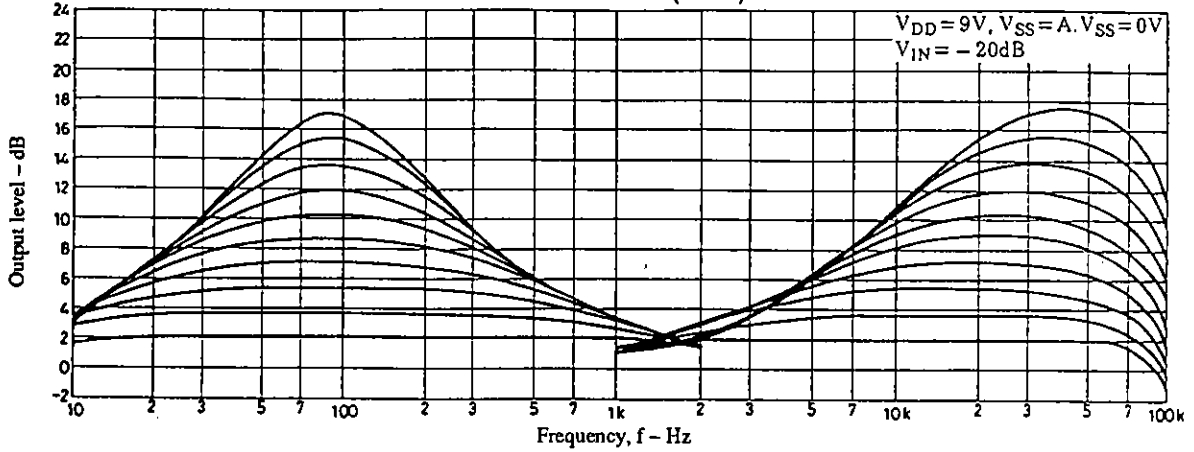
Usage Notes

1. The states of the internal analog switches are undefined when power is first applied. Muting should be applied externally until data has been transferred.
2. To prevent the high frequency digital signals on the CL, DI and CE pin lines from entering the analog signal system, those lines must be guarded by the ground pattern. Alternatively, shielded cable can be used for those lines.

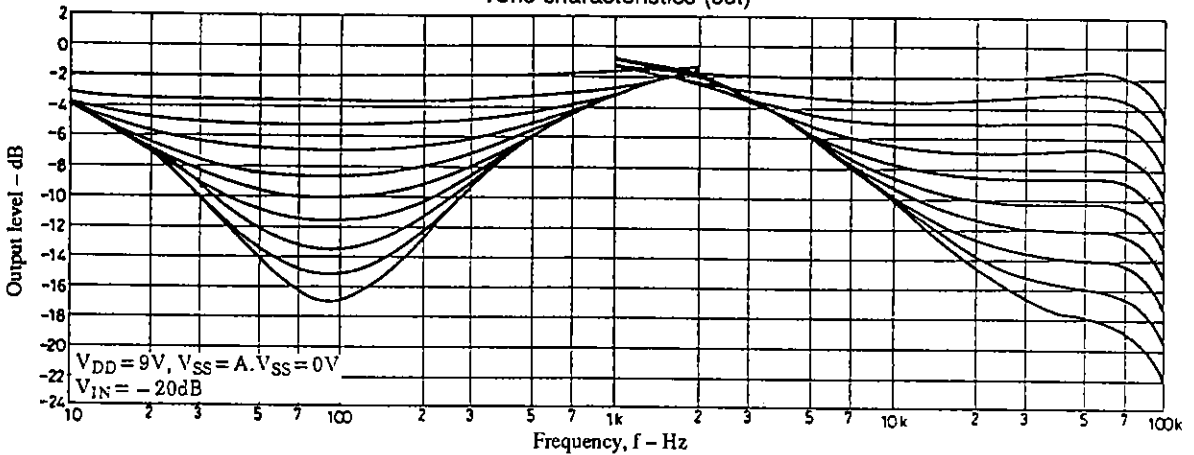


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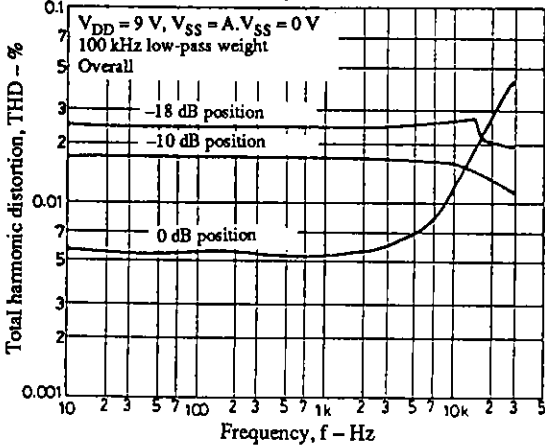
Tone characteristics (boost)



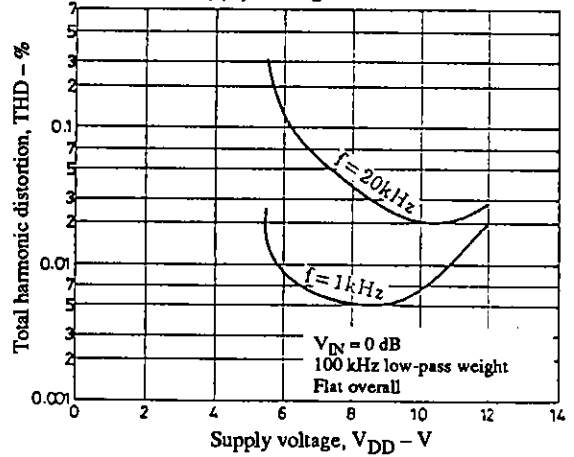
Tone characteristics (cut)



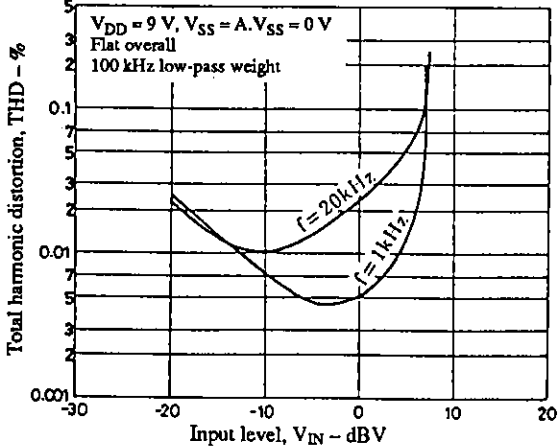
THD - frequency characteristics



THD - supply voltage characteristics



THD - input level characteristics



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