CMOS Nonvolatile Controller Circuit

Features

- Makes volatile memories nonvolatile
- Precision Voltage Monitor disables memory access when supply voltage out of tolerance specification. No incorrect data can be written to the memory.
- Supply voltage selectable with TOL pin (5% or 10%).
- Automatic battery back-up during power failure for nonvolatile data storage in memory.
- Independent dual battery switches for redundancy.
- Battery check at Power-up.
- Memory access disabled for 20 ms after power-up or after power glitches for extra data integrity.
- Low Power CMOS
- Space saving 8-pin DIP or 16-pin SOIC surface mount package.

Operation

The CM1210 nonvolatile controller performs all essential functions for retaining valid data in volatile memory during power failure by a battery backup. With one CM1210 and one or two 3V batteries a bank of SRAM's can be made nonvolatile.

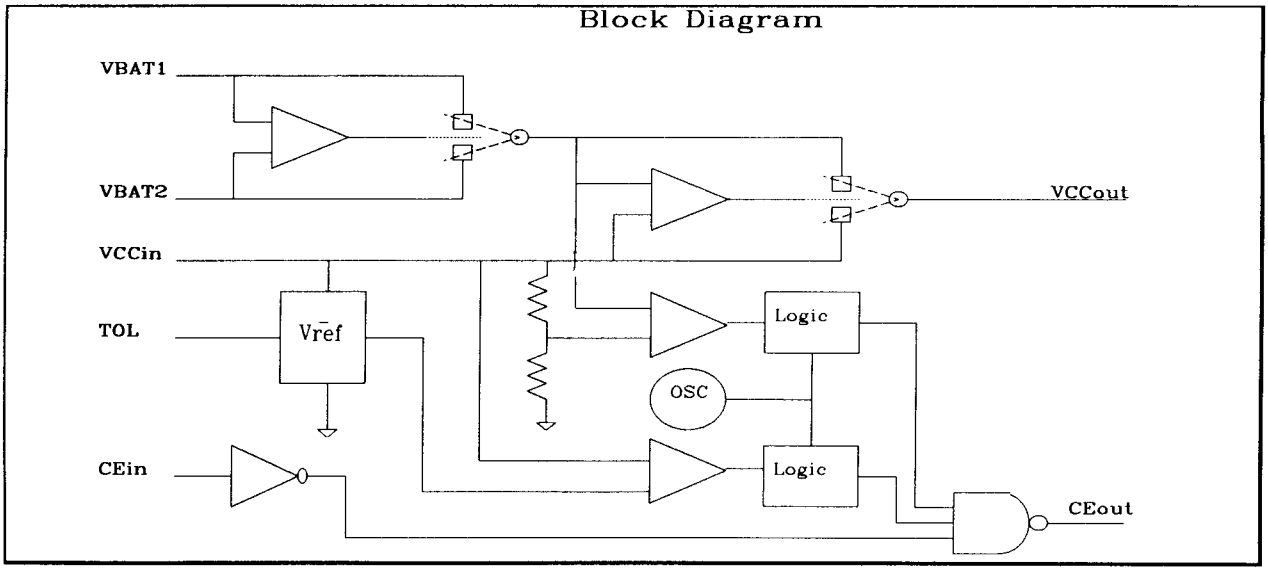
At power-up both batteries are tested under loaded conditions. If only one battery is being used the second battery input needs to be grounded. A battery failure will be only indicated if both battery inputs are below 2.2V. A battery failure is signaled by disabling the 2nd CEO pulse after power-up.

At power-up and for a period of maximum 125 ms thereafter the CEO output is held high, disabling all memory cycles.

During normal operation with VCCI within the programmable tolerance limits, 5% or 10%, the VCCO output is connected to theVCCI input by an internal switch with less than 200 mV voltage drop at 80 mA of output current. CEO will follow CE with a maximum 20 ns delay. Power fail detection occurs in the VCCI range of 4.74V to 4.5V with the tolerance pin grounded (5% tolerance) or in the range of 4.49 V to 4.25 V with the tolerance pin connected to VCCO (10 % tolerance). Power fail must occur during three subsequent 25 ms intervals before it is validated and CEO then will be disabled: If CE is high CEO will stay high at VCCO during a validated power fail condition. If CE is low it will be forced high 75 ms after the validated power fail occurs. A recovery from power fail is equivalent to a power-up.

As long as VCCI is above the higher of the two battery voltages VCCO will be connected to VCCI. As soon as VCCI falls below the higher of the two battery voltages VCCO will be disconnected from VCCI and connected to the higher battery voltage (at a lower current rating of the switch). Once VCCO is connected to a VBAT, this battery voltage must drop .5 V below the other battery voltage before VCCO will be connected to the other battery.

Block Diagram



CMOS Nonvolatile Controller Circuit

Fig. 1 shows a typical application to make CMOS RAMs nonvolatile with all the necessary connections to write protect the RAMs when VCC is less than 4.75 Volts.

Fig. 2 shows the use of the CM1210 to halt the processor when VCC is less than 4.75 Volts and to delay its restart on power-up to prevent erroneous writes.

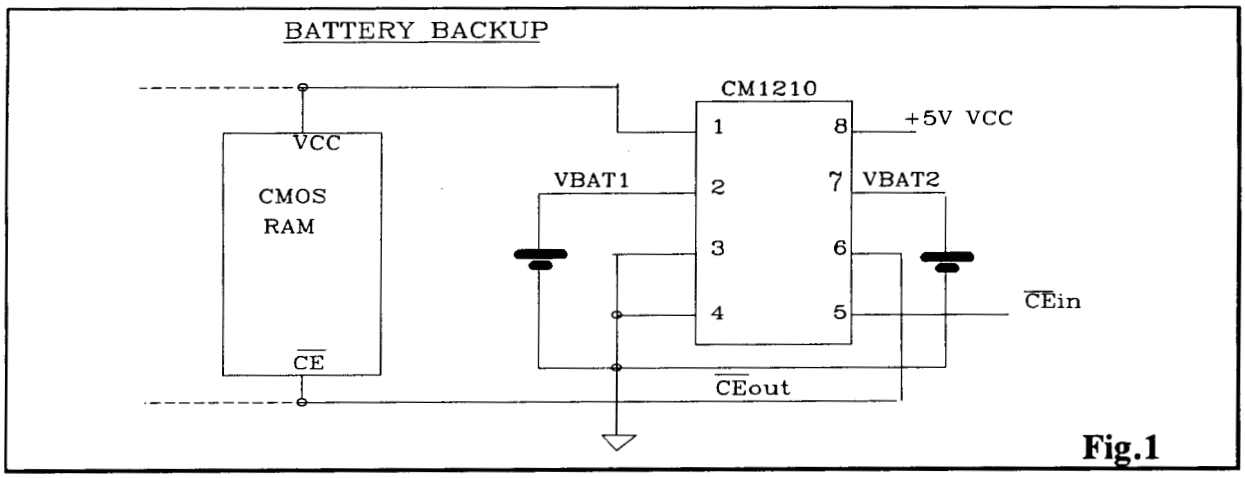


Fig.1

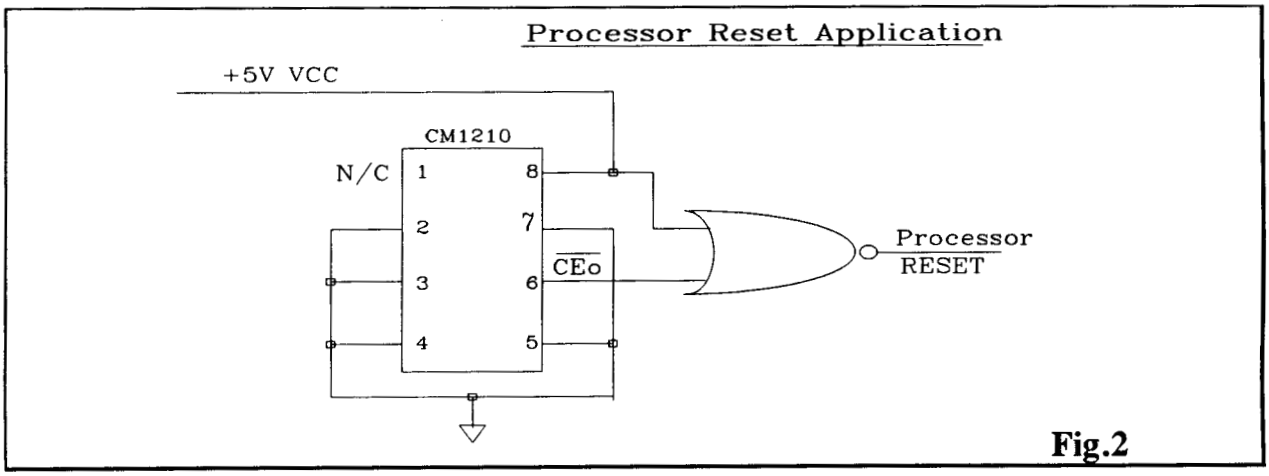


Fig.2

CMOS Nonvolatile Controller Circuit

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to ground.....-0.3V to +7V

Operating temperature.....0°C to 70°C

Storage temperature..... -55°C to 125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C < T_A < 70°C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage PIN3 = GND	VCCI (5%)	4.75	5.0	5.5	V
Supply Voltage PIN3 = VCCO	VCCI (10%)	4.5	5.0	5.5	V
CE input low	VIL	-.3		0.8	V
CE input high	VIH	2.2		VCCO+0.3	V
Battery voltage	VBAT1,2	2.0		4.0	V

D.C. ELECTRICAL CHARACTERISTICS ($0°C < T_A < 70°C$)

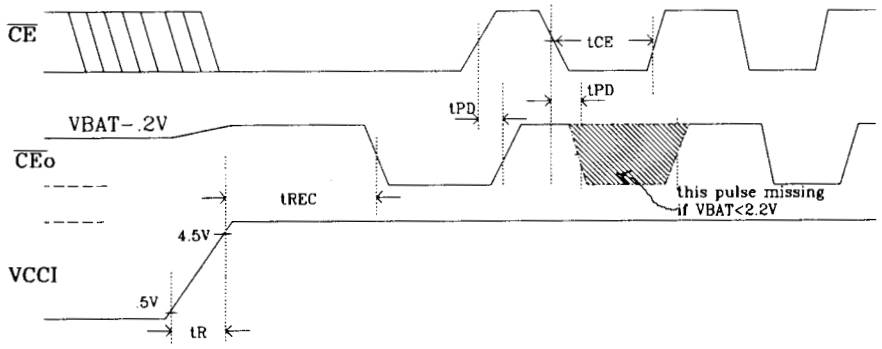
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Standby Current	ICCI			5	mA	VCCI=5.5V,no load
Battery Current	I_{BAT}			100	nA	V_{BAT}=4V,no load
Output Voltage	VCCO1	VCCI-.2			V	VCCI=VTOL=4.5V ICCO1=80 mA
Output Voltage	VCCO2	VBAT-.3			V	VCCI=0,VBAT=2V ICCO2=50 mA
CE output low	V_{OL}			0.4	V	I_L=4 mA, VCCI=4.5V
CE output high	V_{OH}	2.4			V	I_L=-1 mA,VCCI=4.5V
CE output high	V_{OHL}	VBAT-.3			V	VCCI=0, VBAT=2V
VCC Trip Point (TOL=GND)	VCCTP 5%	4.50	4.62	4.74	V	
VCC Trip Point (TOL=VCCO)	VCCTP 10%	4.25	4.37	4.49	V	
VBAT Fail Warning @Power-up	V_{BATF}		2.2		V	VCCI=5V
VBAT Hysteresis	dVBAT		.45		V	VBAT=3V

CMOS Nonvolatile Controller Circuit

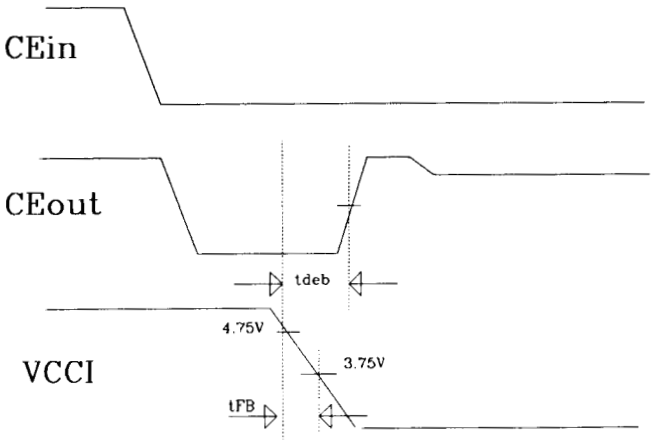
A.C. ELECTRICAL CHARACTERISTICS ($0^oC < T_A < 70^oC$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
CE Propagation Delay	t_{PD}	5	12	20	ns	TTL load (fig.3) VCCI=VTOL=4.5V
CE Pulse Width	t_{CE}			1.5	ms	
VCCI slew rate @ power down	t_{FB}	2			V/ms	
VCCI rise time @ power up	t_R	0			ms	
Power-up Recovery	t_{REC}	2	20	125	ms	VCCI=5V
VCCI debounce time	t_{deb}	6	60	375	ms	
CE_{in} capacitance	C_{in}		5		pF	
CE_{out} capacitance	C_{out}		7		pF	

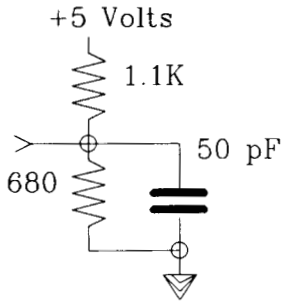
Powerup Timing Diagram



Powerdown Timing Diagram



$\overline{CE}$ output load



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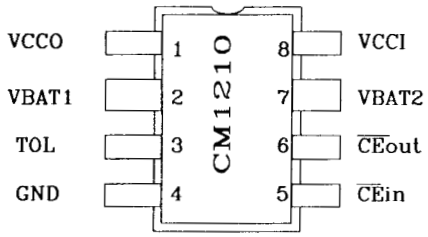
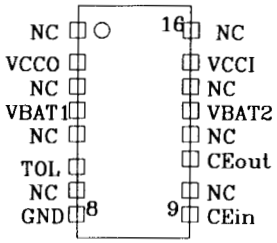
PIN CONFIGURATION



8 PIN DIP



16 PIN SOIC

ORDERING INFORMATION

CM1210	P	I
Product Identification Number	Package Types	Temperature Range
	P - Plastic	None 0°C to +70°C
	S - SOIC, JEDEC	I -40°C to +85°C
	F - SOIC, EIJA	
	C - Ceramic	
	X - Die	