SONY

CXD2458AR

Timing Generator for Color LCD Panels

Description

The CXD2458AR is a timing signal generator for the color LCD panel LCX005BK/BKB, LCX009AK/AKB, LCX024AK and LCX027AK drivers.

Features

- Generates the color LCD panel LCX005BK/BKB, LCX009AK/AKB, LCX024AK and LCX027AK drive pulse
- Supports NTSC/PAL
- Supports 16:9 (WIDE) display (NTSC/PAL)
- Supports composite SYNC and separate SYNC (XHD, XVD) input
- Standby function (low power consumption function)
- Supports right/left inverse display
- AC drive of LCD panels during no signal
- Generates timing signal of external sample-and-hold circuit
- Generates line inversion and field inversion signals
- AFC circuit supporting static and dynamic fluctuations

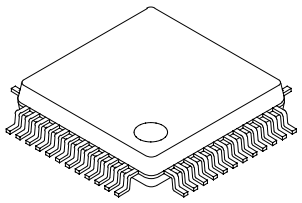
Applications

Color LCD viewfinders, compact LCD projectors, etc.

Structure

Silicon gate CMOS IC

48 pin LQFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

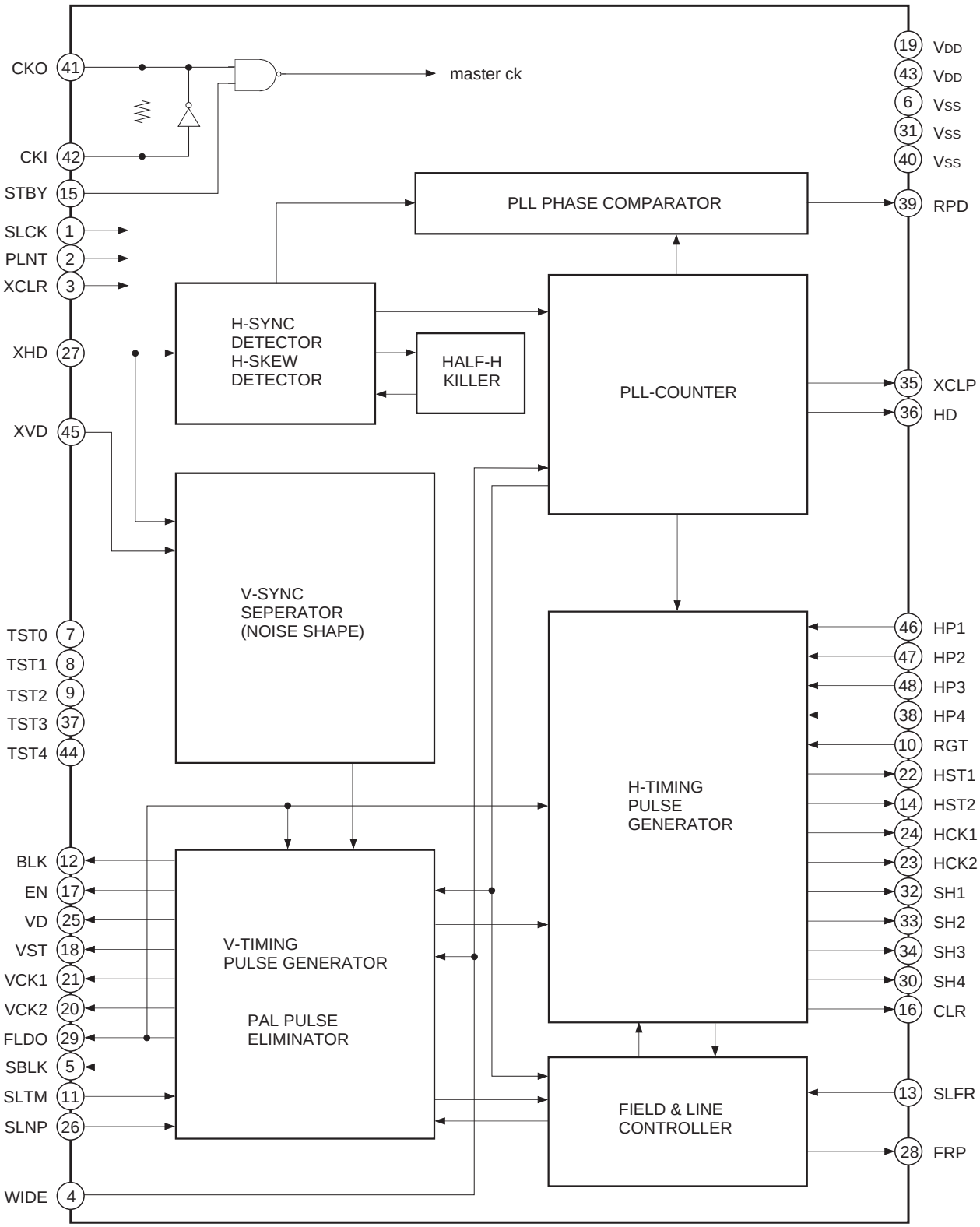
• Supply voltage	V_{DD}	V_{SS} – 0.3 to +6.0	V
• Input voltage	V_I	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Output voltage	V_O	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Operating temperature	Topr	–20 to +85	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	2.7 to 3.3	V
• Operating temperature	Topr	–20 to +85	°C

E98218-PS

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description	Input pin for open status
1	SLCK	I	Switches between LCX005, LCX024 (H) and LCX009, LCX027 (L)	L
2	PLNT	I	Switches between PAL (H) and NTSC (L)	L
3	XCLR	I	Cleared at 0V	H
4	WIDE	I	Switches between 16:9 display (H) and 4:3 display (L)	L
5	SBLK	O	SBLK pulse output (during WIDE MODE) (positive polarity)	—
6	V_{SS}	—	GND	—
7	TST0	I	Test (Leave open.)	L
8	TST1	I	Test (Leave open.)	L
9	TST2	I	Test (Leave open.)	L
10	RGT	I	Switches between Normal scan (H) and Reverse scan (L)	H
11	SLTM	I	Switches between LCX027 (H) and LCX009 (L)	L
12	BLK	O	BLK pulse output (during WIDE MODE) (positive polarity)	—
13	SLFR	I	Switches between field inversion (H) and line inversion (L)	L
14	HST2	O	H start pulse 2 (positive polarity)	—
15	STBY	I	Standby input (H: Operating mode, L: Standby mode)	H
16	CLR	O	CLR pulse output	—
17	EN	O	EN pulse output	—
18	VST	O	V start pulse output	—
19	V_{DD}	—	Power supply	—
20	VCK2	O	V clock pulse 2	—
21	VCK1	O	V clock pulse 1	—
22	HST1	O	H start pulse 1 (positive polarity)	—
23	HCK2	O	H clock pulse 2	—
24	HCK1	O	H clock pulse 1	—
25	VD	O	VD pulse output (positive polarity)	—
26	SLNP	I	Switches between LCX024 (H) and LCX005 (L)	L
27	XHD	I	XHD (negative polarity)/Composite SYNC (positive polarity) input	—
28	FRP	O	AC drive timing pulse	—
29	FLDO	O	Field identification signal	—
30	SH4	O	Sample-and-hold pulse (positive polarity)	—
31	V_{SS}	—	GND	—
32	SH1	O	Sample-and-hold pulse (positive polarity)	—
33	SH2	O	Sample-and-hold pulse (positive polarity)	—
34	SH3	O	Sample-and-hold pulse (positive polarity)	—

Pin No.	Symbol	I/O	Description	Input pin for open status
35	XCLP	O	Burst position clamp pulse (negative polarity)	—
36	HD	O	HD pulse (positive polarity)	—
37	TST3	I	Test (Leave open.)	H
38	HP4	I	Switches the horizontal display position	H
39	RPD	O	Phase comparator output	—
40	V_{SS}	—	GND	—
41	CKO	O	Oscillation cell (output)	—
42	CKI	I	Oscillation cell (input)	—
43	V_{DD}	—	Power supply	—
44	TST4	I	Test (Leave open.)	H
45	XVD	I	XVD (negative polarity) input	L
46	HP1	I	Switches the horizontal display position	L
47	HP2	I	Switches the horizontal display position	L
48	HP3	I	Switches the horizontal display position	L

(H: Pull up, L: Pull down)

Note) The CXD2458AR processes the composite SYNC and separate SYNC inputs with the same pins. Therefore, care should be given to the following points when using the CXD2458AR.

1) During composite SYNC input, the XVD input pin should be set to L or left open.
2) During separate SYNC (XHD, XVD) input, the XVD width specification is from 2H to 10H.

Electrical Characteristics

DC Characteristics

(V_{DD} = 3.0V ± 10%, Topr = –20 to +85°C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit	Remarks
H level input voltage	V_{IH}		0.7V_{DD}			V	*1
L level input voltage	V_{IL}				0.3V_{DD}	V	
H level input current	I_{IH1}	V_I = V_{DD}			1.0	µA	*2
L level input current	I_{IL1}	V_I = 0V			–1.0	µA	
H level input current	I_{IH2}	V_I = V_{DD}	10		180	µA	*3
L level input current	I_{IL2}	V_I = 0V			–3.0	µA	
H level input current	I_{IH3}	V_I = V_{DD}			3.0	µA	*4
L level input current	I_{IL3}	V_I = 0V	–10		–180	µA	
L level output voltage	V_{OL1}	I_{OL} = 1mA			0.2	V	*5
H level output voltage	V_{OH1}	I_{OH} = –250µA	2.6			V	
L level output voltage	V_{OL2}	I_{OL} = 500µA			0.2	V	*6
H level output voltage	V_{OH2}	I_{OH} = –125µA	2.6			V	
L level output voltage	V_{OL3}	I_{OL} = 500µA			0.2	V	*7
H level output voltage	V_{OH3}	I_{OH} = –250µA	2.6			V	
Output leak current	I_{OZ}	At high impedance state	–1.0		1.0	µA	*8
Current consumption	I_{DD}	V_{DD} = 3.0V, STBY = H		12		mA	
		V_{DD} = 3.0V, STBY = L		3		mA	

*1 All input pins.
*2 Input pins XHD and CKI.
*3 Input pins SLNP and XVD.
*4 Input pins XCLR, RGT, STBY, HP4, TST3 and TST4.
*5 Output pins HCK1 and HCK2.
*6 All output pins other than those listed in *5, *7 and *8.
*7 Output pin CKO. However, set the input level of input pin CKI to 0V or V_{DD} during measurement.
*8 Output pin RPD.

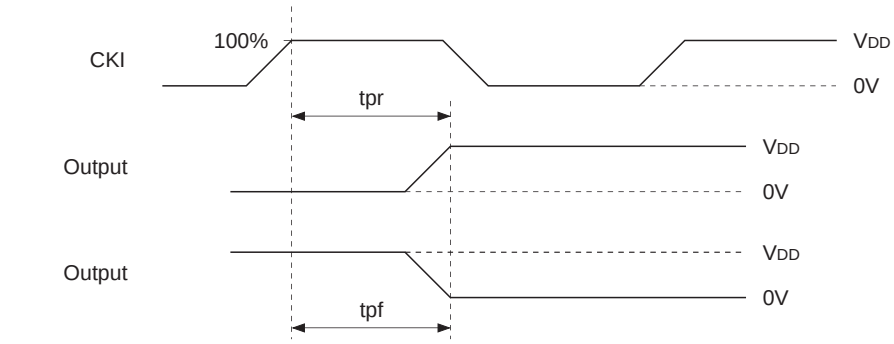
AC Characteristics

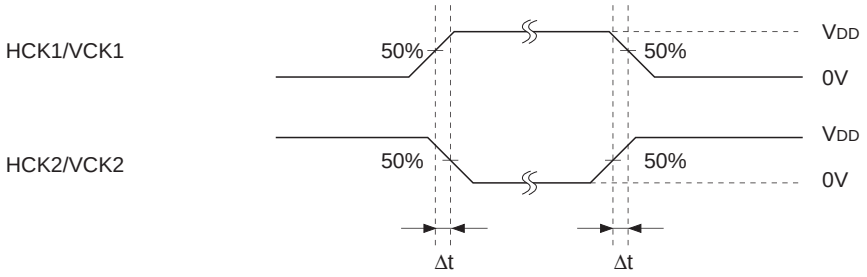
(V_{DD} = 3.0V ± 10%, Topr = –20 to +85°C)

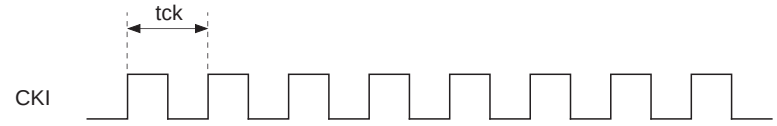
Item	Applicable pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock input cycle	CKI	tck		60			ns
Cross-point time difference	HCK1, HCK2	∆t	CL = 30pF	1		15	ns
	VCK1, VCK2		CL = 30pF	3		20	ns
Output rise delay time	VCKn, HCKn	tpr	CL = 30pF			84	ns
	Other than HCKn and VCKn		CL = 30pF			76	ns
Output fall delay time	VCKn, HCKn	tpf	CL = 30pF			71	ns
	Other than HCKn and VCKn		CL = 30pF			62	ns
HCK1, SH1 delay time difference	HCK1, SH1	dt1	CL = 30pF	1		5	ns
HCK2, SH1 delay time difference	HCK2, SH1	dt2	CL = 30pF	1		5	ns
HCK Duty	HCK1, HCK2	dtyH	CL = 30pF	48		53	%

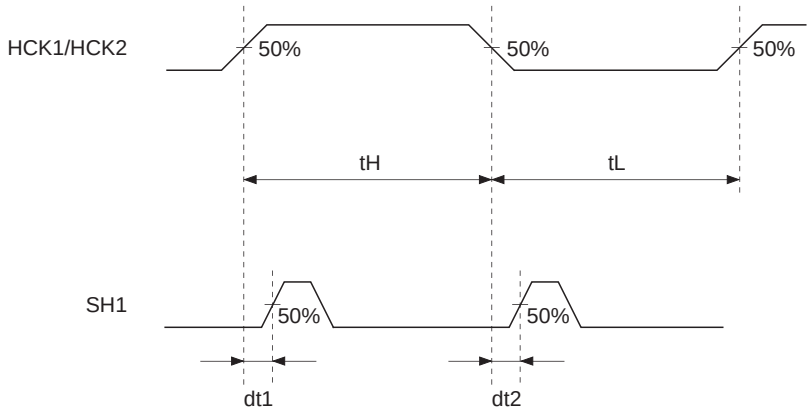
Timing Definition

AC Characteristics

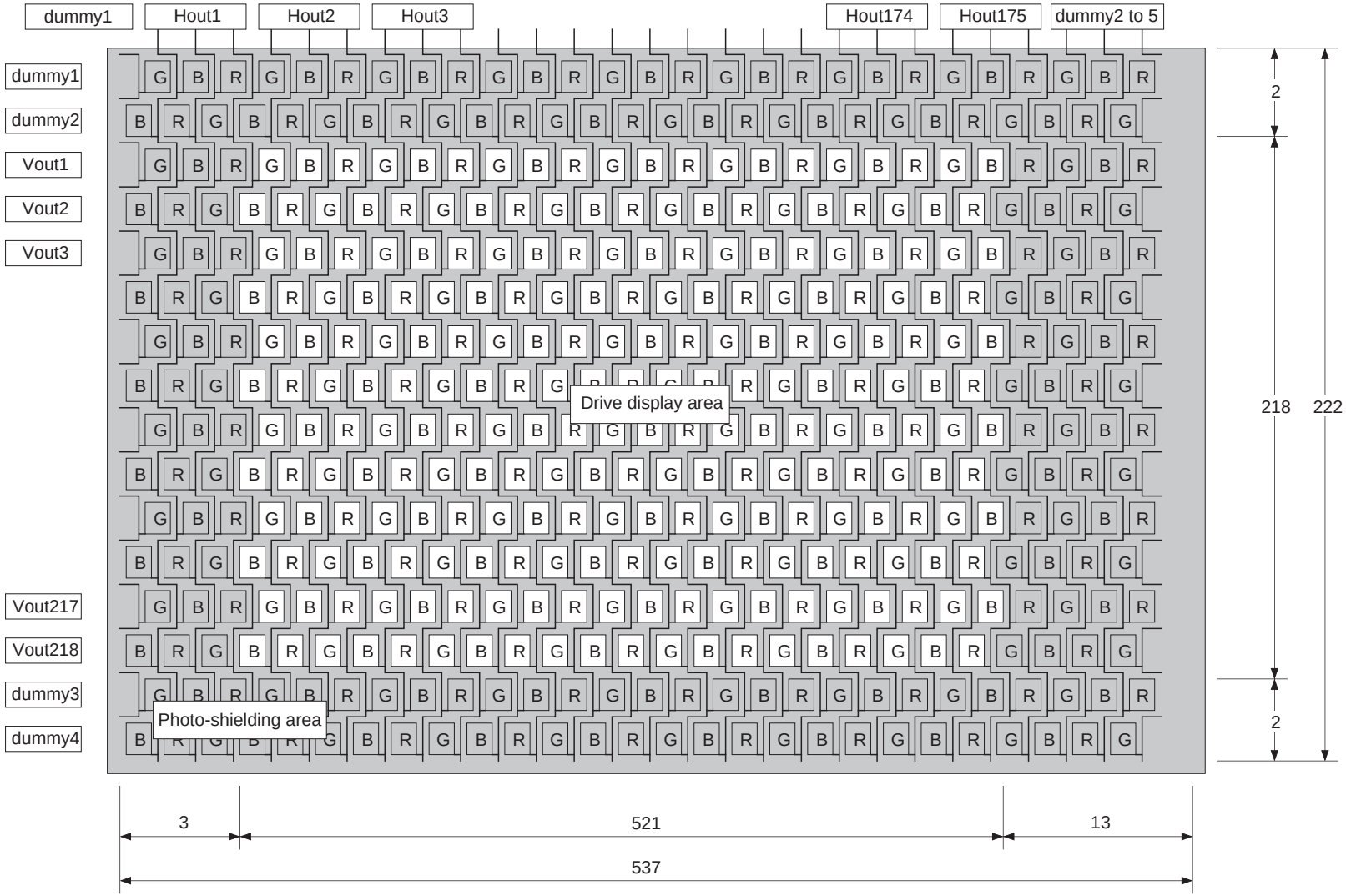




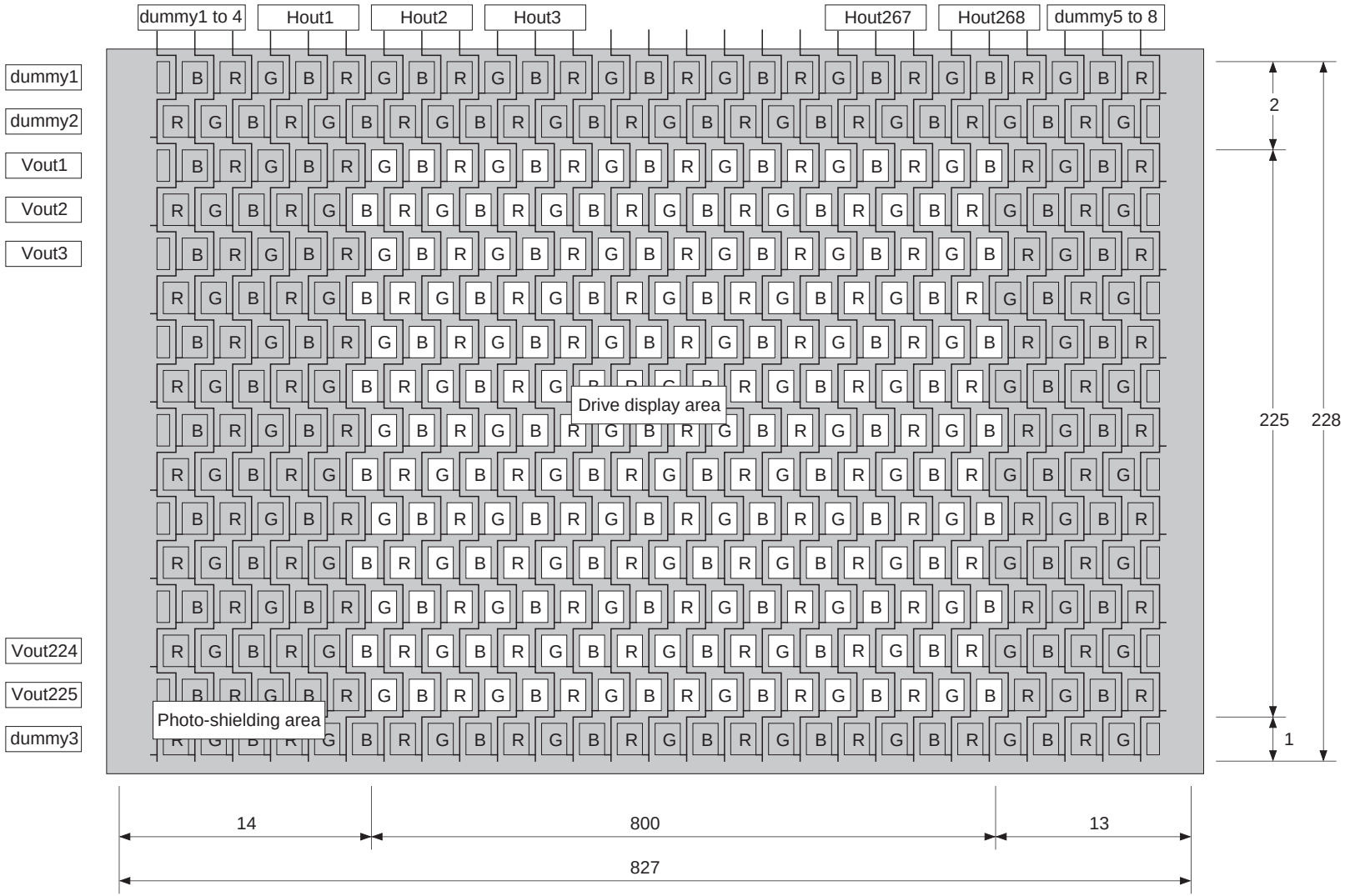




LCX005BK/BKB, LCX024AK Pixel Arrangement



LCX009AK/AKB, LCX027AK Pixel Arrangement



Description of Mode Selection Switch (SLCK, SLTM, SLNP, PLNT, WIDE)

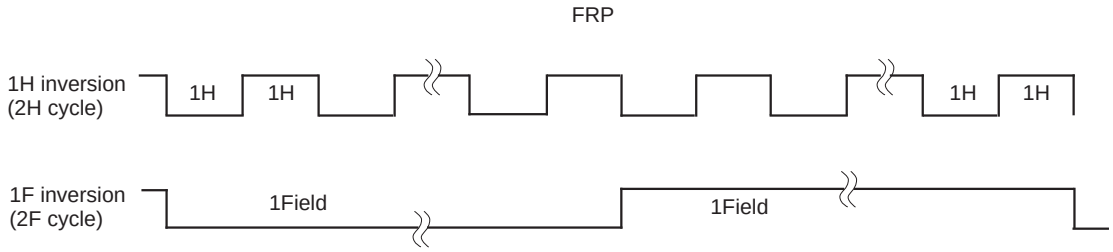
SLCK	SLTM	SLNP	PLNT	WIDE	MODE
H	X	L	L	L	LCX005BK/BKB, NTSC, NORMAL
H	X	L	L	H	LCX005BK/BKB, NTSC, WIDE
H	X	L	H	L	LCX005BK/BKB, PAL, NORMAL
H	X	L	H	H	LCX005BK/BKB, PAL, WIDE
H	X	H	L	L	LCX024AK, NTSC, NORMAL
H	X	H	L	H	LCX024AK, NTSC, WIDE
H	X	H	H	L	LCX024AK, PAL, NORMAL
H	X	H	H	H	LCX024AK, PAL, WIDE
L	L	X	L	L	LCX009AK/AKB, NTSC, NORMAL
L	L	X	L	H	LCX009AK/AKB, NTSC, WIDE
L	L	X	H	L	LCX009AK/AKB, PAL, NORMAL
L	L	X	H	H	LCX009AK/AKB, PAL, WIDE
L	H	X	L	L	LCX027AK, NTSC, NORMAL
L	H	X	L	H	LCX027AK, NTSC, WIDE
L	H	X	H	L	LCX027AK, PAL, NORMAL
L	H	X	H	H	LCX027AK, PAL, WIDE

* NORMAL (4:3 display), WIDE (16:9 display)

∗ X: Don't Care

SLFR

SLFR is the selector switch for the AC drive timing pulse (FRP). This switch selects field inversion when H and line inversion when L. Normally, line inversion (L) is used. The transition point is one clock cycle after the transition point of the VCK1 and VCK2 pulses.



* FRP polarity is not specified.

AFC Circuit (PLL Method)

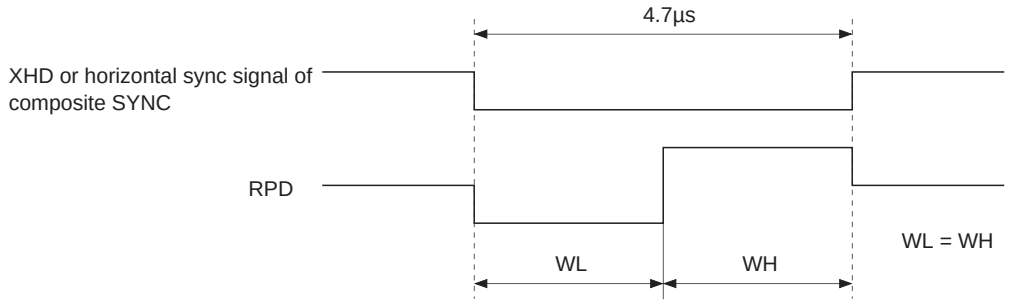
The CXD2458AR employs the PLL method in order to achieve phase synchronization with the input sync signal.

The PLL circuit phase comparator and frequency division counter are built in, and a fully synchronized AFC circuit is comprised by connecting an external VCO circuit and LPF.

PLL errors are detected at the following timing.

The phase comparison output of the entire bottom of XHD or the horizontal sync signal of composite SYNC and the internal H counter becomes RPD. RPD output is converted to DC error with the lag-lead filter (LPF), and then it changes the varicap capacitance to stabilize the oscillating frequency at 702fh in the LCX005BK/BKB and LCX024AK, and 1050fh in the LCX009AK/AKB and LCX027AK.

This PLL circuit is adjusted by setting the RPD transition point so that it sets in the center of the window (XHD or horizontal sync signal of composite SYNC) as shown in the figure below.



AC Driving for No Signal

HST1/2, HCK1/2, FRP, VCK1/2, XCLP, VST, HD, VD, SH1/2/3/4 and EN are made to run freely so that the LCD panel is AC driven even when there are no input sync signals (XHD/XVD and composite SYNC).

During this time, the horizontal sync separation circuit stops and the PLL internal frequency division counter is made to run freely. At the same time, the auxiliary V counter is used to create the reference pulse for generating the free running VD and VST because the vertical sync separation circuit is also stopped.

The cycle of this V counter is set to 269H for NTSC and 321H for PAL. However, when there is no XVD (VSYNC) input for 301H (NTSC) and 360H (PAL), the no signal state is assumed and the free running VD and VST pulses are generated from the next field.

RPD is kept at high impedance when there is no signal in order to prevent the AFC circuit from causing phase errors due to phase comparison.

System Clear (XCLR)

The entire logic is initialized by setting XCLR = L. Be sure to perform this operation during power-on and after changing the STBY pin from L to H. When this function is activated the outputs (XCLP, HD, FRP, VST, VD, CLR, EN, HST1/2, HCK1/2, SH1/2/3/4, VCK1/2, FLDO, SBLK and BLK) go to L.

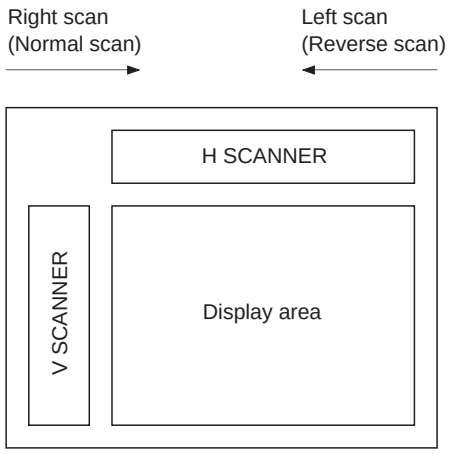
Right/Left Inverse Display

The CXD2458AR outputs a right/left inversion timing pulse that supports the right/left inverse display function of the LCX005BK/BKB, LCX024AK, LCX009AK/AKB and LCX027AK.

The LCD panel is arranged in a delta pattern, where the same signal line is 1.5-dot offset at adjoining vertical lines. For this reason, a 1.5-dot offset is attached to the horizontal start pulse (HST) of the LCD between odd lines and even lines in order to correct this difference. Other H system output pulses are also 1.5-dot offset.

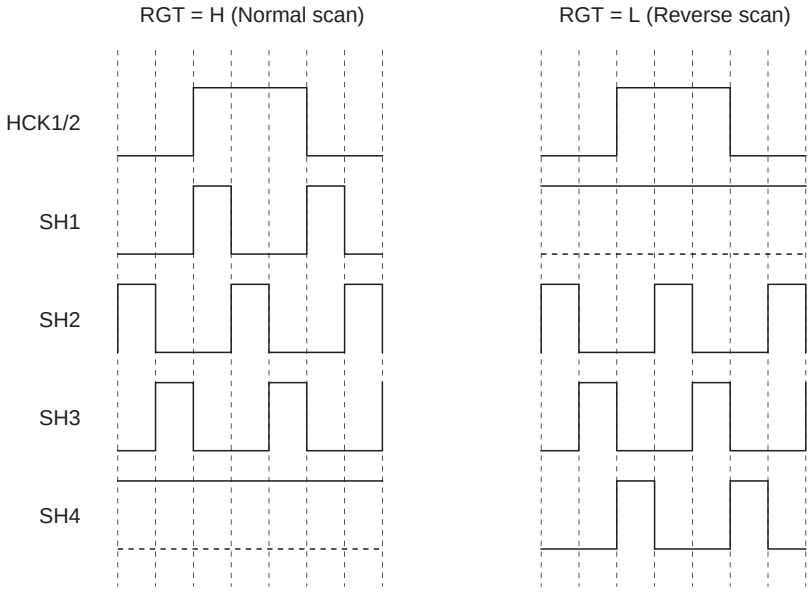
When the panel is driven with left scan (Reverse scan), this offset relationship becomes inverted for even and odd lines, and the asymmetrical dot arrangement produces an offset.

Therefore, the CXD2458AR internally controls the right/left and interline offset to allow right scan or left scan display by setting RGT = H or L for right/left inversion.



SH Pulse and HCK Phase Relationship

The phase relationship between the SH pulse and HCK changes according to switching between right scan (Normal scan) and left scan (Reverse scan). SH3 is the re-sampling pulse.

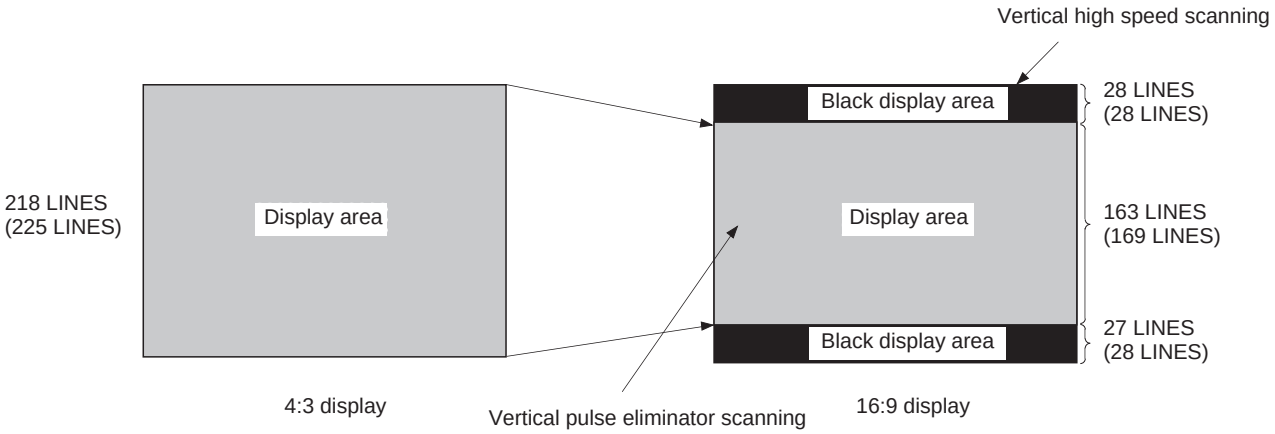


16:9 (WIDE) Display Mode

Setting the WIDE pin to H shifts the unit to WIDE display mode. In this mode, the aspect ratio is converted through pulse eliminator processing, allowing 16:9 quasi-WIDE display.

Vertical pulse eliminator scanning of 1/4 (NTSC) and 2/6 (PAL) for the LCX005BK/BKB and LCX009AK/AKB, and 1/4 (NTSC) and 10/28 (PAL) for the LCX024AK and LCX027AK is performed, and the video signal is compressed in the display area compared to 4:3 display to achieve 16:9 (WIDE) display. In addition, in areas outside the display area, vertical high-speed scanning is performed and black signals are written to the black display area in the upper 28 lines and the lower 27 or 28 lines. During this period, the FRP and HST output cycles are also changed, and EN and CLR are not output. In addition, the SBLK output, which is the black signal generation timing pulse, and the LCX024AK/LCX027AK black display area control signal BLK are both H.
(For example, black display in the panel is permitted by connecting the SBLK output to the external RGB input pin of the CXA1785AR.)

See the Timing Charts for details.



* Numbers in parentheses are for the LCX009AK/AKB and LCX027AK.

Note) When the no signal status occurs during 16:9 (WIDE) display mode, 4:3 display mode results.

HP1, 2, 3, 4

These are selector switches for the horizontal display position. The HST timing can be set at 2fh intervals in 16 different ways by using the four HP1, 2, 3 and 4 bits. The picture center is set at internal preset value: HP1/2/3/4: LLLH. However, because there is actually a difference between the RGB signal and the drive pulse delays, the picture center may not match the design center. In this case, adjust with these switches.
The HST timing (from SYNC termination to the rising edge of HST) for even lines is shown below.

LCX005BK/BKB, LCX024AK (NTSC/PAL)

HP4	HP3	HP2	HP1	HST1 (NTSC/PAL)	HST2 (NTSC/PAL)
0	0	0	0	72fh (6.51/6.56µs)	74.5fh (6.74/6.79µs)
0	0	0	1	70fh	72.5fh
0	0	1	0	68fh	70.5fh
0	0	1	1	66fh	68.5fh
0	1	0	0	64fh	66.5fh
0	1	0	1	62fh	64.5fh
0	1	1	0	60fh	62.5fh
0	1	1	1	58fh	60.5fh
1	0	0	0	56fh (5.06/5.11µs)	58.5fh (5.29/5.33µs)
1	0	0	1	54fh	56.5fh
1	0	1	0	52fh	54.5fh
1	0	1	1	50fh	52.5fh
1	1	0	0	48fh	50.5fh
1	1	0	1	46fh	48.5fh
1	1	1	0	44fh	46.5fh
1	1	1	1	42fh (3.80/3.83µs)	44.5fh (4.02/4.06µs)

* The HST1 and 2 timing for odd lines is 1.5fh delayed and 1.5fh advanced respectively from the above timings. (See the Timing Charts for details.)

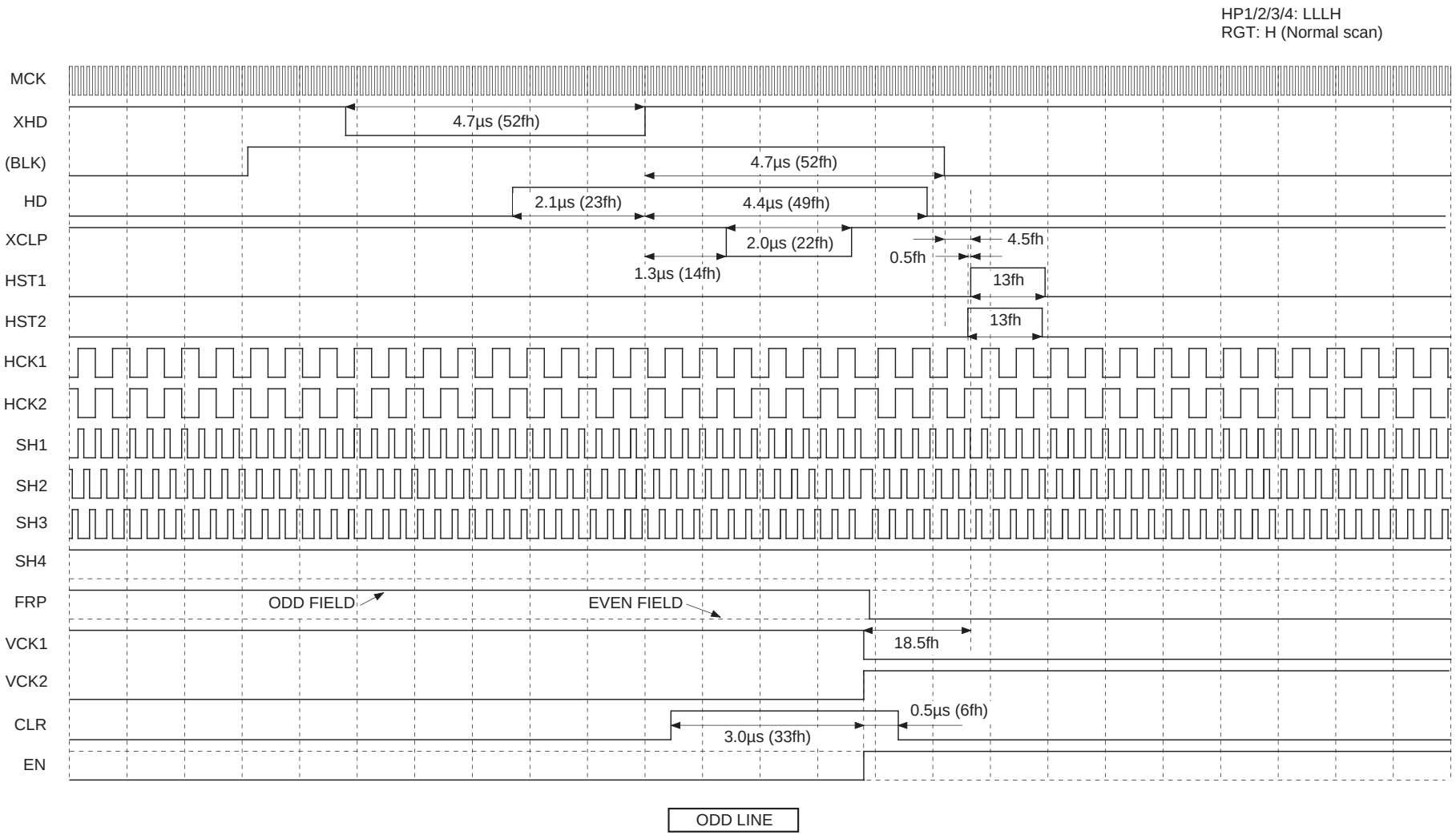
LCX009AK/AKB, LCX027AK (NTSC/PAL)

HP4	HP3	HP2	HP1	HST1 (NTSC/PAL)	HST2 (NTSC/PAL)
0	0	0	0	91fh (5.51/5.55µs)	93.5fh (5.66/5.70µs)
0	0	0	1	89fh	91.5fh
0	0	1	0	87fh	89.5fh
0	0	1	1	85fh	87.5fh
0	1	0	0	83fh	85.5fh
0	1	0	1	81fh	83.5fh
0	1	1	0	79fh	81.5fh
0	1	1	1	77fh	79.5fh
1	0	0	0	75fh (4.54/4.57µs)	77.5fh (4.69/4.72µs)
1	0	0	1	73fh	75.5fh
1	0	1	0	71fh	73.5fh
1	0	1	1	69fh	71.5fh
1	1	0	0	67fh	69.5fh
1	1	0	1	65fh	67.5fh
1	1	1	0	63fh	65.5fh
1	1	1	1	61fh (3.69/3.72µs)	63.5fh (3.84/3.87µs)

* The HST1 and 2 timing for odd lines is 1.5fh delayed and 1.5fh advanced respectively from the above timings. (See the Timing Charts for details.)

LCX005BK/BKB, LCX024AK Horizontal Direction Timing Chart

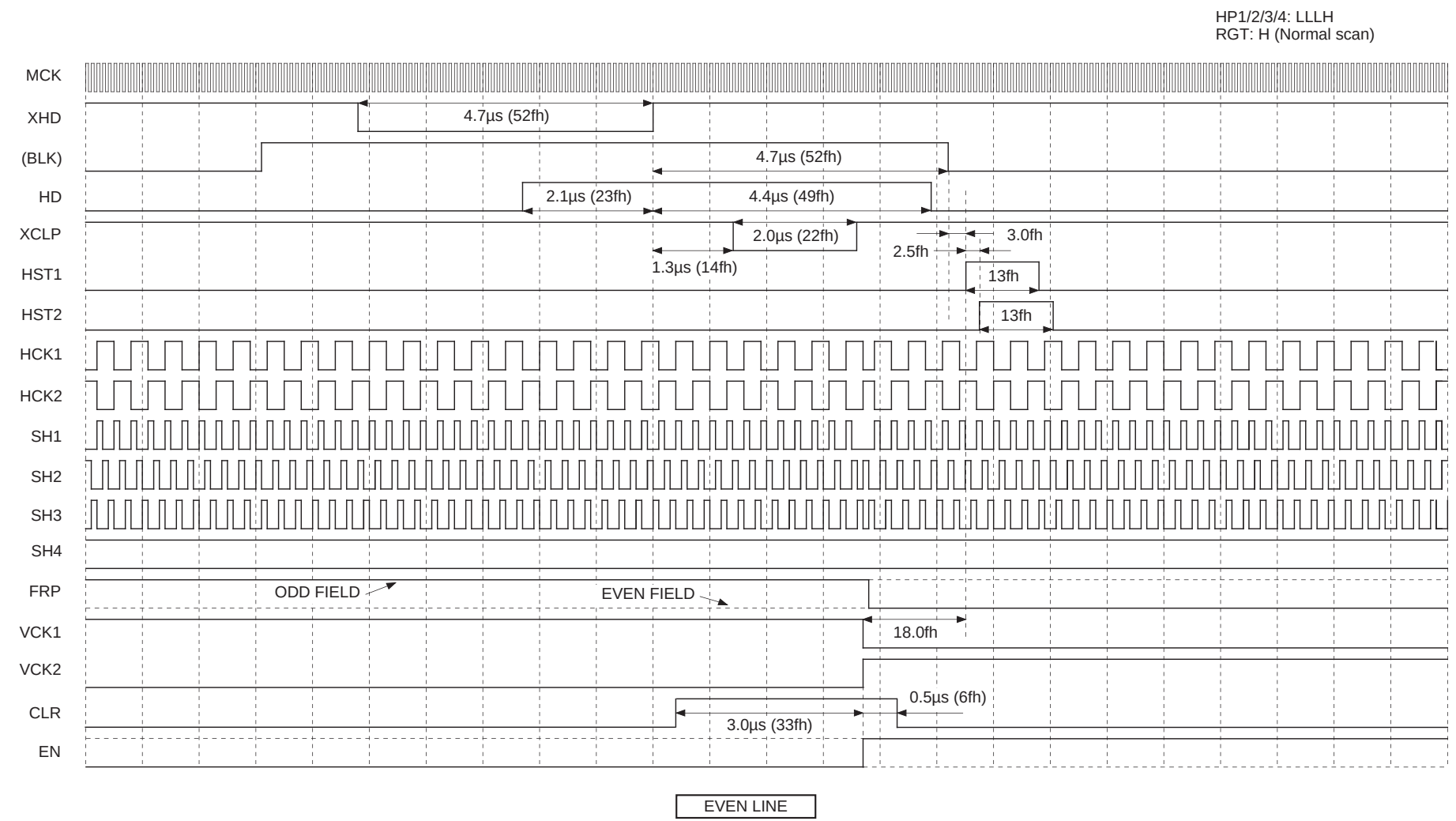
NTSC/PAL



Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB, LCX024AK Horizontal Direction Timing Chart

NTSC/PAL

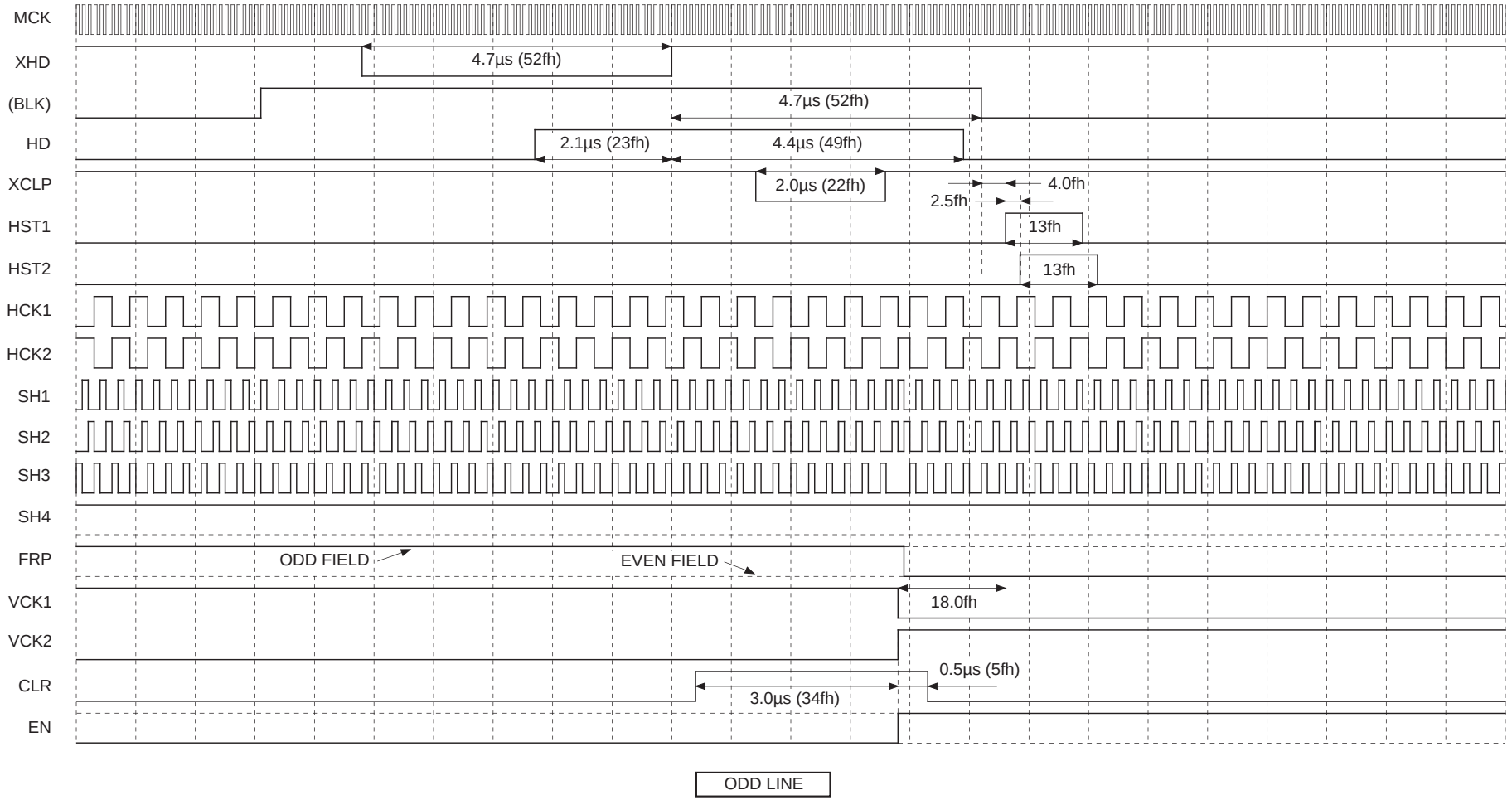


Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB, LCX024AK Horizontal Direction Timing Chart

NTSC/PAL

HP1/2/3/4: LLLH
RGT: L (Reverse scan)

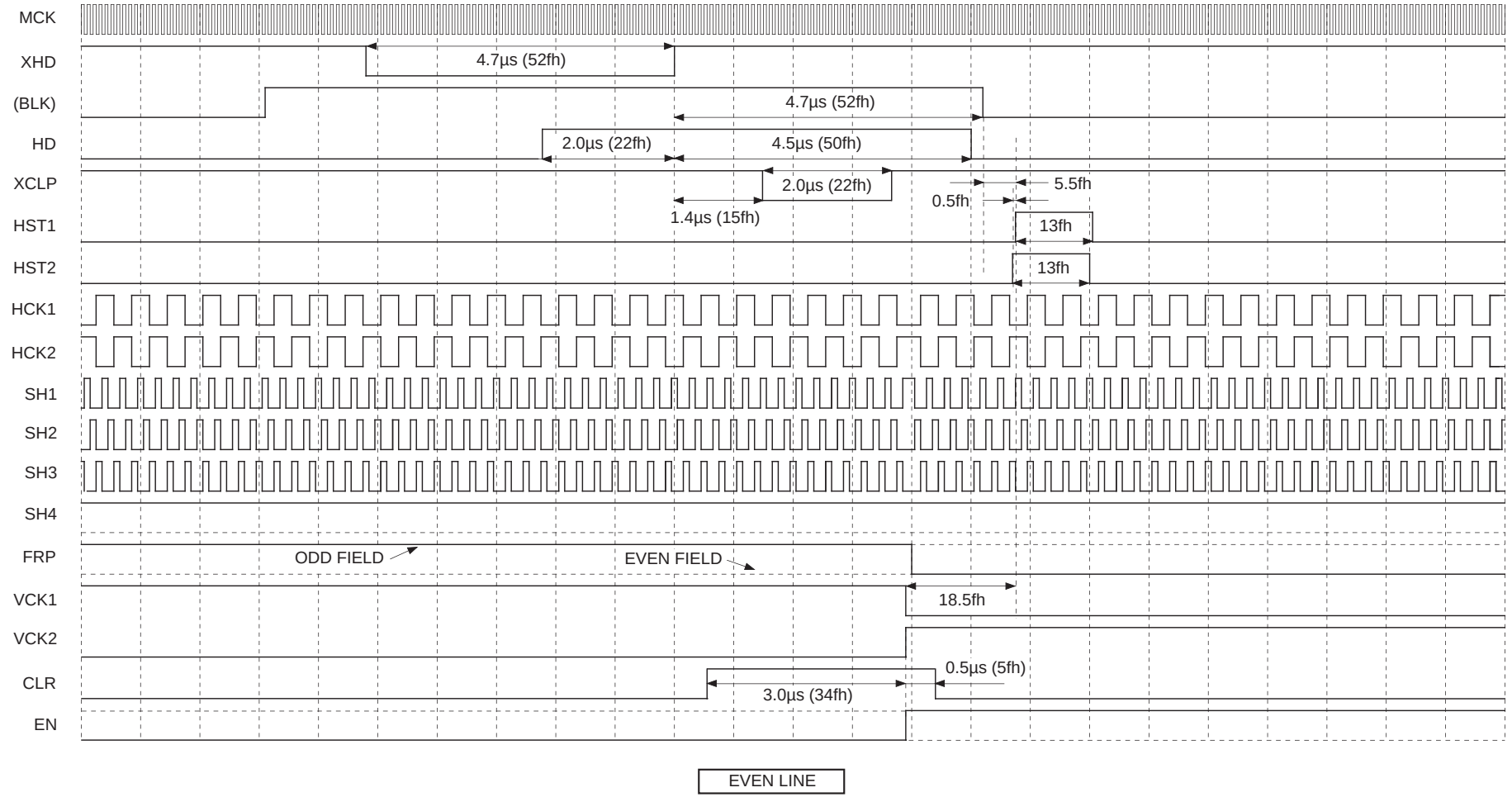


Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB, LCX024AK Horizontal Direction Timing Chart

NTSC/PAL

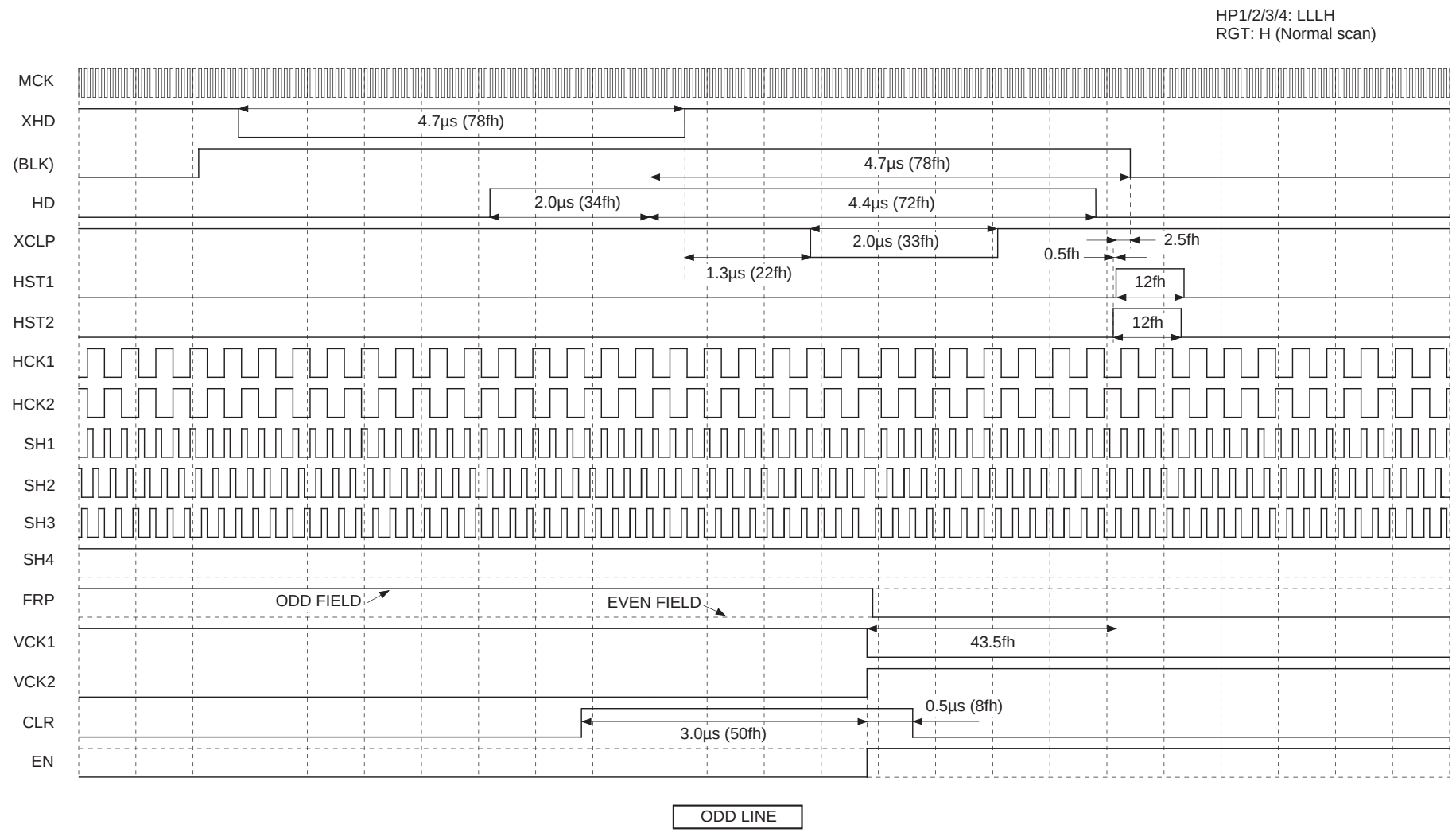
HP1/2/3/4: LLLH
RGT: L (Reverse scan)



Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB, LCX027AK Horizontal Direction Timing Chart

NTSC/PAL

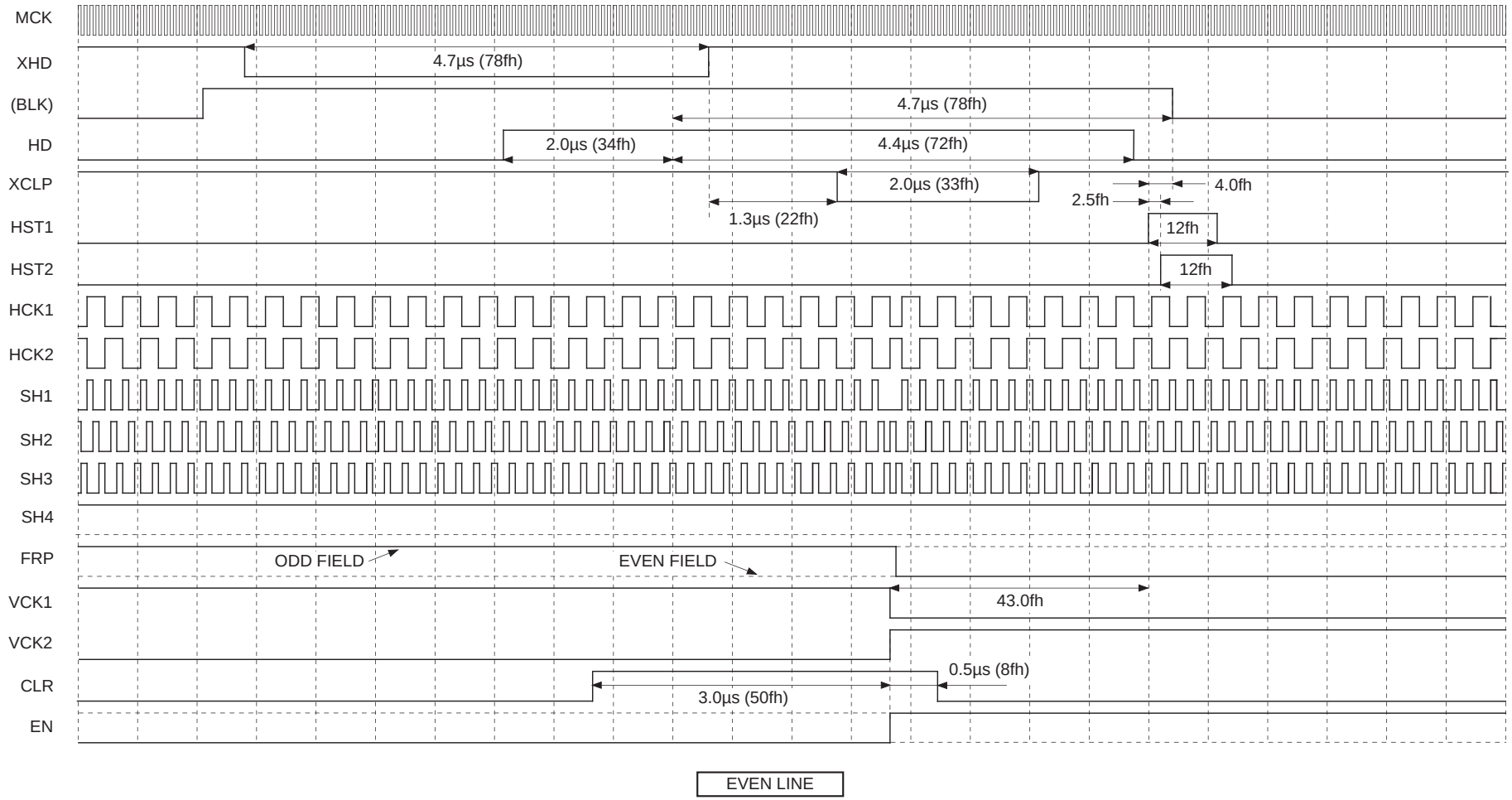


Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB, LCX027AK Horizontal Direction Timing Chart

NTSC/PAL

HP1/2/3/4: LLLH
RGT: H (Normal scan)

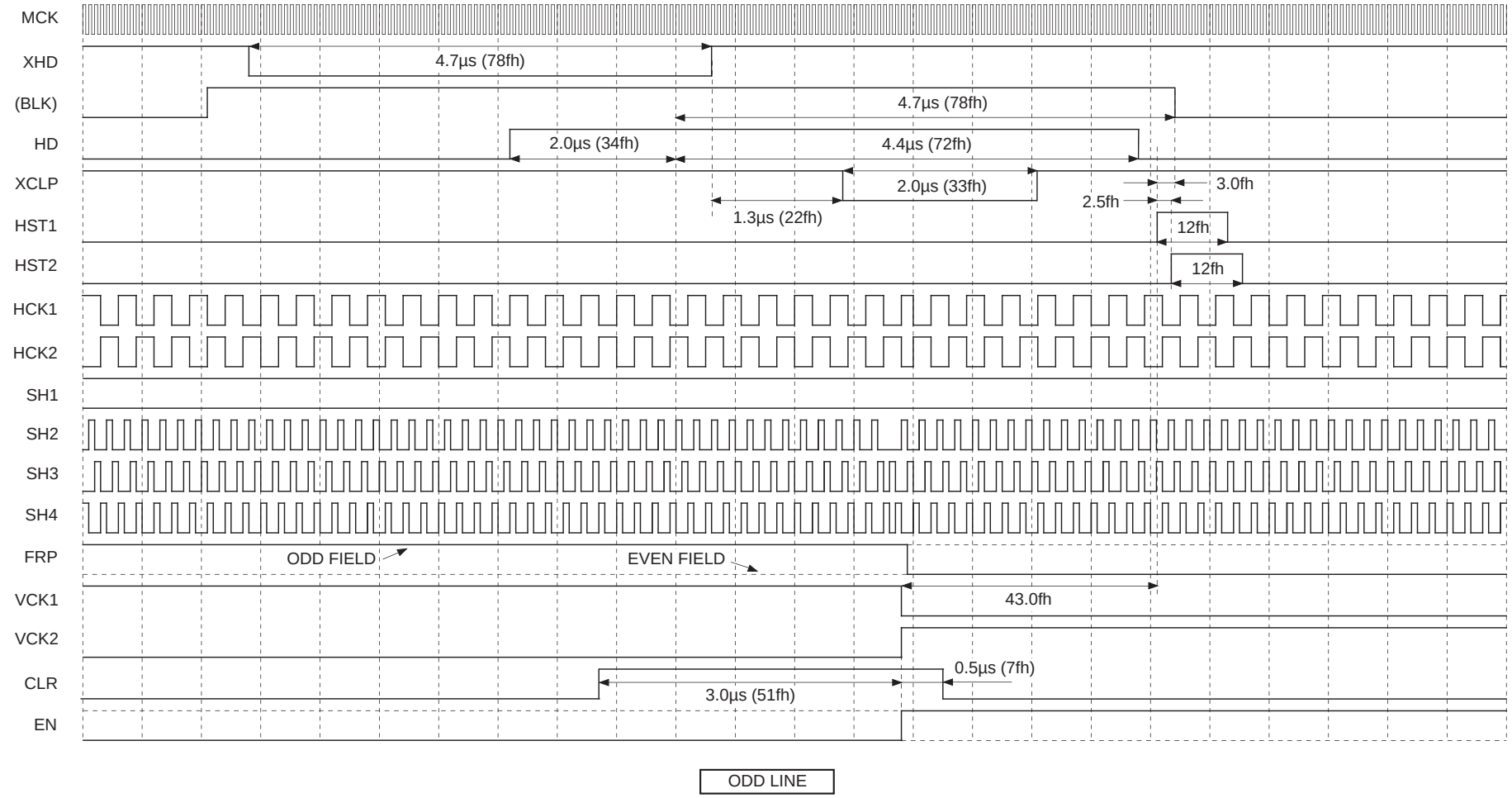


Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB, LCX027AK Horizontal Direction Timing Chart

NTSC/PAL

HP1/2/3/4: LLLH
RGT: L (Reverse scan)

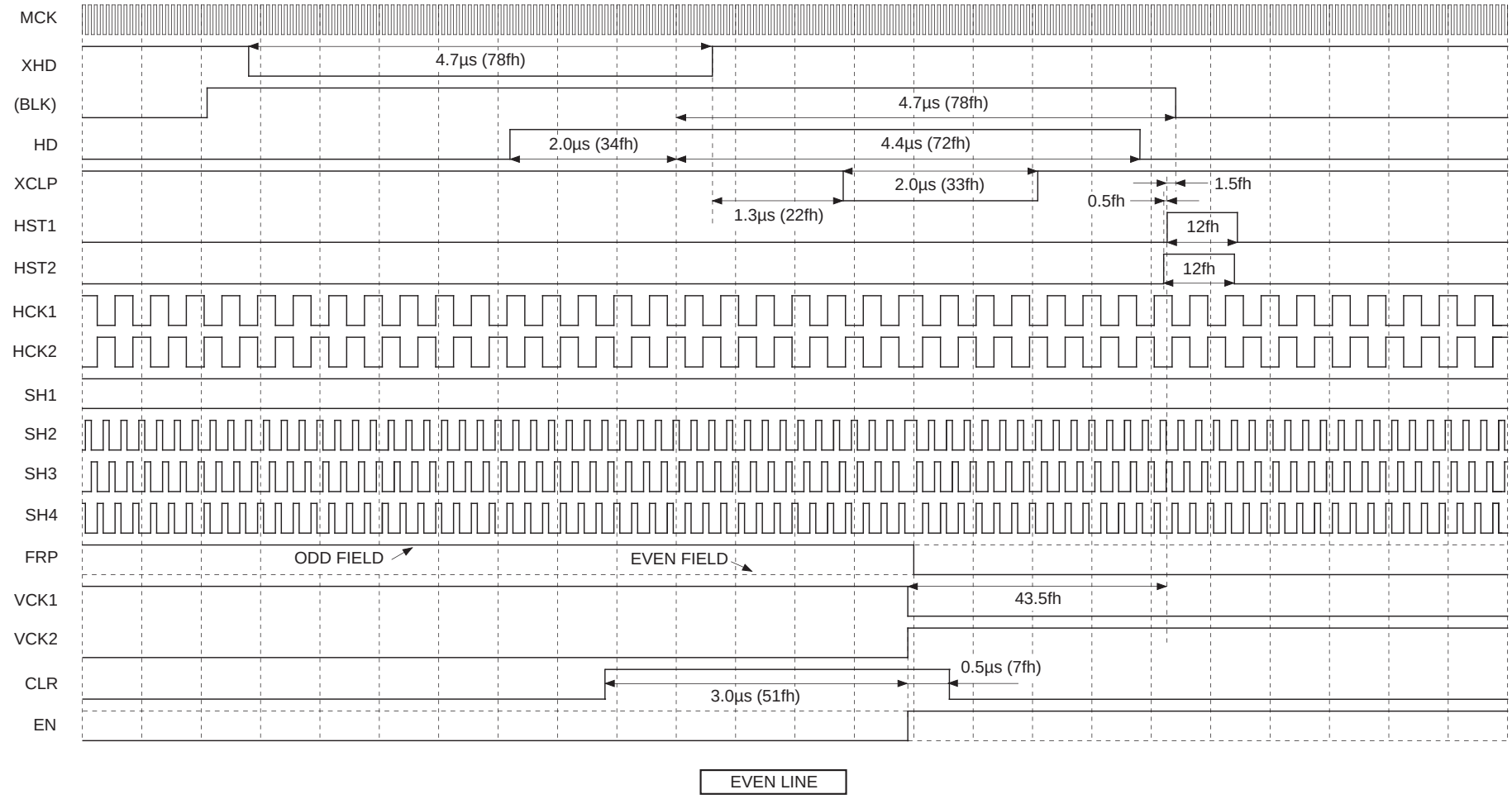


Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB, LCX027AK Horizontal Direction Timing Chart

NTSC/PAL

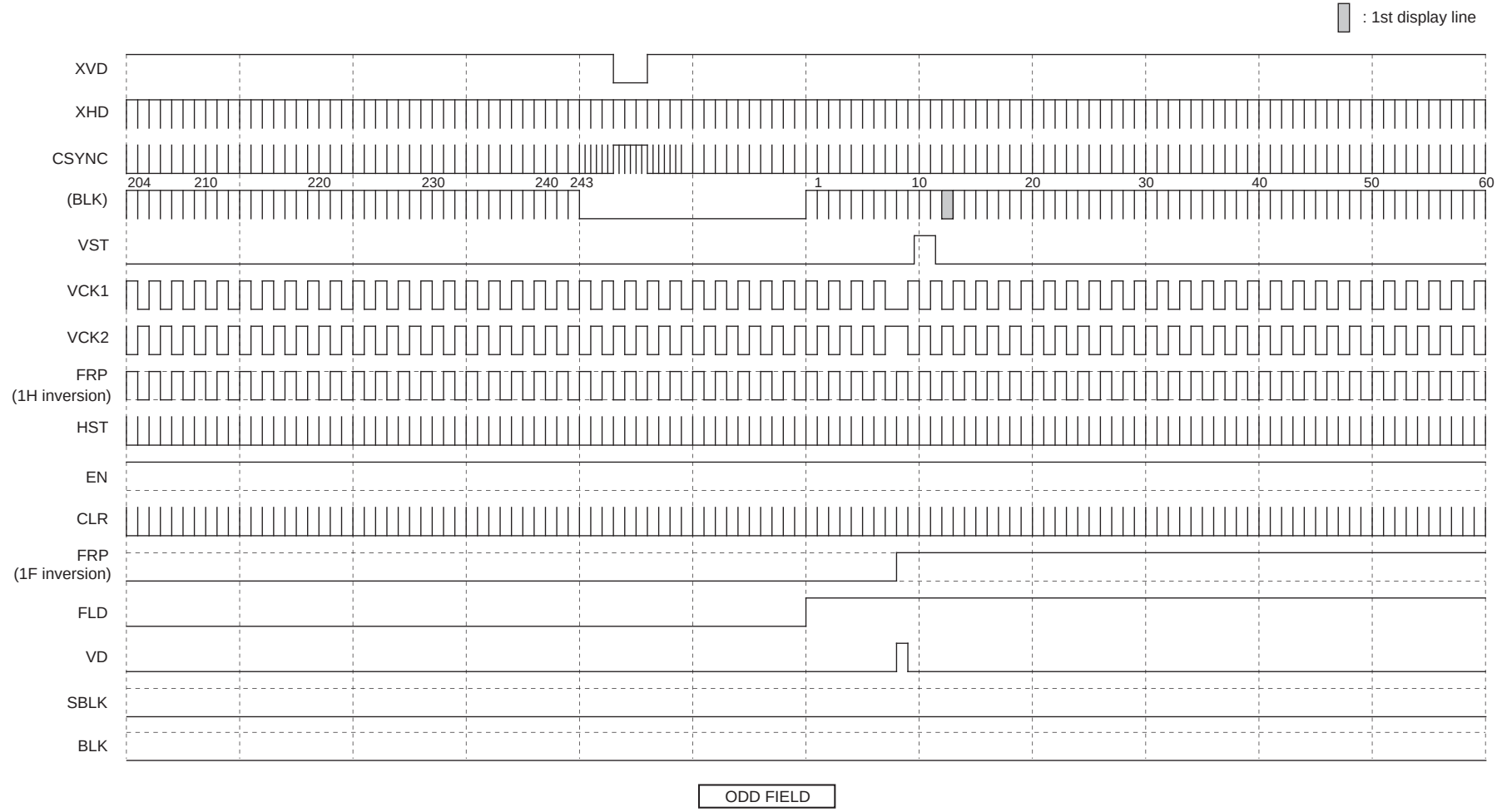
HP1/2/3/4: LLLH
RGT: L (Reverse scan)



Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

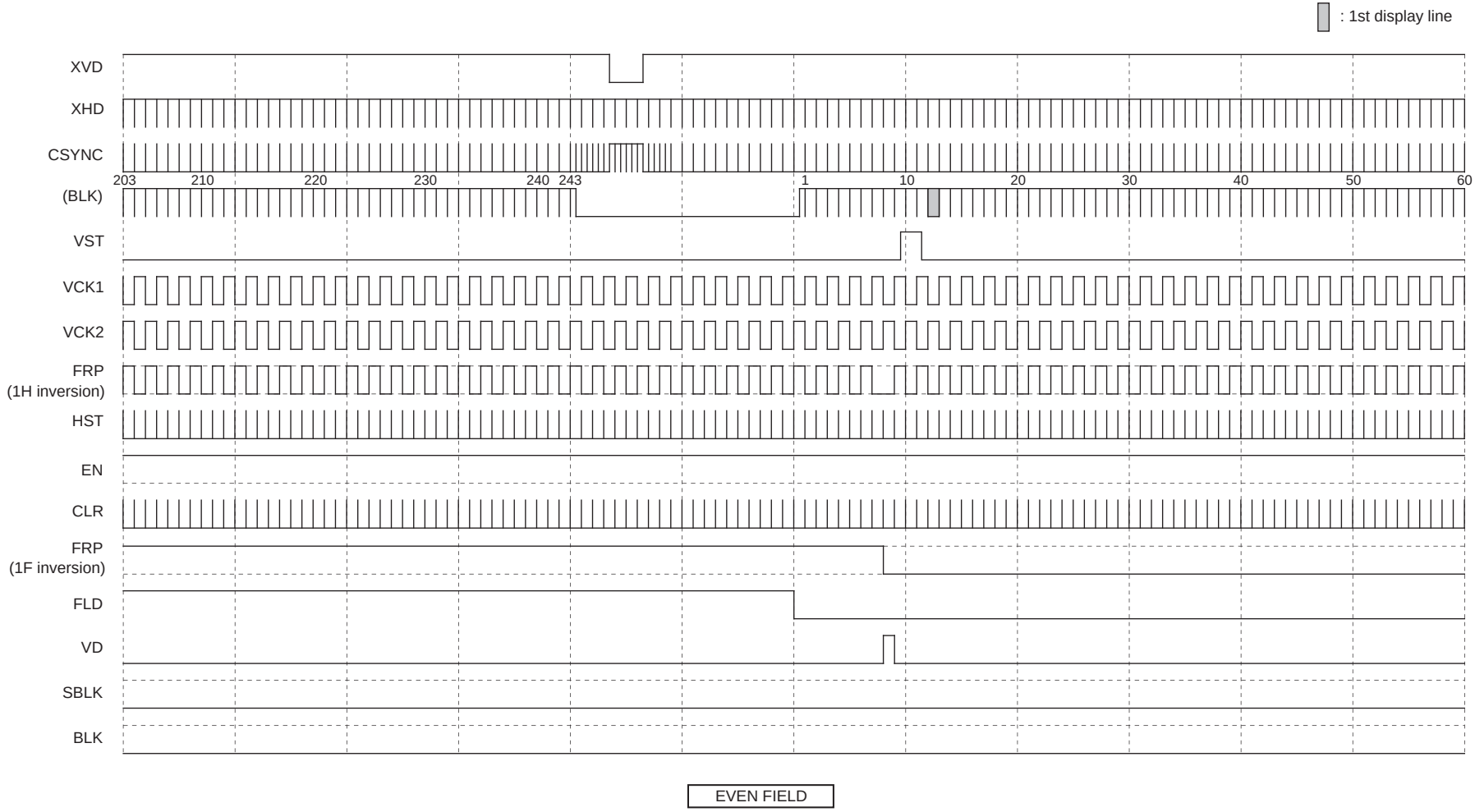
NTSC



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

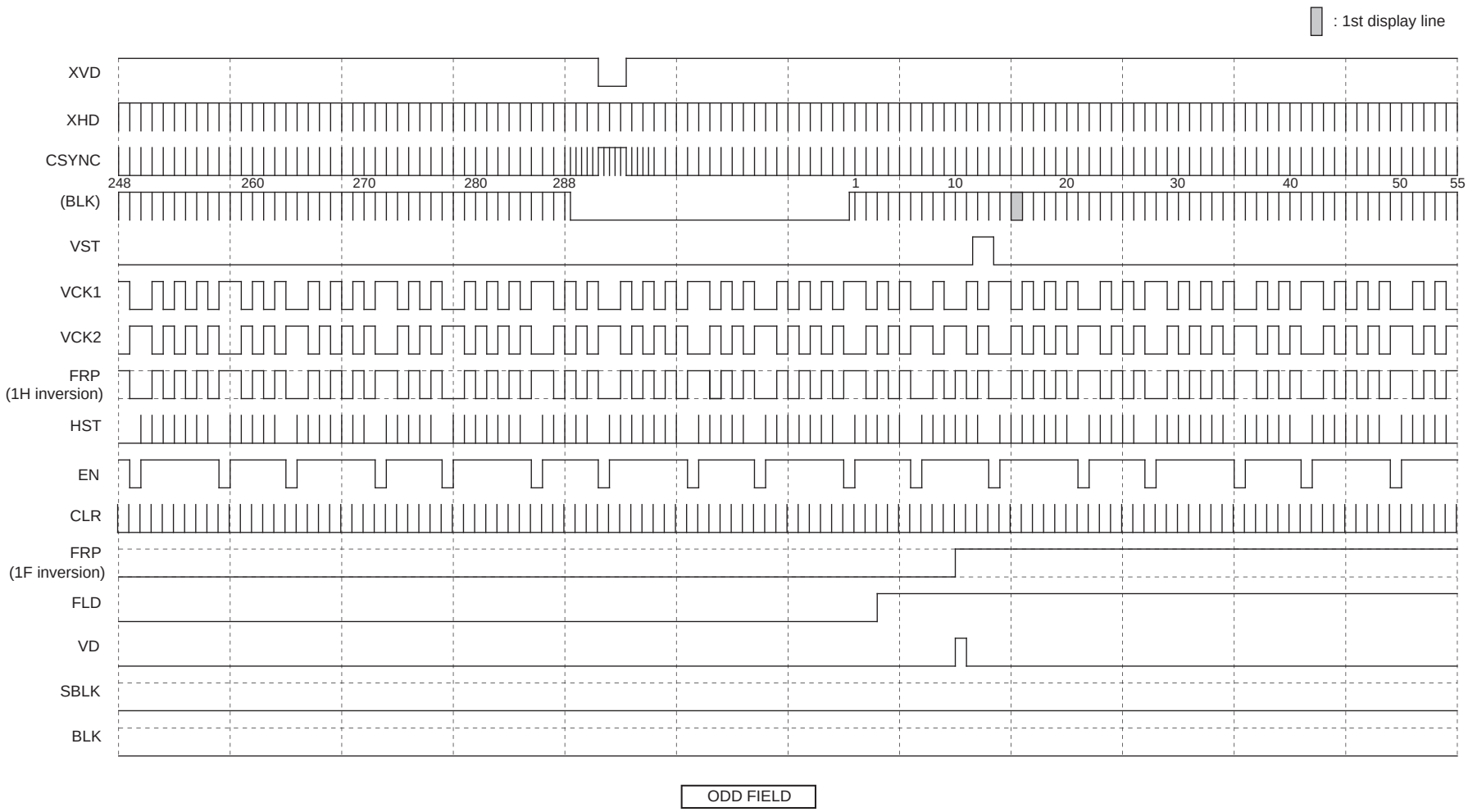
NTSC



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

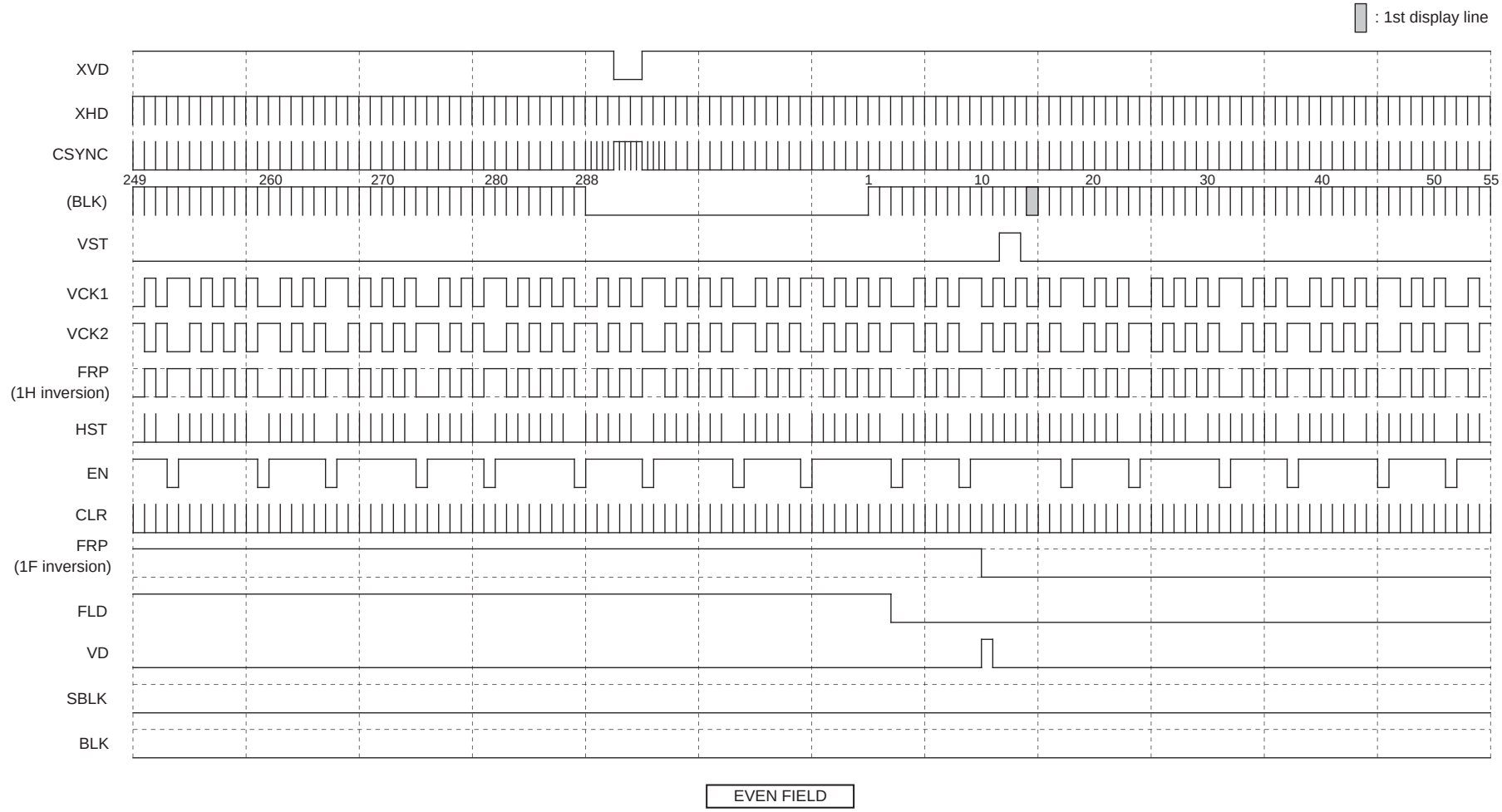
PAL



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

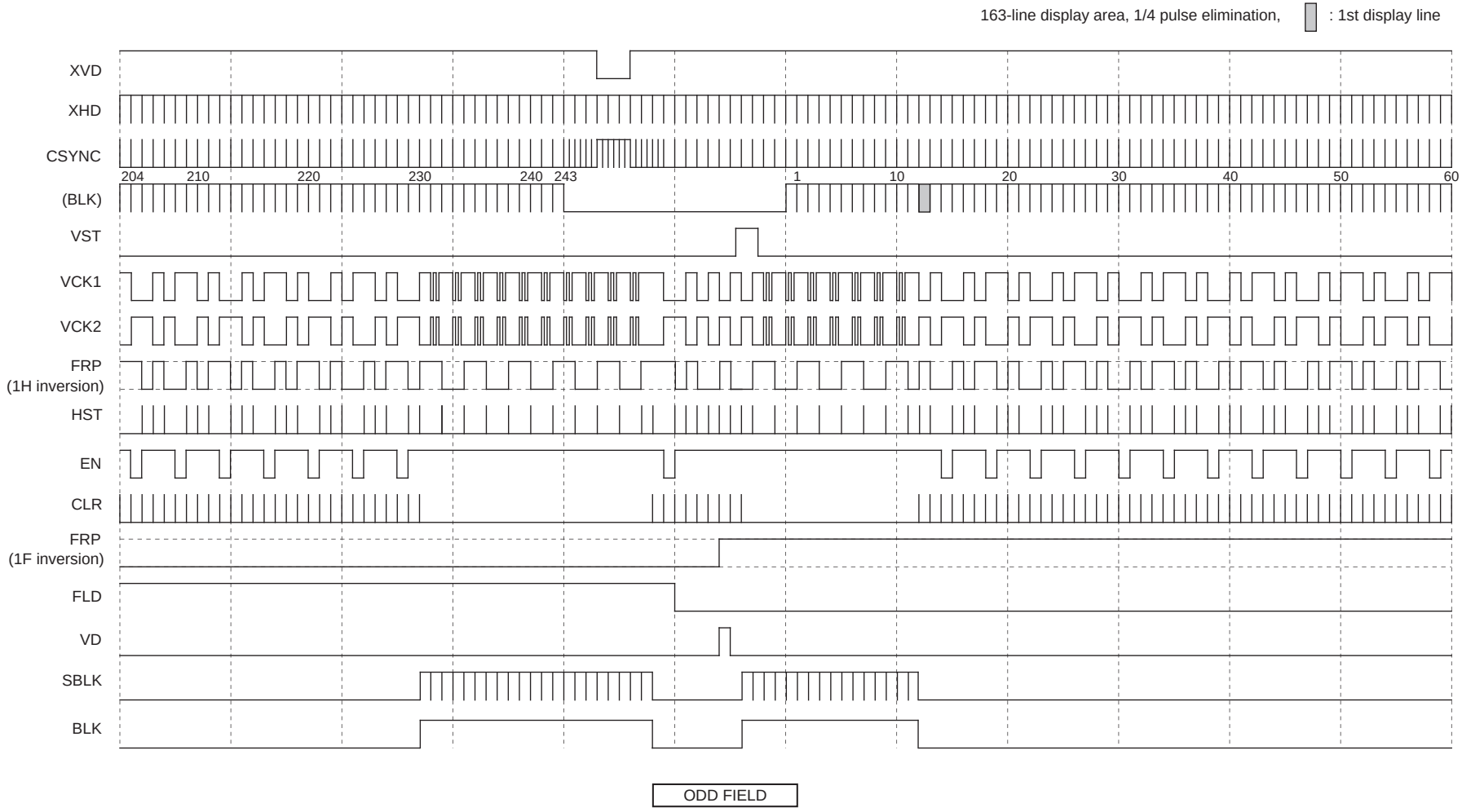
PAL



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

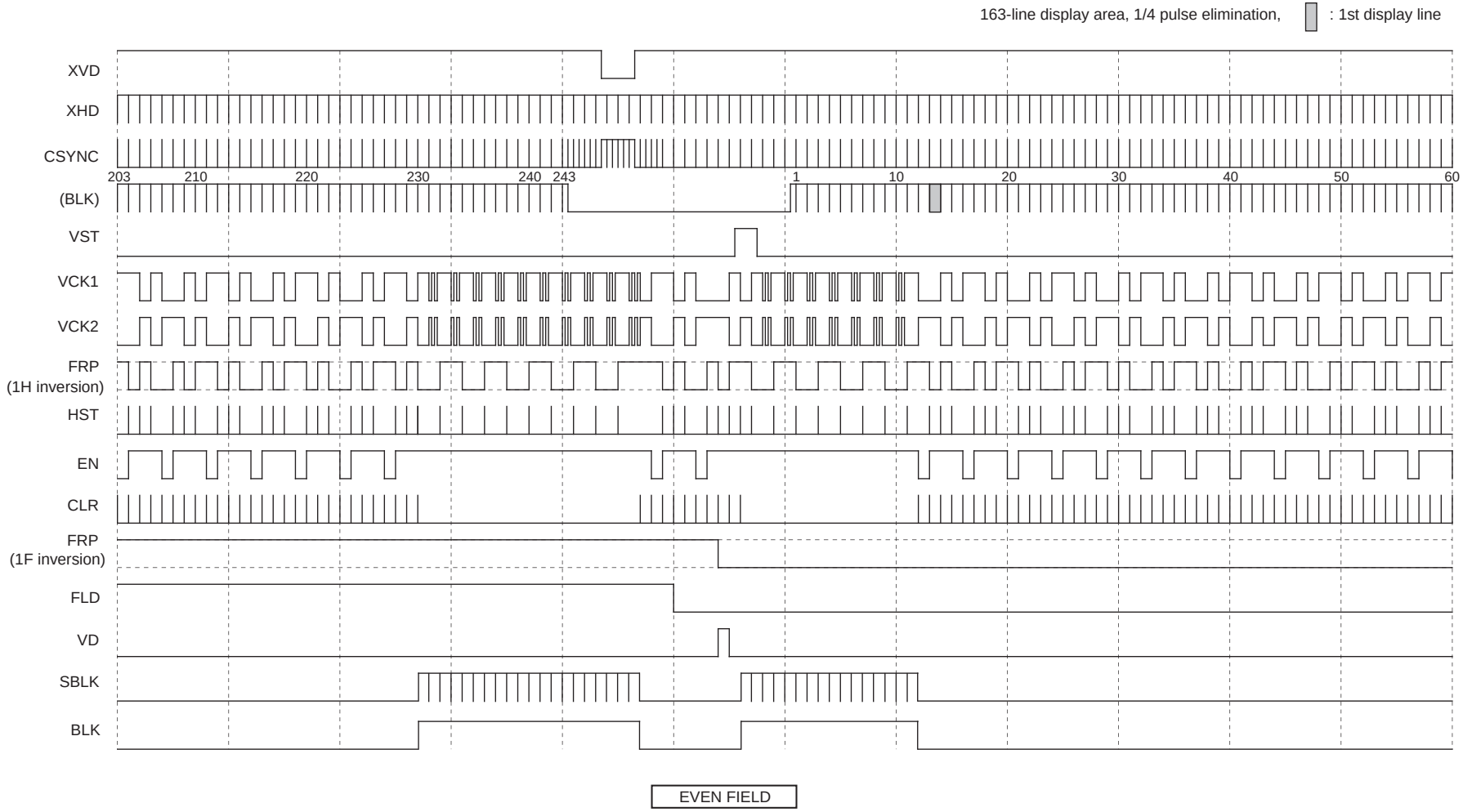
NTSC WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

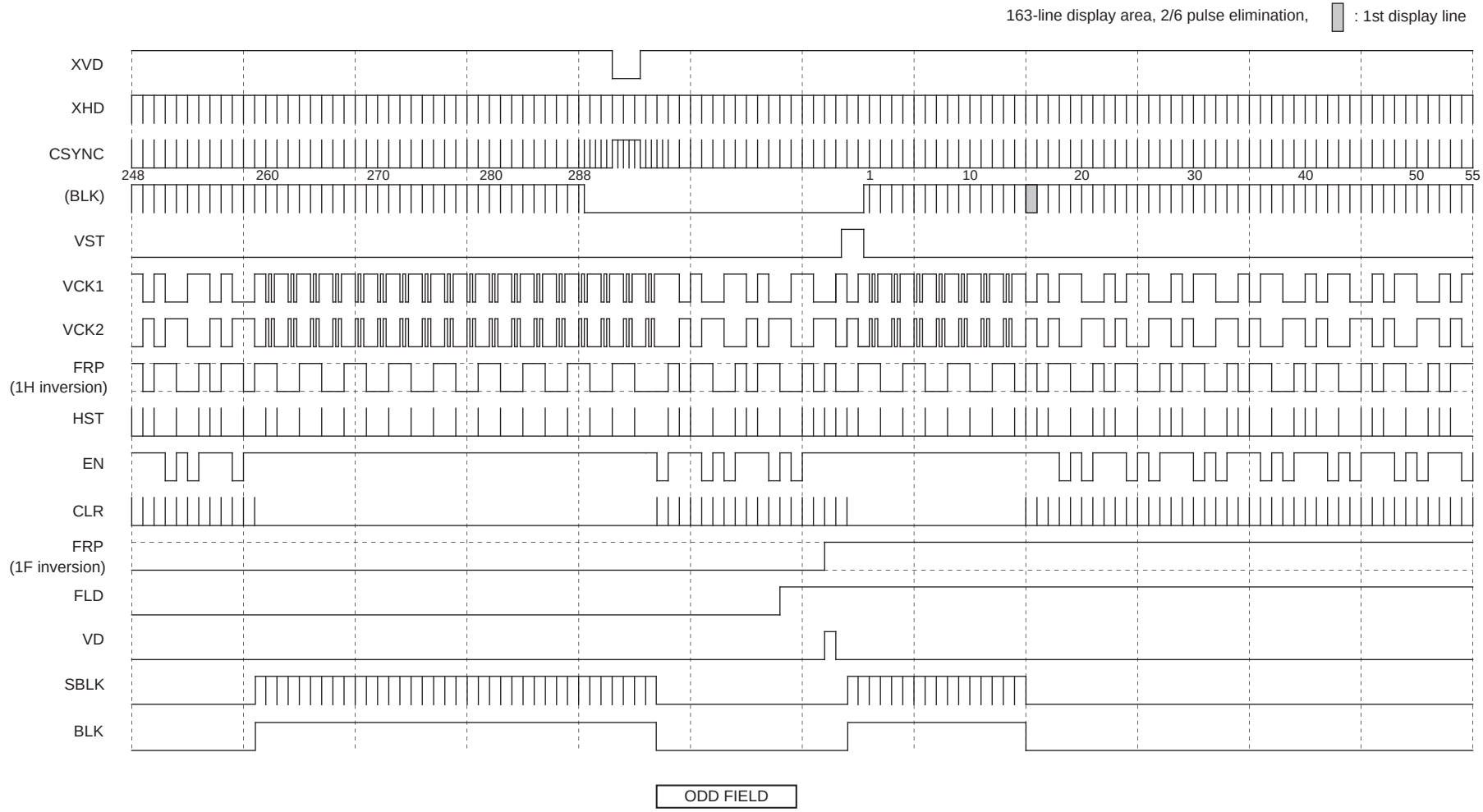
NTSC WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

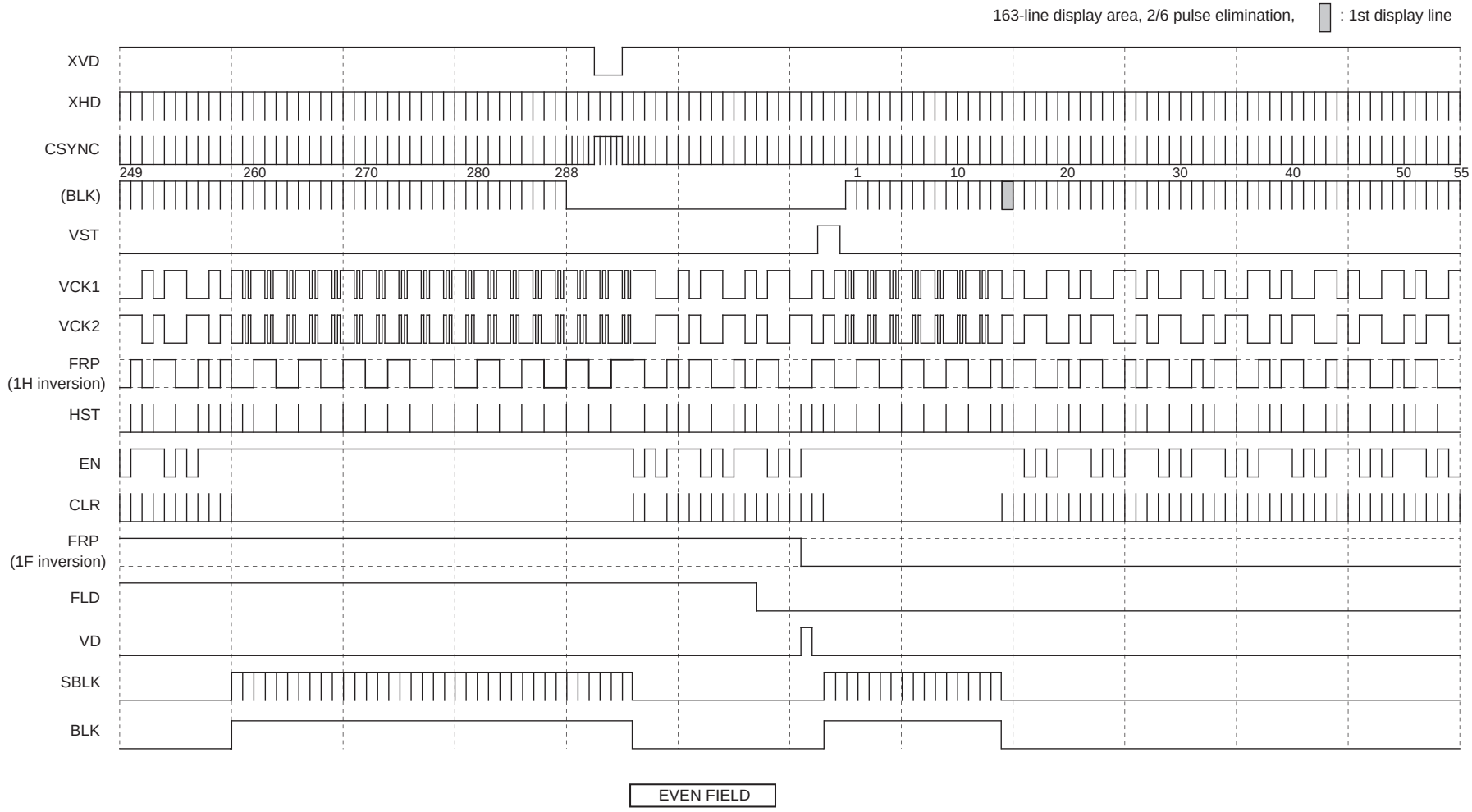
PAL WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

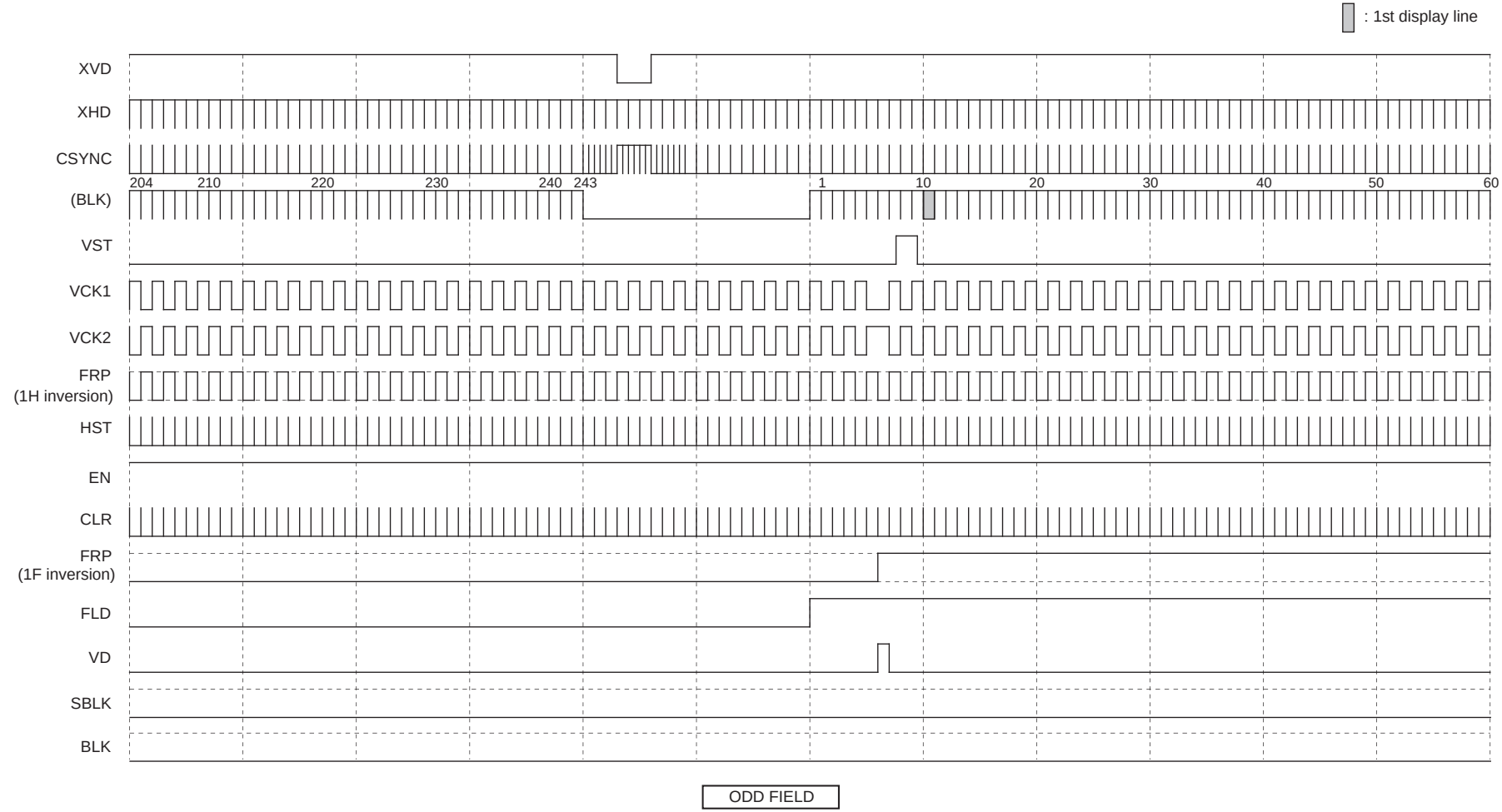
PAL WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX024AK Vertical Direction Timing Chart

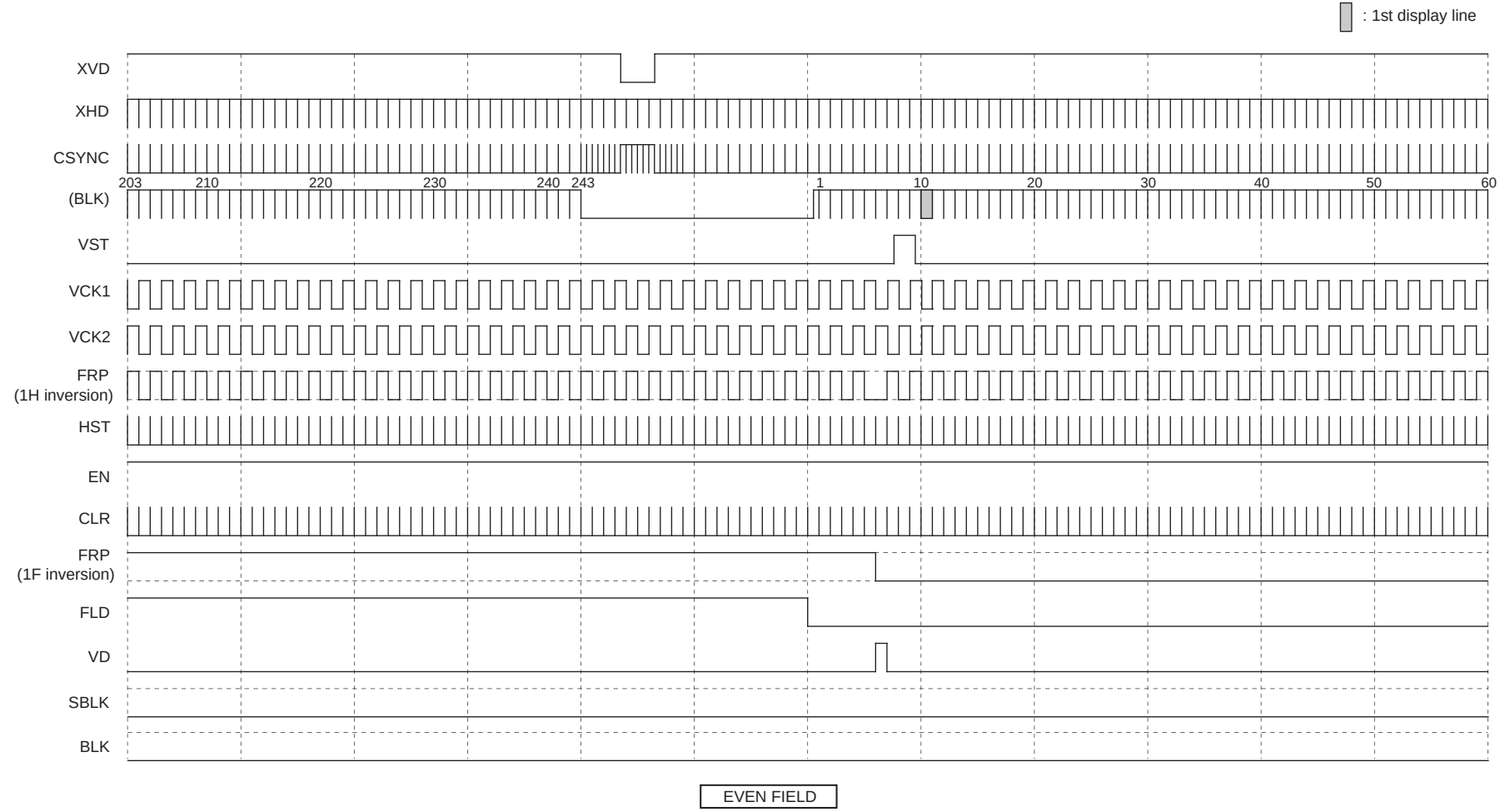
NTSC



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX024AK Vertical Direction Timing Chart

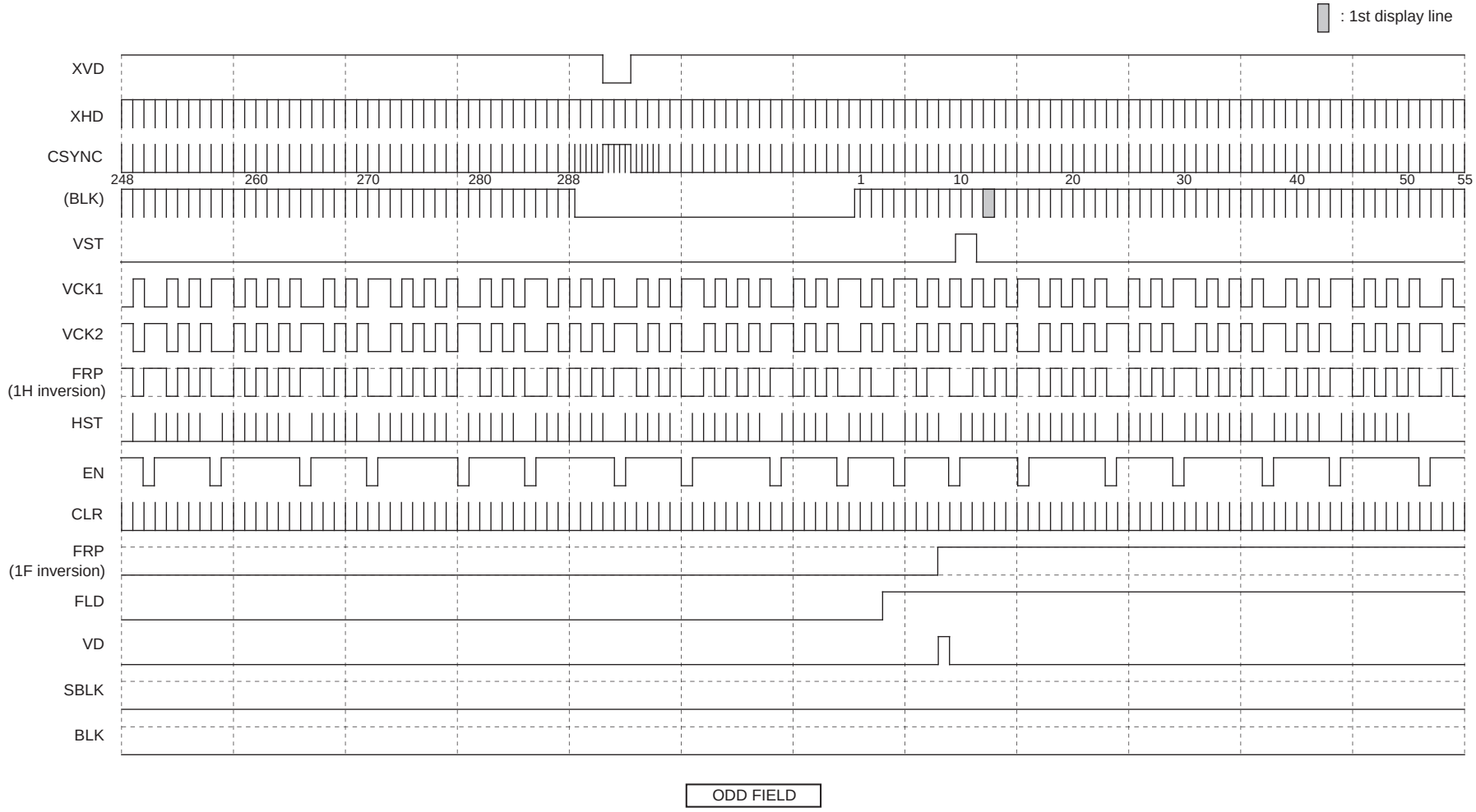
NTSC



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX024AK Vertical Direction Timing Chart

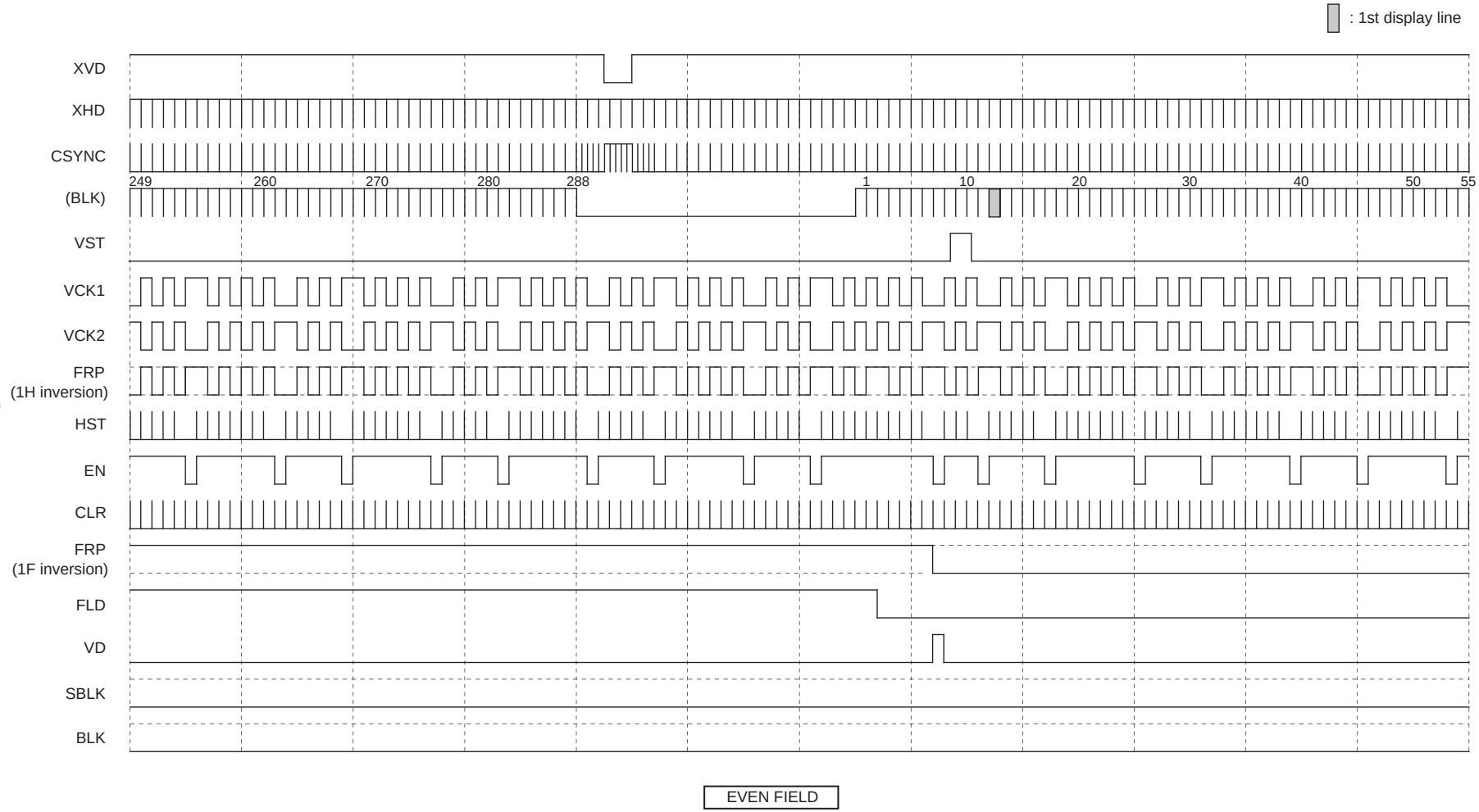
PAL



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX024AK Vertical Direction Timing Chart

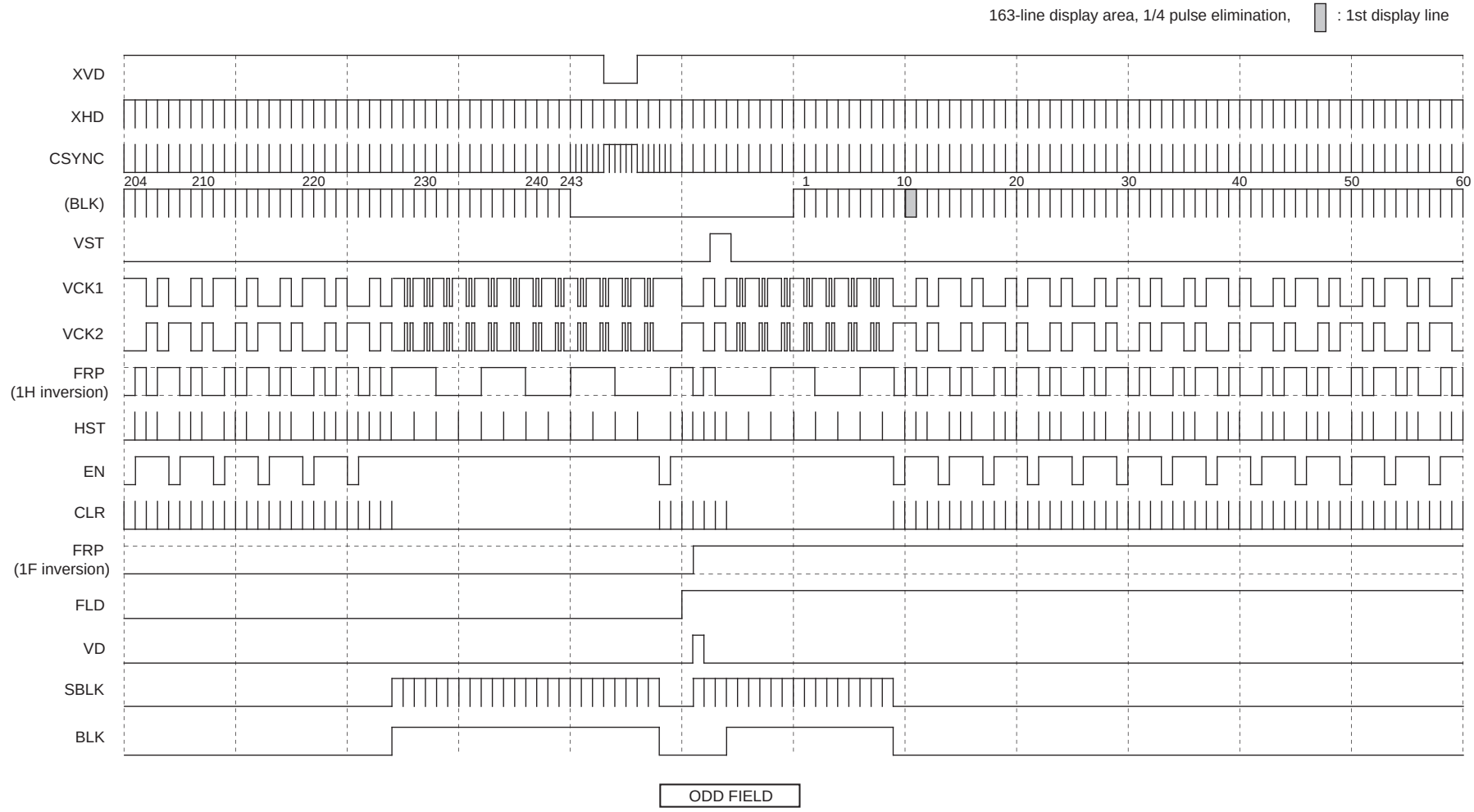
PAL



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX024AK Vertical Direction Timing Chart

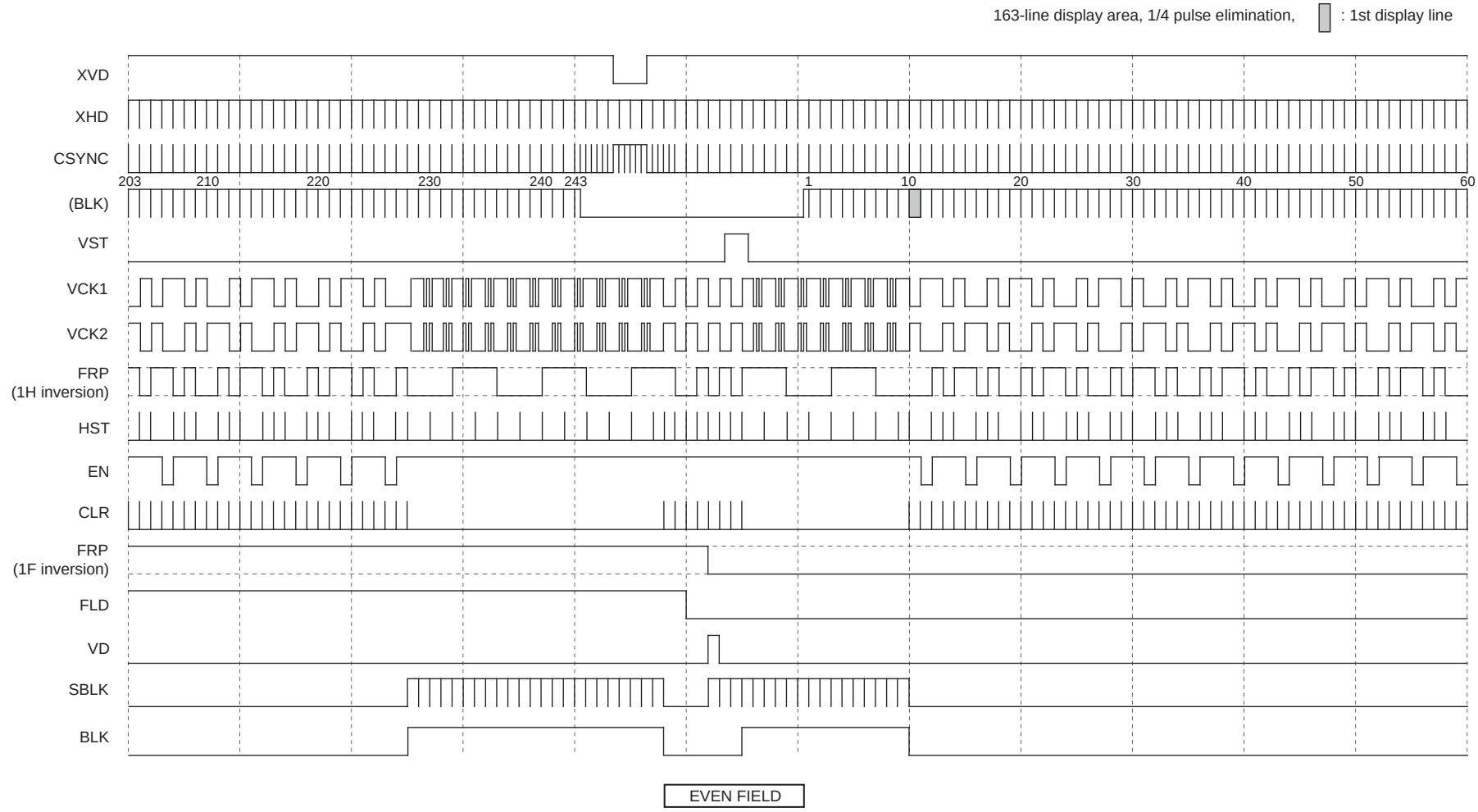
NTSC WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX024AK Vertical Direction Timing Chart

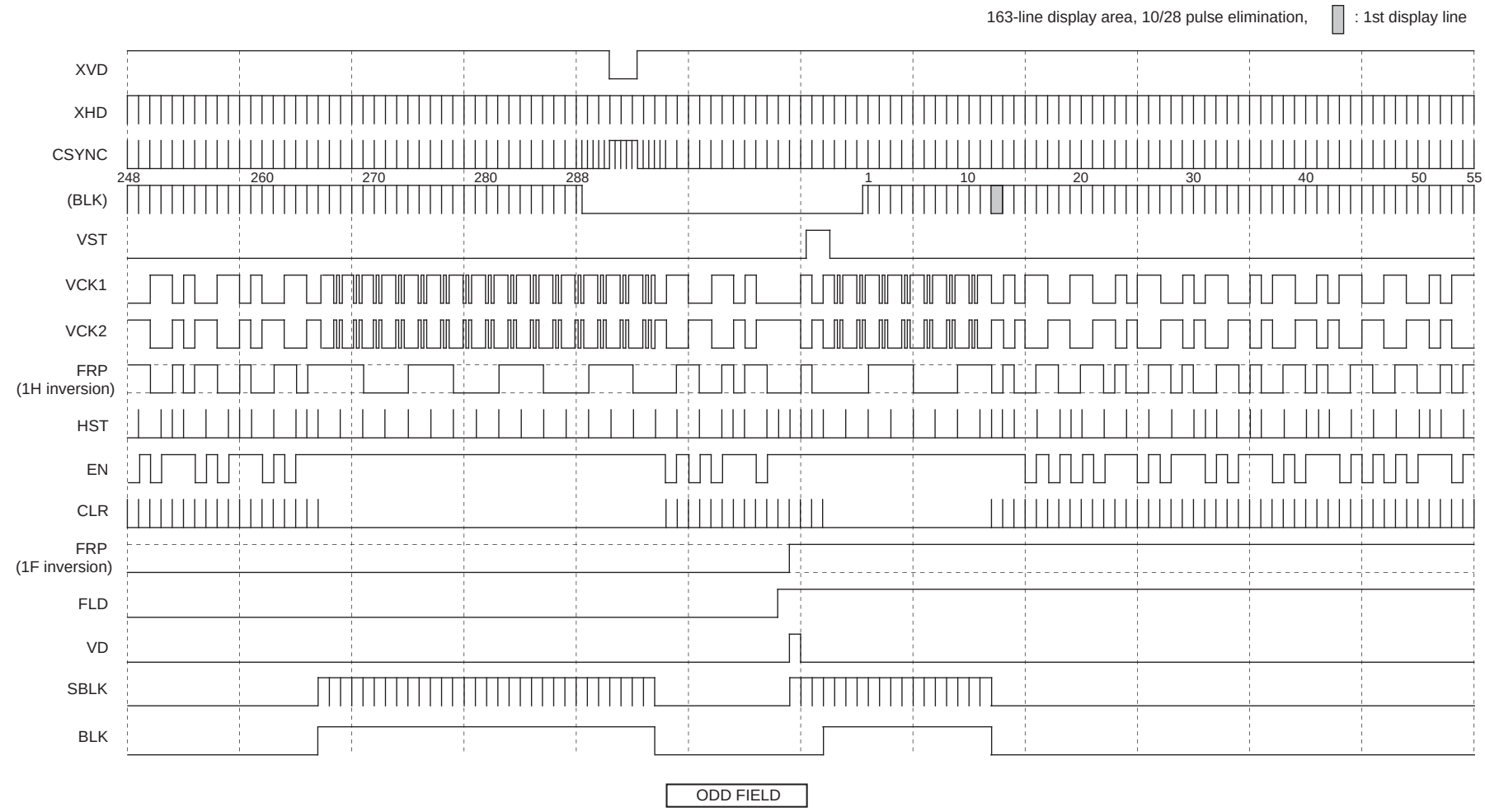
NTSC WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX024AK Vertical Direction Timing Chart

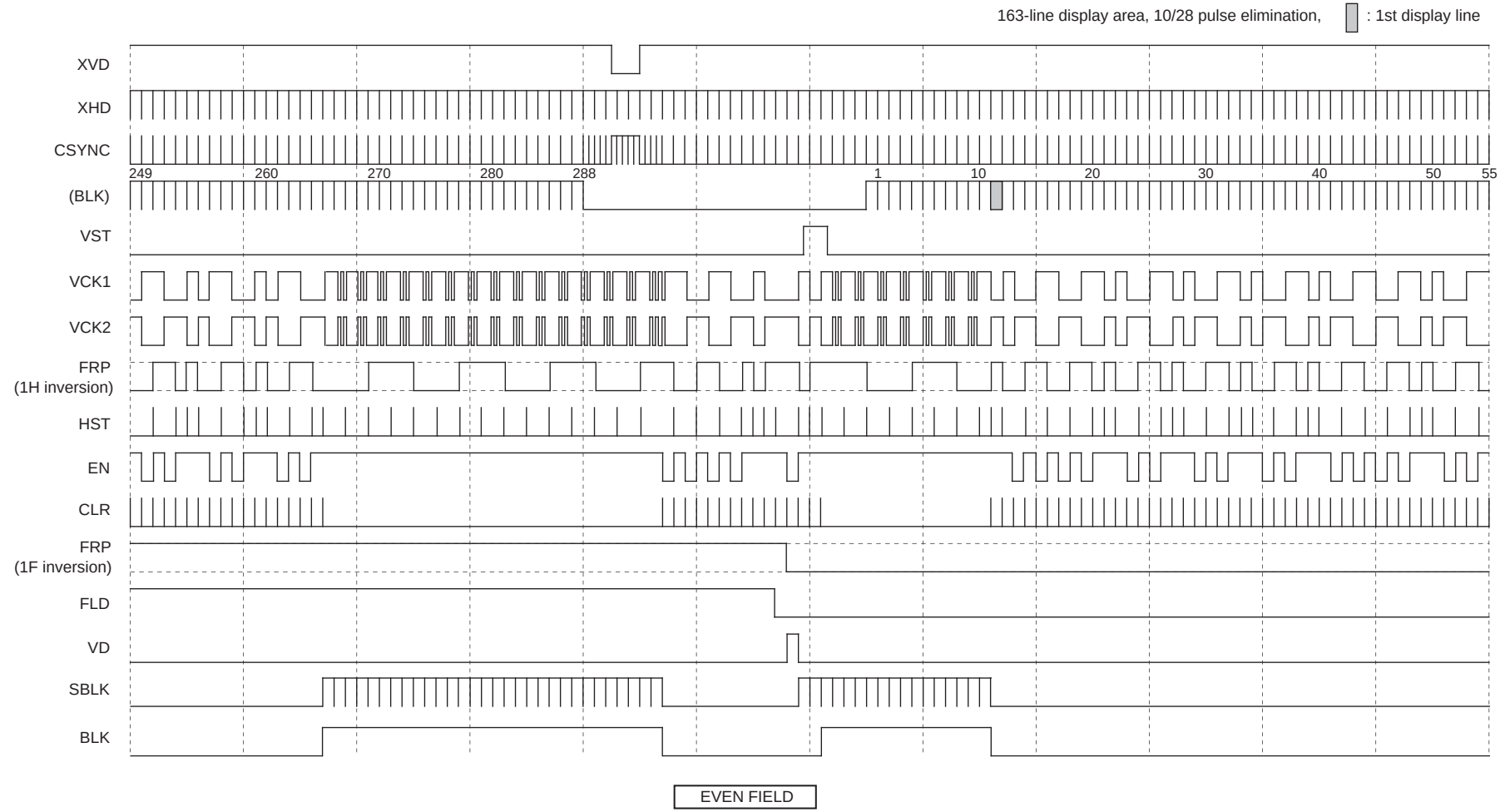
PAL WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX024AK Vertical Direction Timing Chart

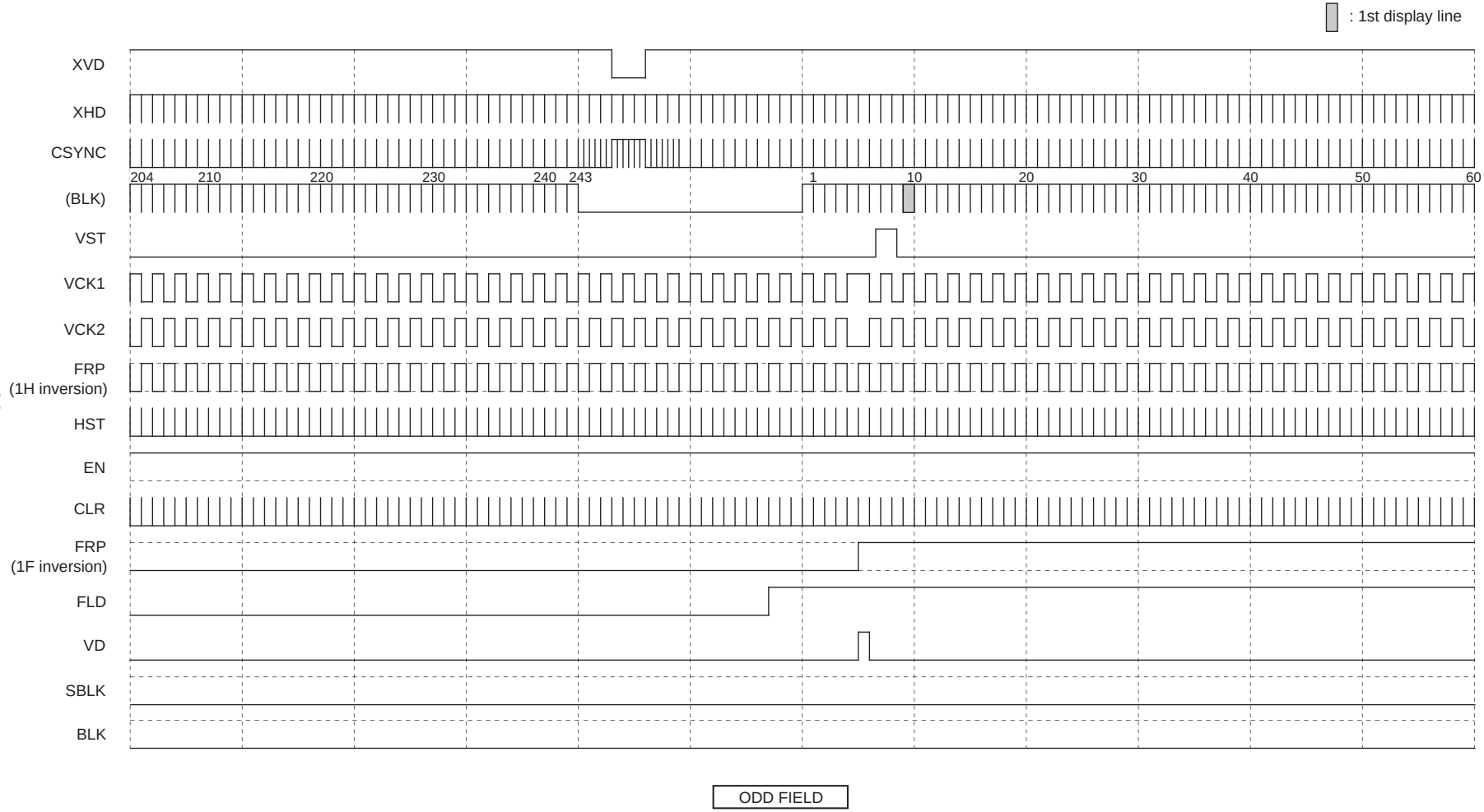
PAL WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

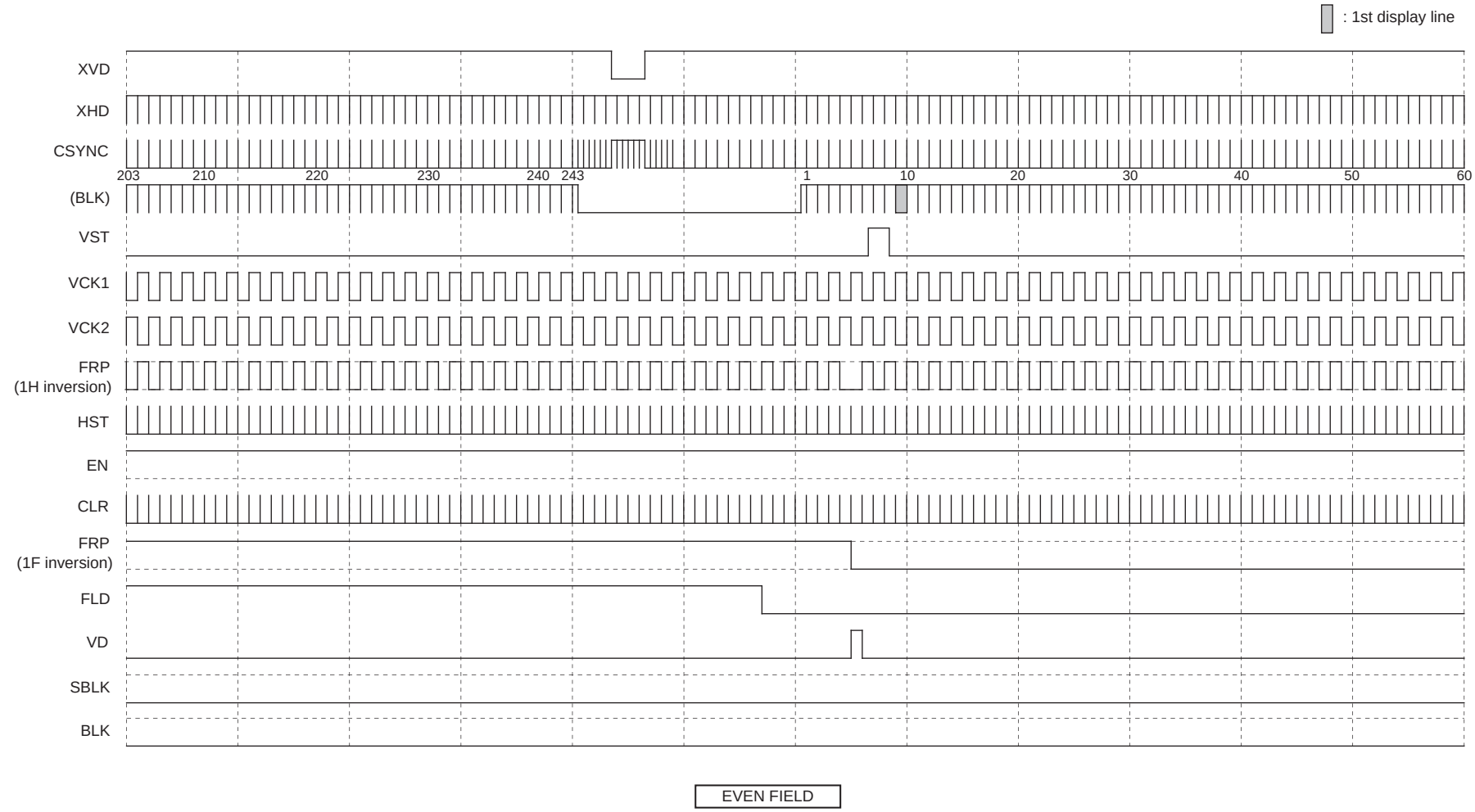
NTSC



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

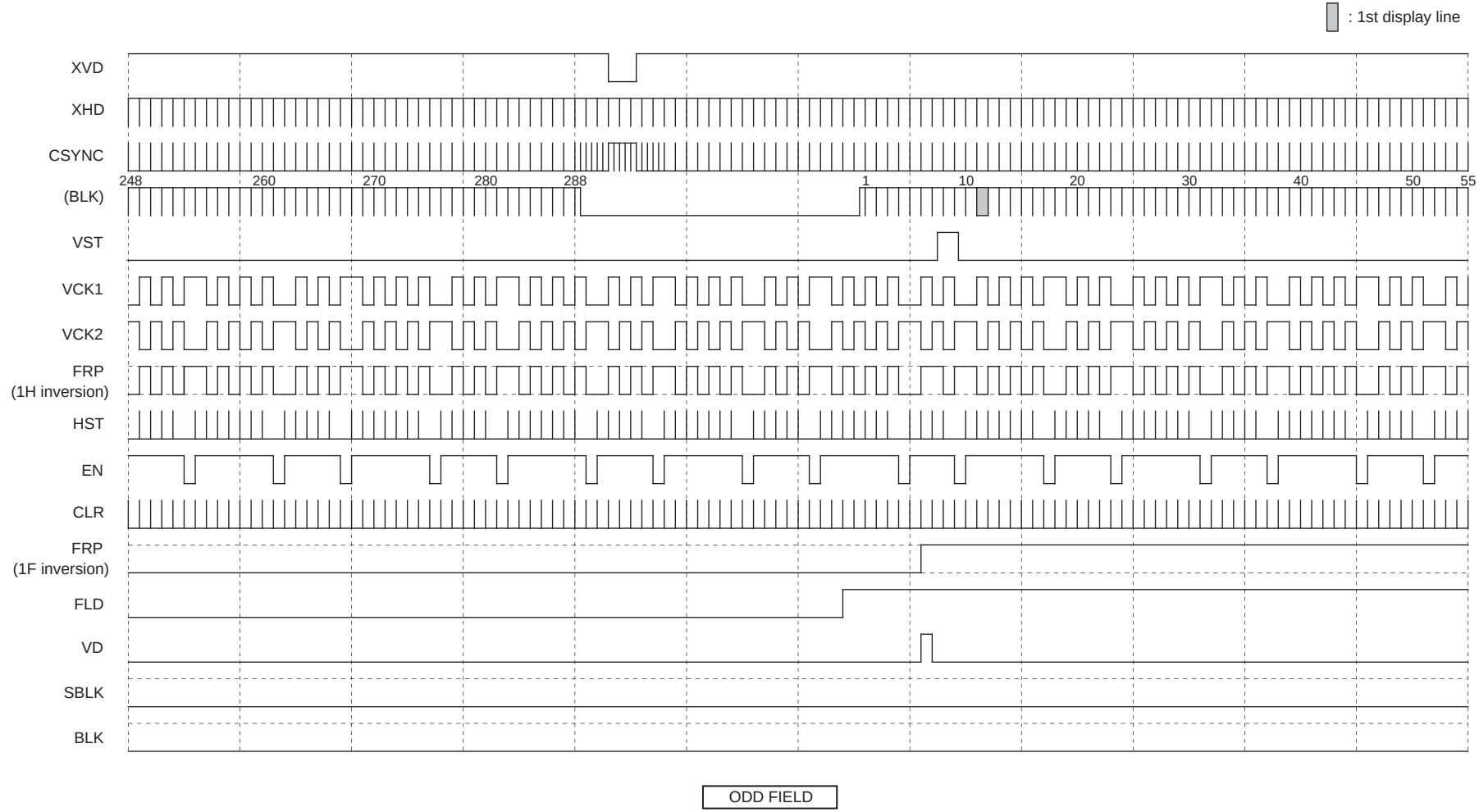
NTSC



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

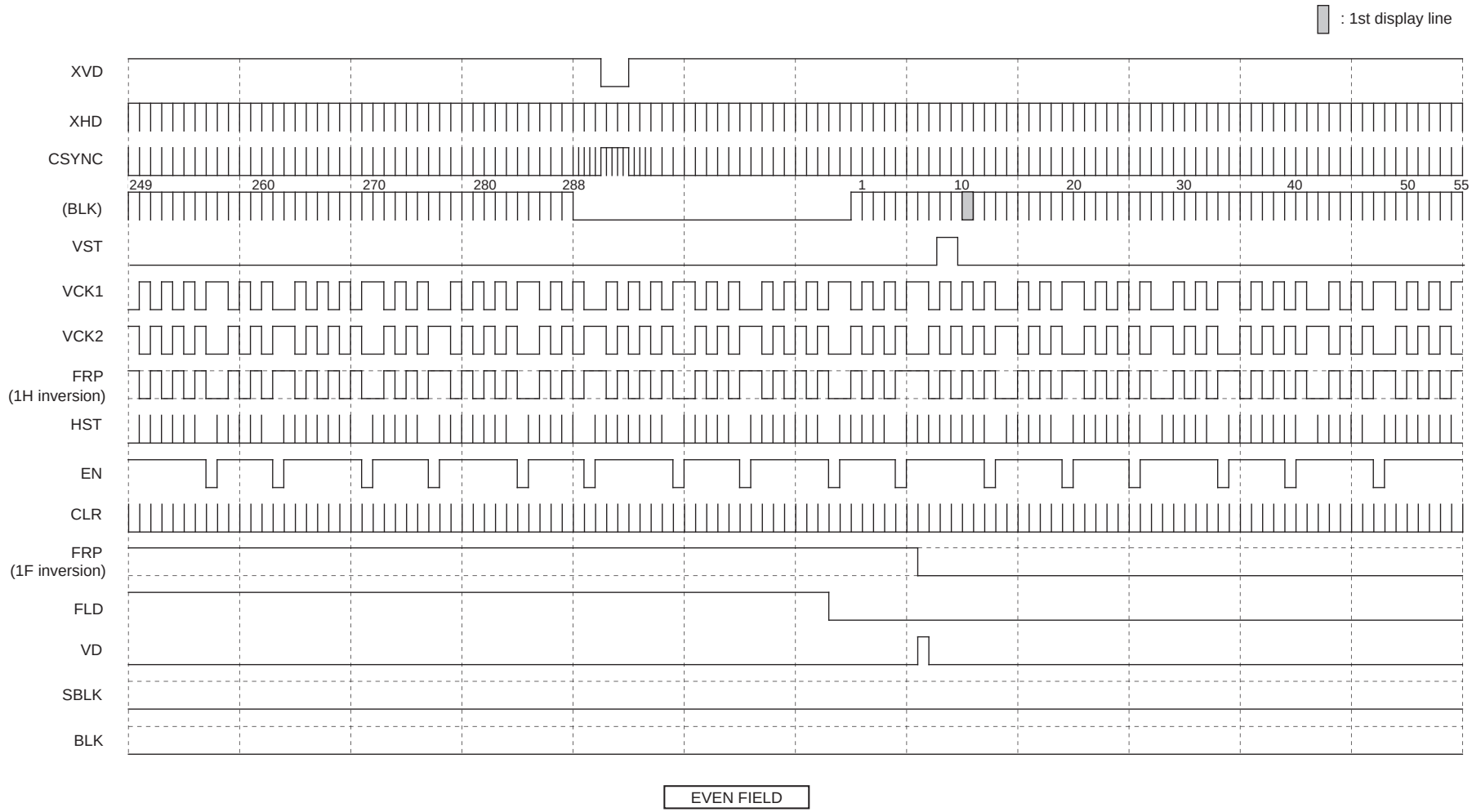
PAL



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

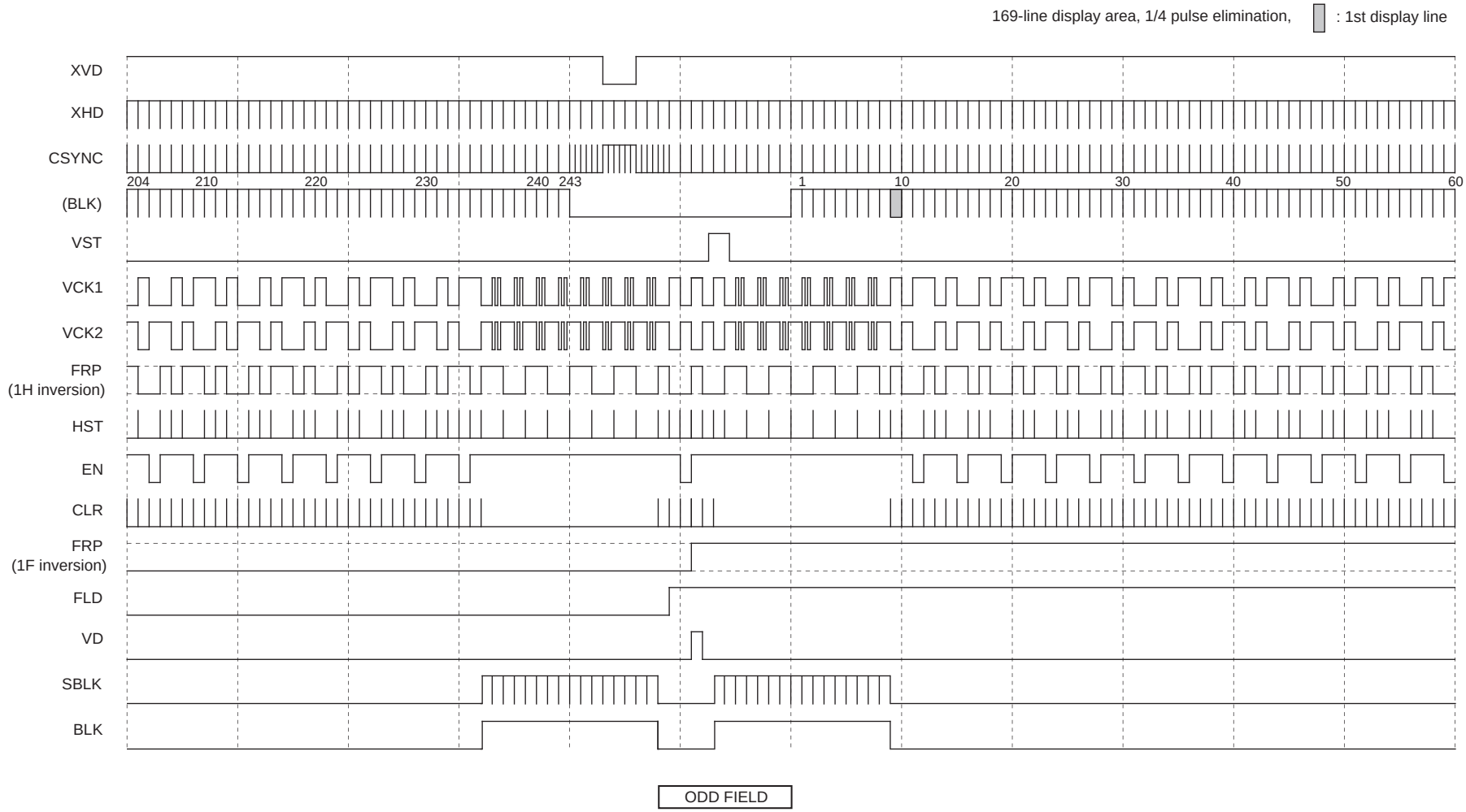
PAL



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

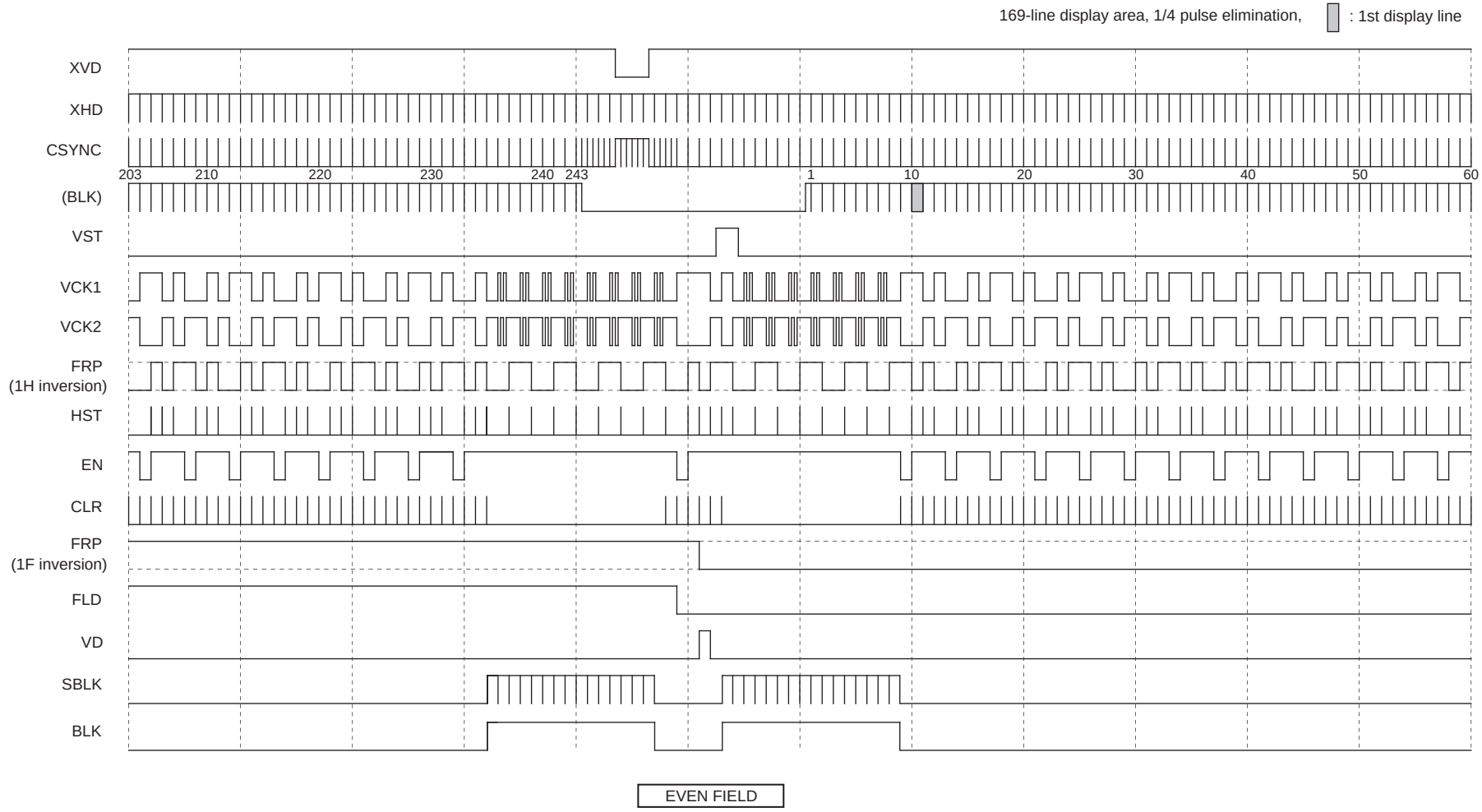
NTSC WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

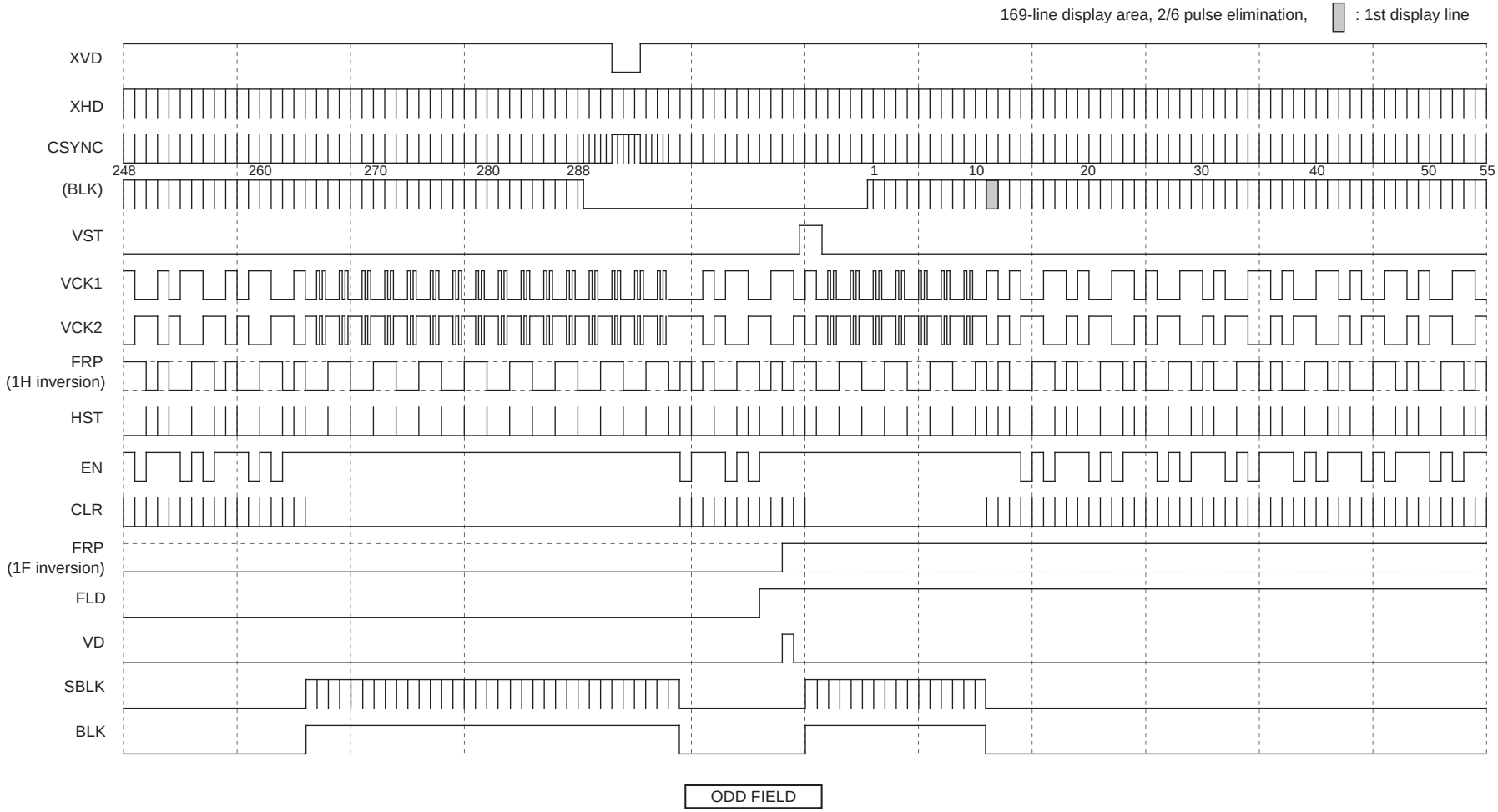
NTSC WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

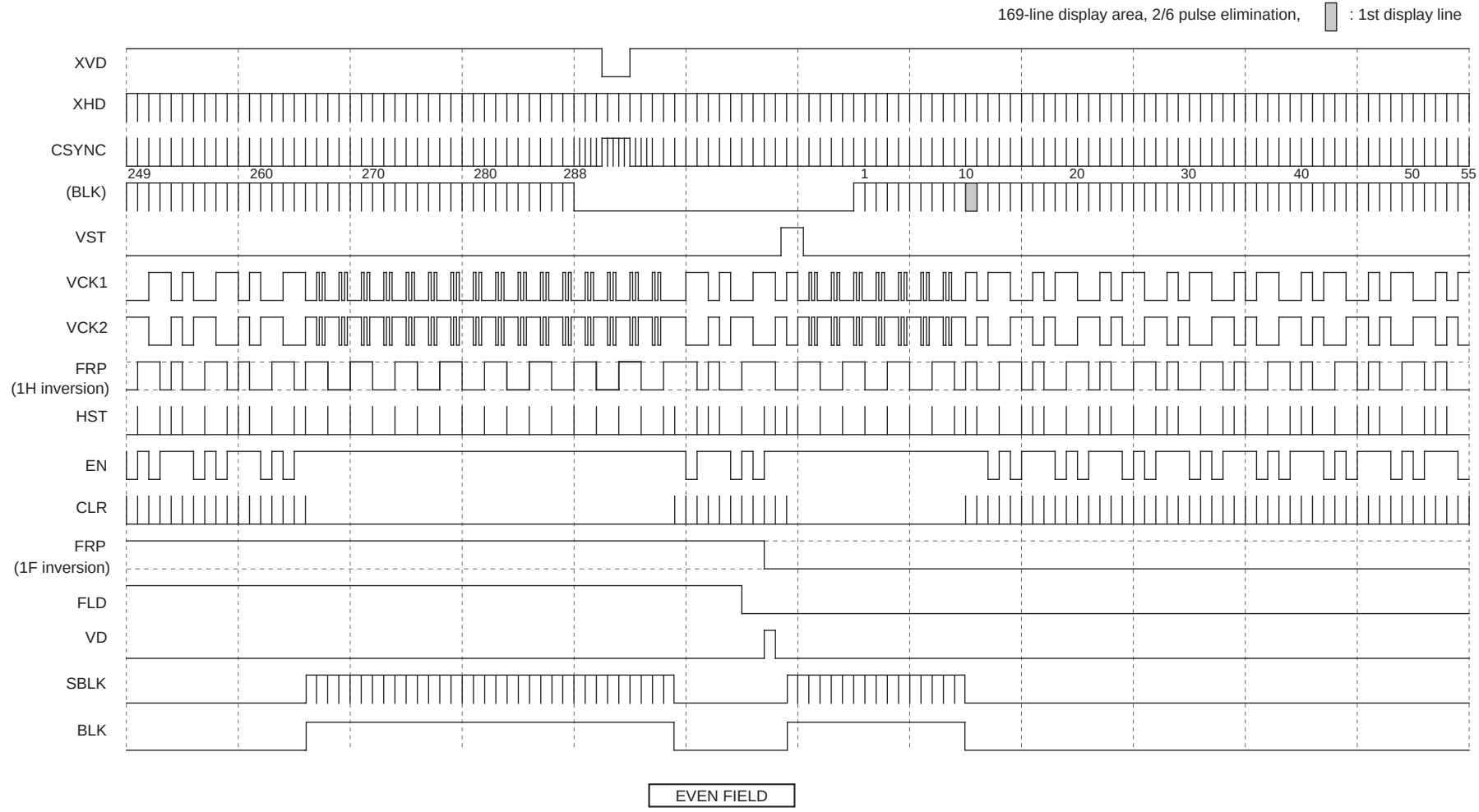
PAL WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

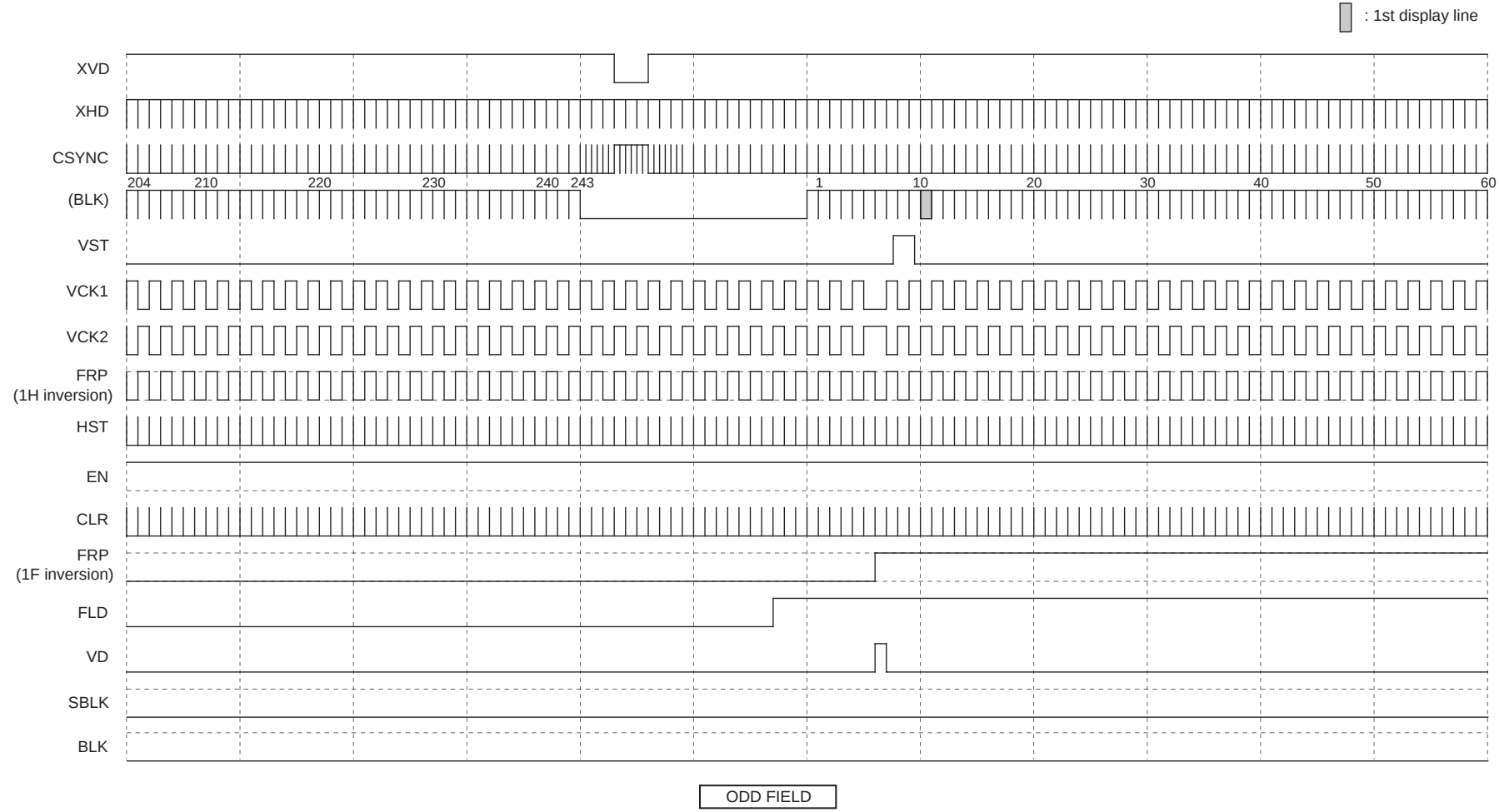
PAL WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX027AK Vertical Direction Timing Chart

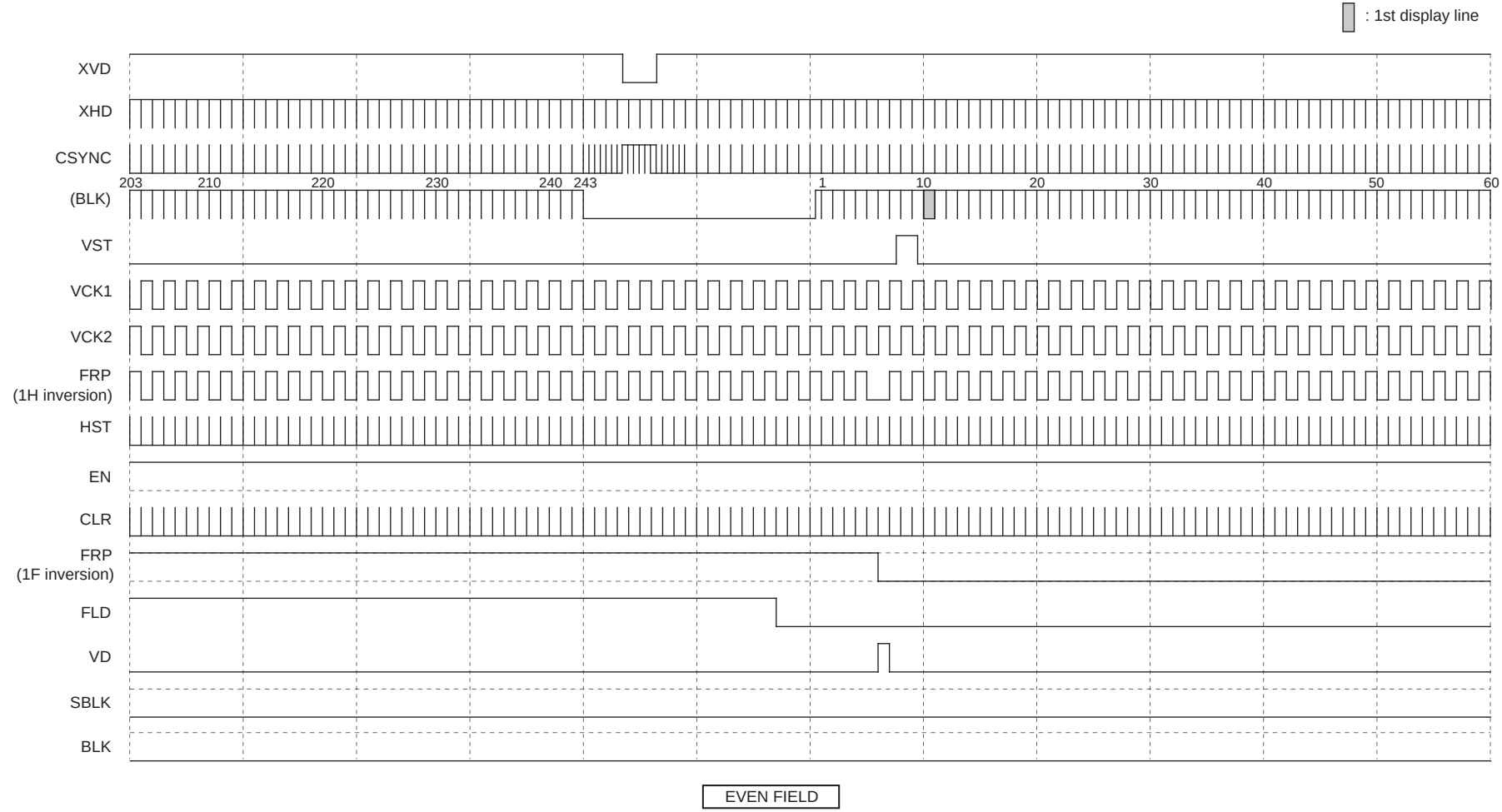
NTSC



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX027AK Vertical Direction Timing Chart

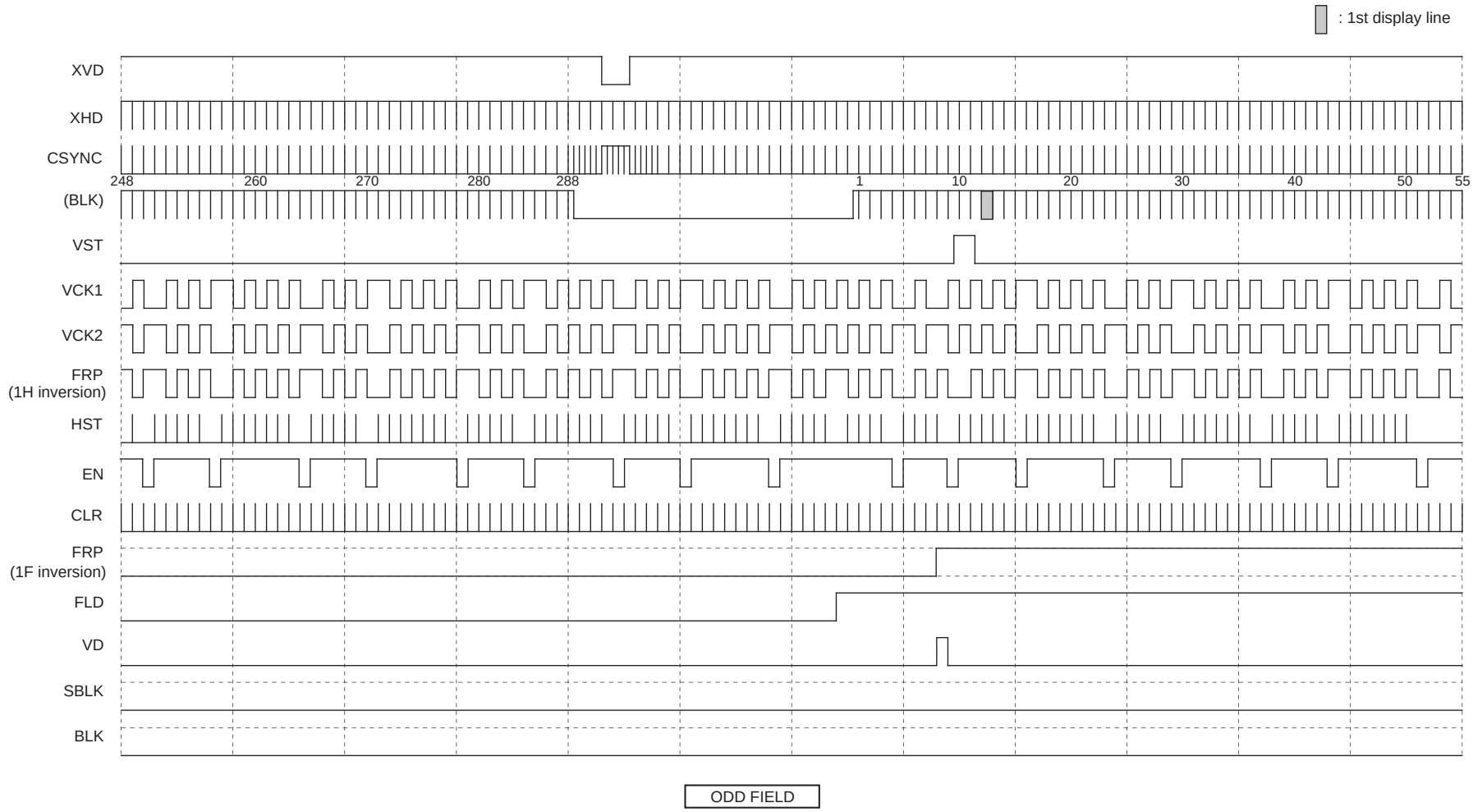
NTSC



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX027AK Vertical Direction Timing Chart

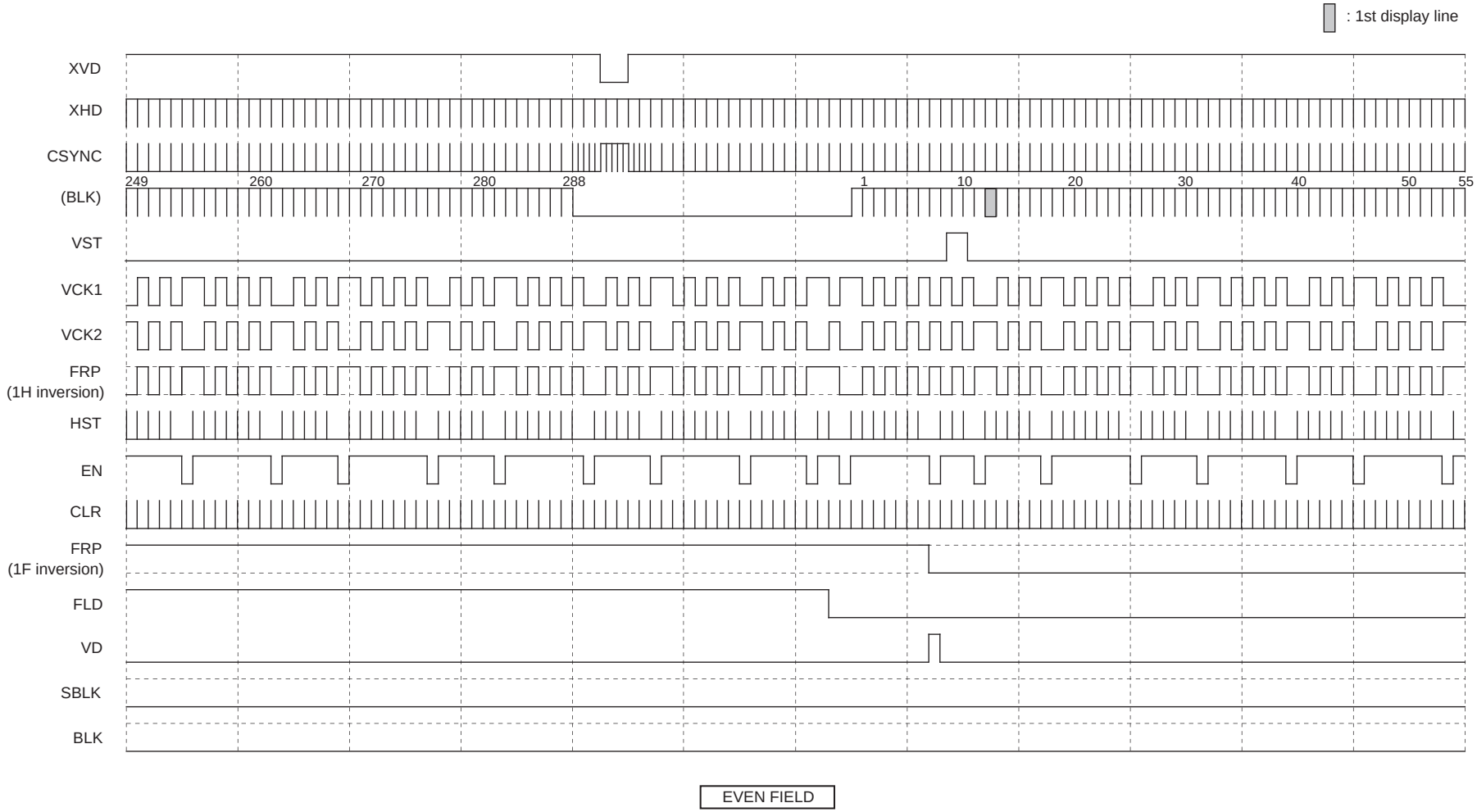
PAL



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX027AK Vertical Direction Timing Chart

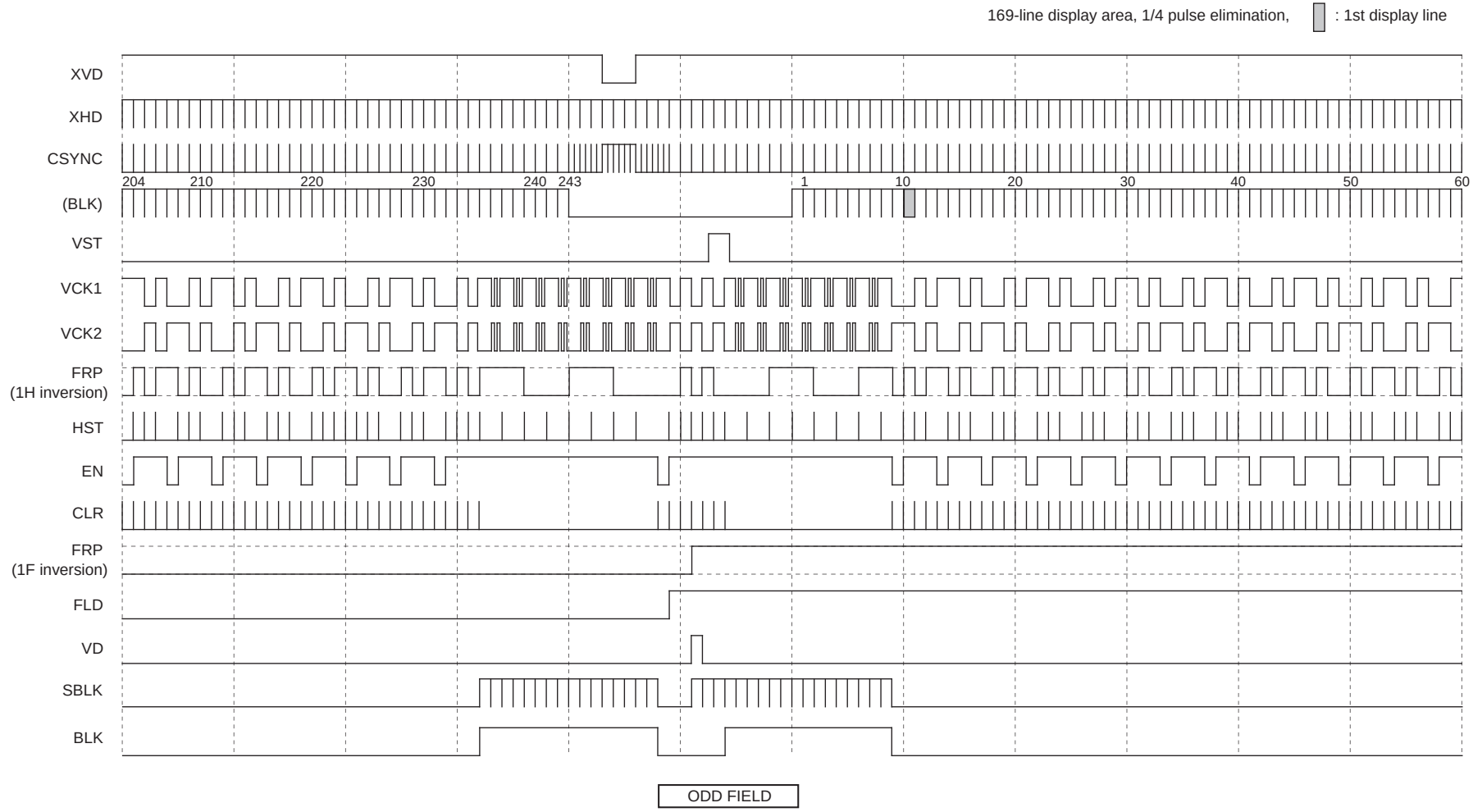
PAL



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX027AK Vertical Direction Timing Chart

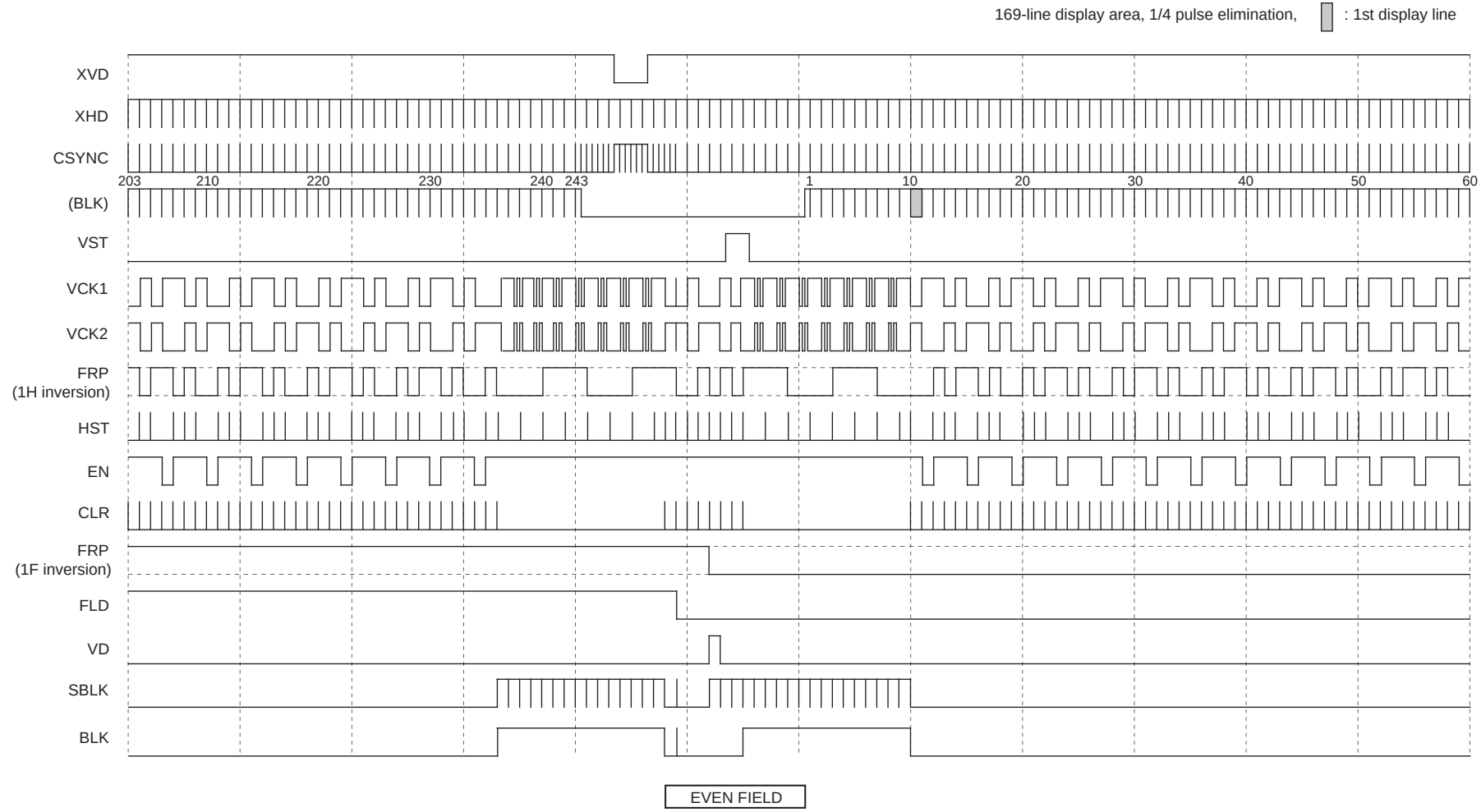
NTSC WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX027AK Vertical Direction Timing Chart

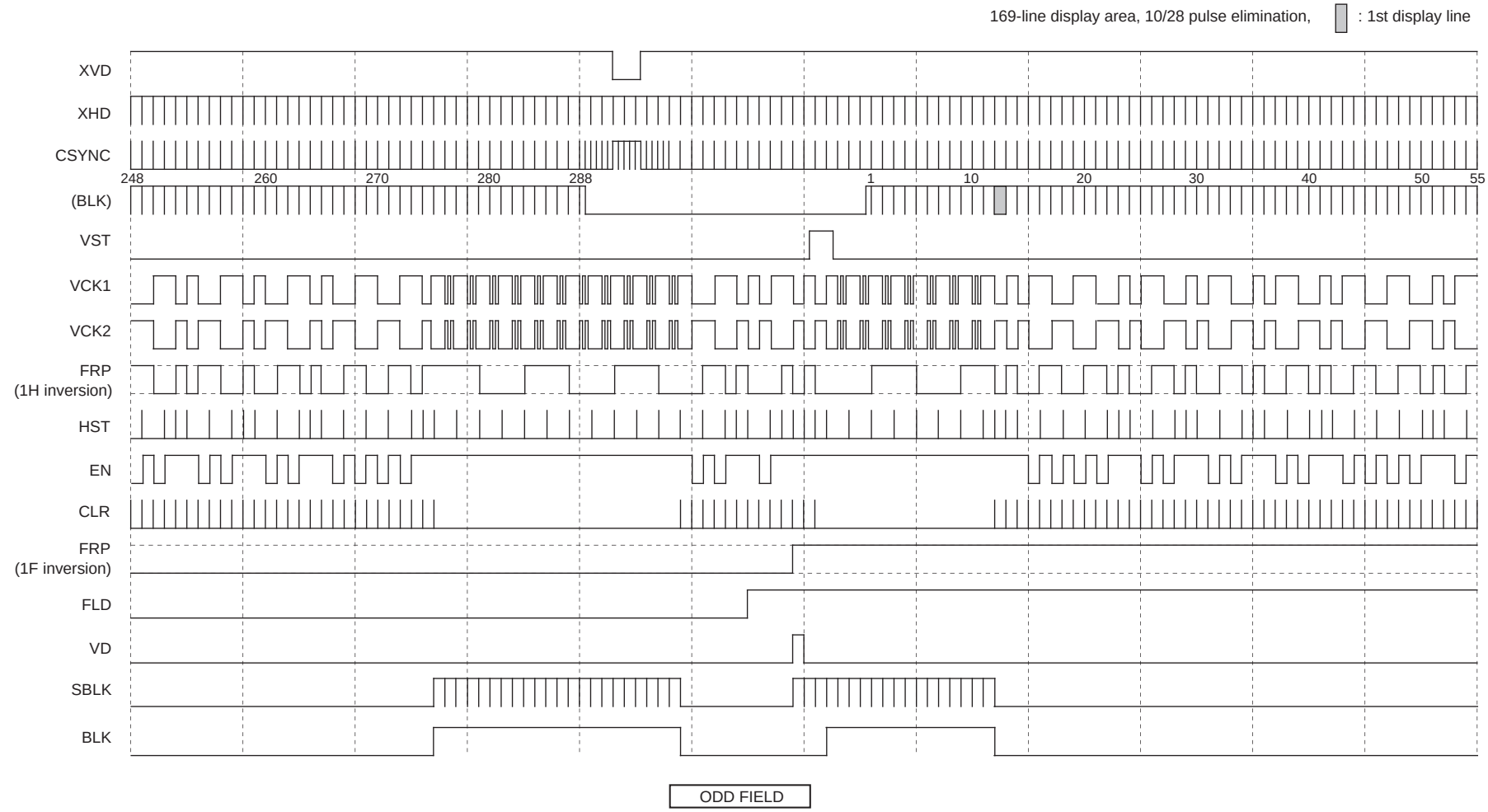
NTSC WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX027AK Vertical Direction Timing Chart

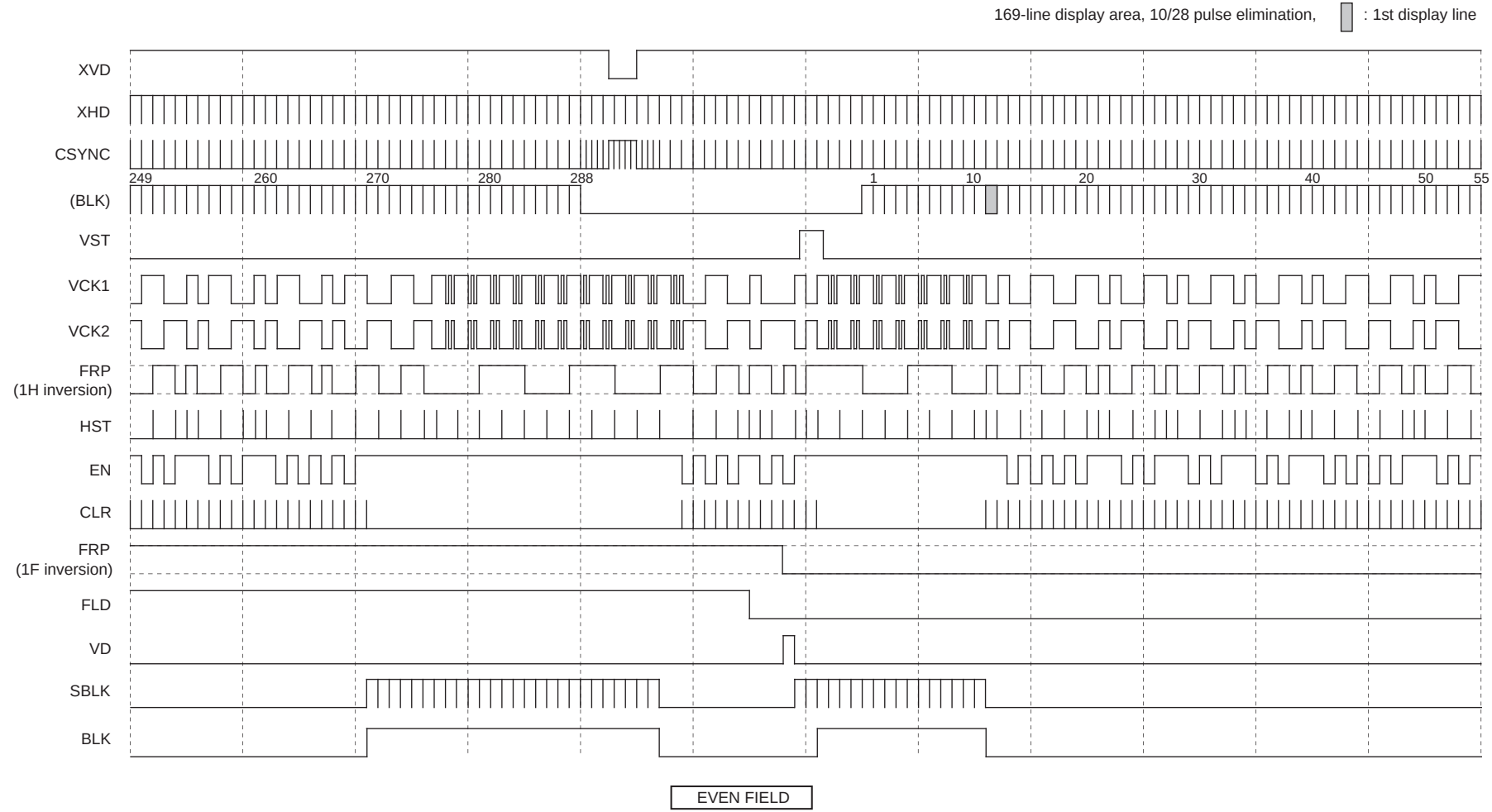
PAL WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

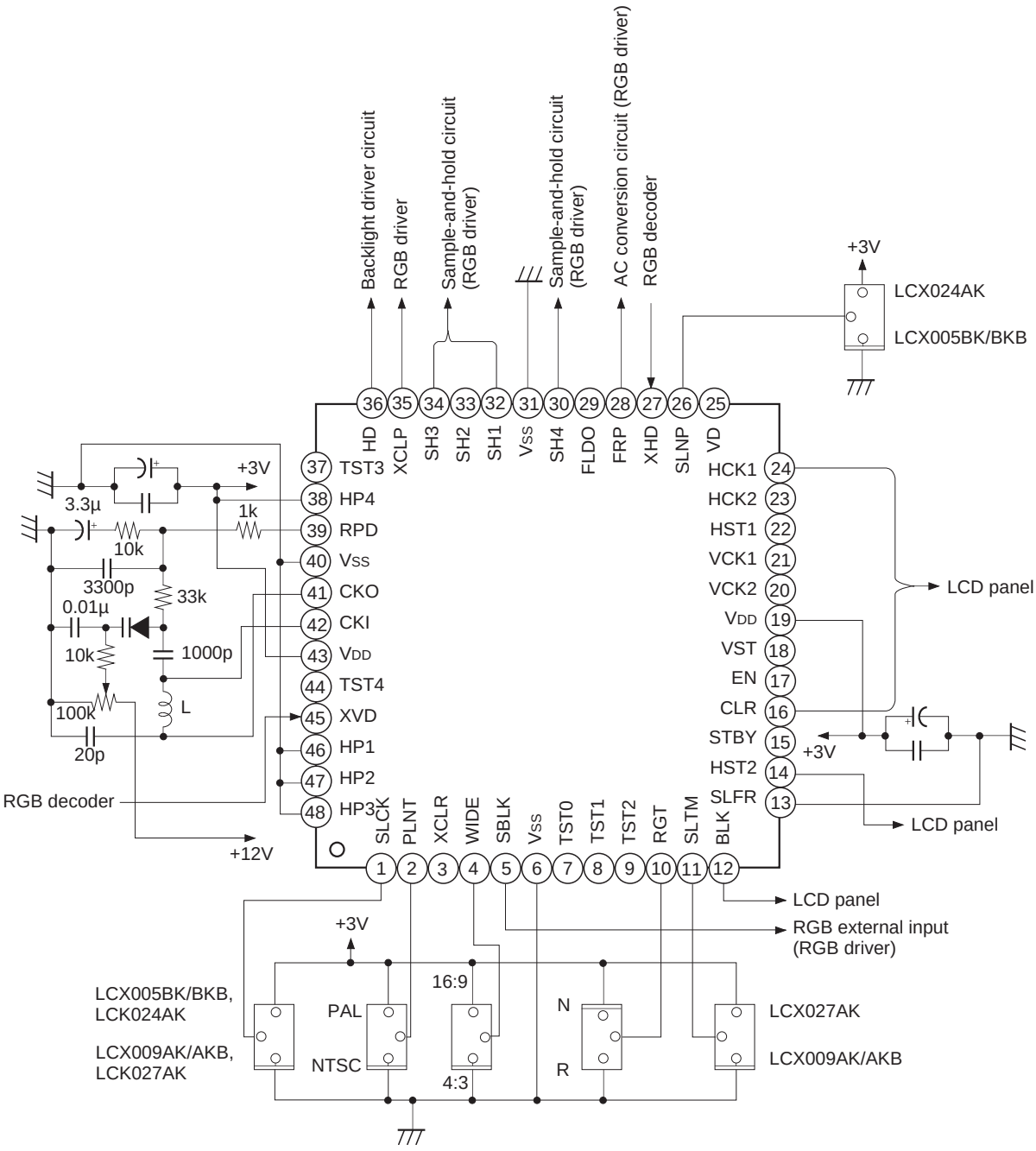
LCX027AK Vertical Direction Timing Chart

PAL WIDE



Note) The fourth row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

Application Circuit



Reference examples of L value: when using LCX009AK/AKB, LCX027AK 4.7µH
when using LCX005BK/BKB, LCX024AK 10µH

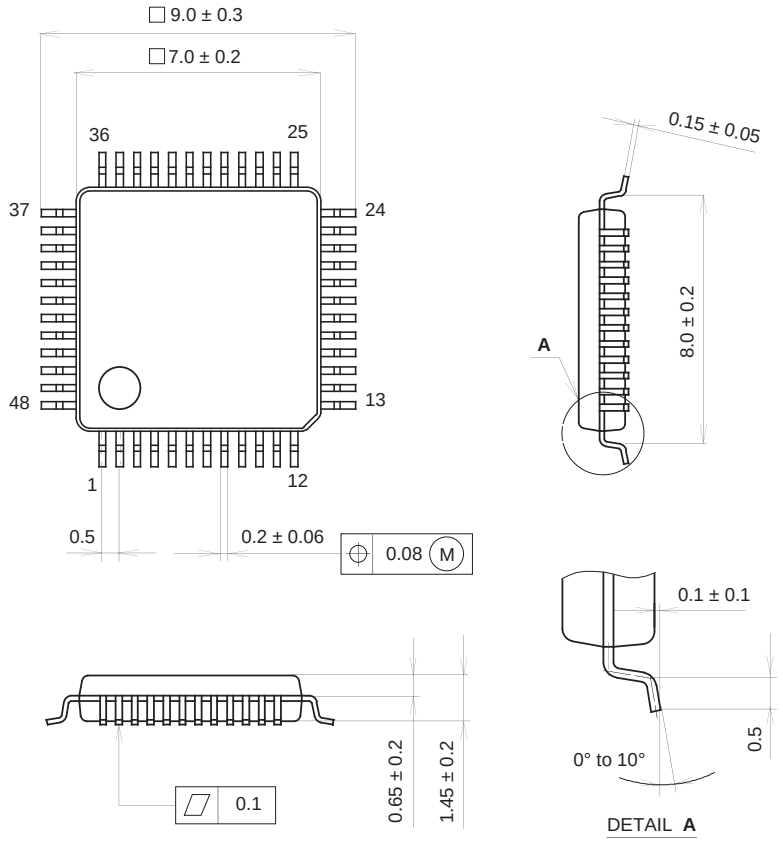
Recommended varicap: 1T369 (SONY)

The constants noted above are reference values, so care should be taken as they may change according to the wiring capacitance on the board, etc.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

48PIN LQFP (PLASTIC)



SONY CODE	LQFP-48P-L111
EIAJ CODE	LQFP048-P-0707-AP
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.2g