M52026SP

SECAM CHROMA SIGNAL PROCESSOR

DESCRIPTION

The M52026SP is a semiconductor integrated circuit for processing color signals for SECAM color television sets. This IC consists of a limiter amplifier, color signal demodulator, IDENT detector, SECAM switch, system discriminator, system switch, color saturation control, matrix, AM modulator, local oscillator and DC regenerating circuit.

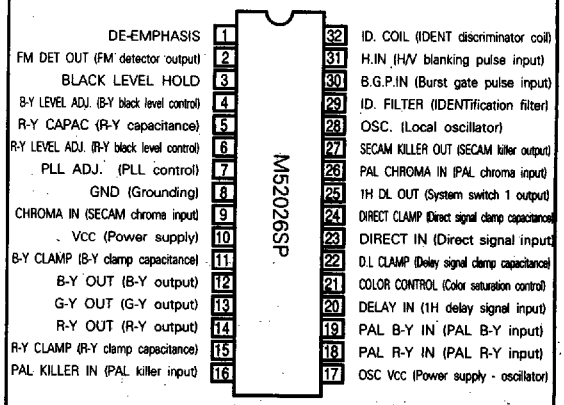
FEATURES

- Reduced crosstalk
- Small number of external components
- Superior linearity of color signal detector
- Few PAL/SECAM system switching errors
- Wide range of operating supply voltage

APPLICATION

SECAM system color TV

PIN CONFIGURATION (TOP VIEW)

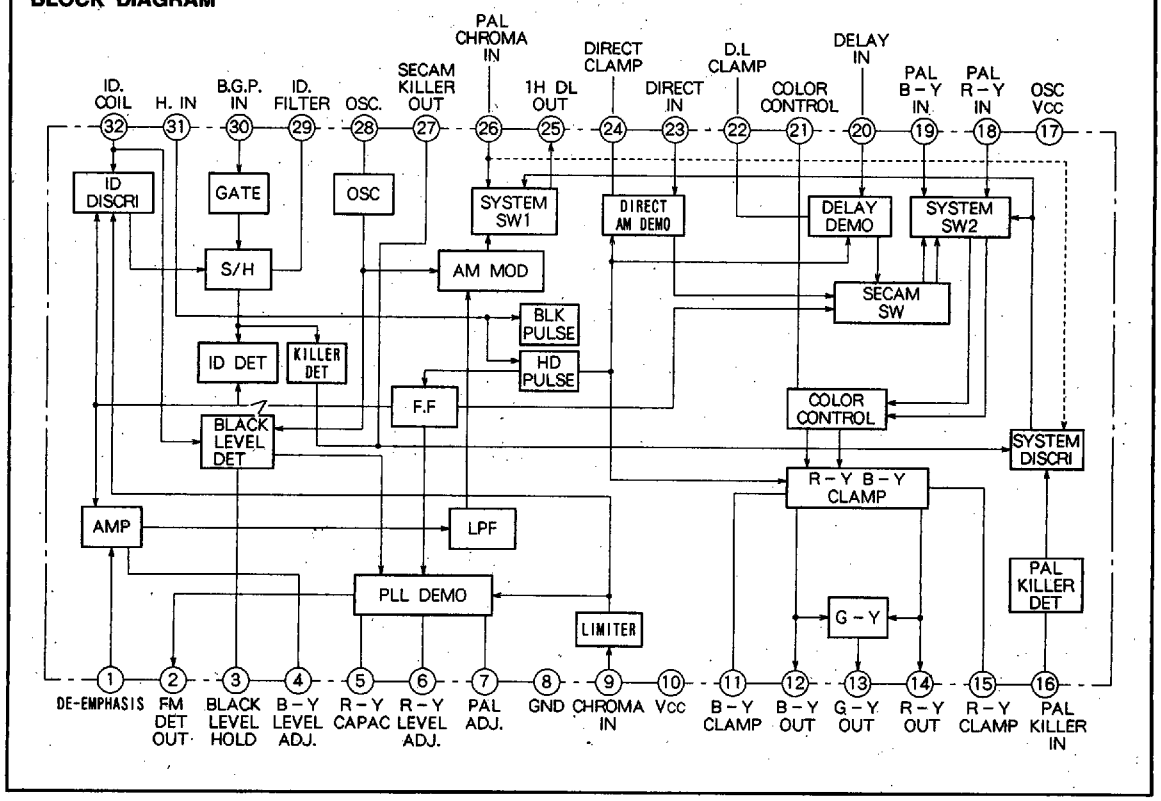


Outline 32P4B

RECOMMENDED OPERATING CONDITION

Supply Voltage Range ..... 8.5~13V
Rated Supply Voltage 11V

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	13.5	V
P_d	Internal power dissipation	1.25	W
Vsurge	Electrostatic discharge	± 200	V
K_θ	Thermal derating	10	mV/℃
Vlatch	Latch – up voltage	± 300	V
T_{opr}	Operating temperature	– 20~65	℃
T_{stg}	Storage temperature	– 40~125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test point	Input	Test conditions															Limits			Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	Note	Min.	Typ.	Max.	
I_{CC1}	Circuit current I	A1	–	1	2	2	1	2	2	1	2	2	3	4	1	1	1		45	60	75	mA
I_{CC2}	Circuit current II	A2	–	1	2	2	1	2	2	1	2	2	3	4	1	1	1		18	24	30	mA
V_{O32}	ID discriminator output amplitude	32	C IN SG1 100mVP-P	1	2	2	1	2	2	1	2	2	3	4	1	1	1		119	170	225	mVP-P
V_{LIM} (Note1)	Limiting sensitivity	32	C IN SG1 – 3dB	1	2	2	1	2	2	1	2	2	3	4	1	1	1	1	22	26	30	dB
I/K (Note2)	IDENT killer characteristics	1	C IN SG0 variable	1	2	2	1	2	2	1	2	2	3	4	1	1	1	2	29	39	49	dB
$V_{O\ (K)}$	Killer color residual	12 13 14	C IN SG0 100mVP-P	1	2	2	1	2	2	1	3	3	3	4	1	1	1		–	6.0	20	mVP-P
V_{1R}	FM demodulator output amplitude R – Y, B – Y	1	C IN SG0 100mVP-P	1	2	2	1	2	2	1	2	2	3	4	1	1	1		310	390	468	mVP-P
V_{1B}																			256	320	384	mVP-P
V_{1R} / V_{1B}	FM demodulator relative amplitude	1	C IN SG0 100mVP-P	1	2	2	1	2	2	1	2	2	3	4	1	1	1		1.1	1.2	1.3	–
V_{1LIN} (Note3)	FM demodulator output linearity	1	C IN SG0 100mVP-P	1	2	2	1	2	2	1	2	2	3	4	1	1	1	3	2.6	3.0	3.4	–
V_{1CL} (Note4)	FM demodulator output carrier leak	1	C IN SG1 100mVP-P	1	2	2	1	2	2	1	2	2	3	4	1	1	1	4	–	– 34	– 28	dB
$V_{IB\ \theta}$	FM demodulator output temperature dependency	1	C IN SG0 100mVP-P	1	2	2	1	2	2	1	2	2	3	4	1	1	1		– 1	0	+ 1	mV/℃
$V_{OBH\ \theta}$	FM demodulator output black – level temperature dependency	1	C IN SG0 100mVP-P	1	2	2	1	2	2	1	2	2	3	4	1	1	1		–	+ 2	–	mV/℃
V_{OBH} (Note5)	B – Y to black – level voltage	12	C IN SG0 100mVP-P	1	2	2	1	2	2	1	2	2	3	4	1	2	1	5	– 150	0	+ 150	mV
Δ V_{OH}	Final output 1H step difference	12 13 14	C IN SG2 100mVP-P	1	2	2	1	2	2	1	2	2	3	4	1	1	1		0	4	20	mV
AMR (Note6)	AMR	7A	C IN SG2 100mVP-P VEXT1=0V	1	2	2	1	2	2	1	2	2	3	1	2	1	1	6	32	42	52	dB

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test point	Input	Test conditions S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	Note	Limits Min.	Typ.	Max.	Unit
V_B	Final output amplitude	12	C IN SG0 100mVP-P	1	2	2	1	2	2	1	2	2	3	4	1	1	1		2.4	3.2	4.0	VP-P
V_R		14																	2.1	2.8	3.5	VP-P
V_{CTB}	Crosstalk (carrier beat – 156kHz beat)	12	C IN SG2 100mVP-P	1	2	2	1	2	2	1	2	2	3	4	1	1	1	7	40	48	–	dB
V_{CTR} (Note7)		14																	50	58	–	dB
V_{CTH} (Note8)	1H delay crosstalk	14	C IN SG4	1	2	2	1	2	2	1	2	2	3	4	1	1	1	8	25	30	–	dB
V_{26TH} (Note9)	System priority SW threshold voltage	26	VEXT3 variable	1	2	2	1	2	2	1	1	3	3	4	1	1	1	9	7.0	7.5	8.0	V
V_{26}	Pin ㉖ voltage	26	–	1	2	2	1	2	2	1	2	2	3	4	1	1	1		8.7	9.2	9.7	V
V_{26DR} (Note10)	System SW1 dynamic range	25	EXTAC2 SG5 variable	1	2	2	1	2	2	1	2	3	3	4	1	1	1	10	2.3	3.0	–	VP-P
GI	System SW1 gain	25	EXTAC2 SG1 100mVP-P	1	2	2	1	2	2	1	2	3	3	4	1	1	1		– 3	– 1	1	dB
θ 1	System SW1 phase difference	25	EXTAC2 SG1 100mVP-P	1	2	2	1	2	2	1	2	3	3	4	1	1	1		– 10	– 4	0	deg
CT_{1P} (Note11)	System SW1 crosstalk (P to S)	25	EXTAC2 SG5 2VP-P	1	2	2	1	2	2	1	3	3	3	4	1	1	1	11	50	60	–	dB
CT_{1S} (Note12)	System SW1 crosstalk (S to P)	25	–	1	2	3	1	2	2	1	2	3	3	4	1	1	1	12	50	60	–	dB
V_{16TH} (Note13)	PAL killer detection threshold voltage	25	VEXT2 variable	1	2	2	1	2	2	1	3	3	3	4	1	1	1	13	0.9	1.4	1.9	V
fosc	OSC oscillation frequency	25	–	1	2	2	1	2	2	1	3	3	3	4	1	1	1		4.252	4.255	4.258	MHz
Vosc	Carrier level	25	–	1	2	2	1	2	2	1	3	3	3	4	1	1	1		1.0	1.5	2.0	VP-P
M_{AM} (Note14)	AM modulation degree	25	C IN SG0 100mVP-P	1	2	2	1	2	2	1	2	2	3	4	1	1	1	14	42	53	64	%
THD_{AM} (Note15)	AM demodulator distortion rate	12	VEXT3 VEXT2 EXTAC2 SG6 1.4VP-P	1	1	2	1	2	1	2	3	3	2	4	3	1	2	15	0	1.5	5	%
		14																				
G_{CAM} (Note16)	AM demodulator gain	12	↑	1	1	2	1	2	1	2	3	3	2	4	3	1	2	16	30	33	36	dB
		14																				
V_{21}	Color control pin voltage	21	–	1	2	2	1	2	2	1	2	2	3	4	1	1	1		5.4	5.9	6.4	V
V_{O12} (Note17)	Color control output	12	EXTAC1 SG7 VEXT1 variable	1	1	2	2/1	2	2	1	2	3	3	4	1	1	1	17	1.2	1.5	1.8	VP-P
V_{O14}		14																				VP-P
CC_1 (Note18)	Color control 1	12	↑ V_{21}=7V	1	1	2	2/1	2	2	1	2	3	3	4	1	1	1	18	2	6	10	dB
		14																				
CC_2	Color control 2	12	↑ V_{21}=6V	1	1	2	2/1	2	2	1	2	3	3	4	1	1	1	19	– 3	4	9	dB
		14																				
CC_3	Color control 3	12	↑ V_{21}=5.5V	1	1	2	2/1	2	2	1	2	3	3	4	1	1	1	20	– 55	– 38	– 28	dB
		14																				
CC_{MIN}	Color control color residual	12	EXTAC1 SG7 VEXT1= variable V_{21}=4V	1	1	2	2/1	1	2	1	2	3	3	4	1	1	1	21	–	– 60	– 54	dB
		14																				

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test point	Input	Test conditions															Limits			Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	Note	Min.	Typ.	Max.	
V_{OD}	Output dynamic range	12	EXTAC1 SG7 variable	1	1	2	2	2	2	1	2	3	3	4	1	1	1		4.8	6.0	7.2	V_{P-P}
		14	VEXT1 variable				1															
G_{MAX} (Note19)	Maximum gain	12	EXTAC1 SG7 0.7V_{P-P} V_{21}=8V	1	1	2	2	1	2	1	2	3	3	4	1	1	1	22	11	14	17	dB
		14	VEXT1 variable				1															
B/R	Relative amplitude	12	EXTAC1 SG7 0.4V_{P-P} VEXT1 variable	1	1	2	2	2	2	1	2	3	3	4	1	1	1		0.8	1	1.2	–
G/R		13																	0.4	0.49	0.6	–
G/B		14					1												0.16	0.20	0.24	–
V_{11}	Clamp pin voltage	11	–	1	2	2	1	2	2	1	2	2	3	4	1	1	1		4.0	4.6	5.4	V
V_{15}		15																				V
V_{12DC}	Output pin clamp level	12	–	1	2	2	1	2	2	1	2	3	3	4	1	1	1		6.6	7.2	7.8	V
V_{13DC}		13																	6.5	7.1	7.7	V
V_{14DC}		14																	6.6	7.2	7.8	V
ΔV_{OC}	Differential voltage between clamp level pins	12 13 14	V_{13DC}-V_{12DC} V_{12DC}-V_{14DC} V_{13DC}-V_{14DC}	1	2	2	1	2	2	1	2	3	3	4	1	1	1		−250	0	+150	mV
ΔV_{OCH} (Note20)	DC clamp offset	12 13 14	–	1	2	2	1	2	2	1	2	3	3	4	1	1	1	23	−50	0	+50	mV
ΔV_{OC} (P−S)	Differential voltage between clamp level systems	12 13 14	–	1	2	2	1	2	2	2	3	3	3	4	1	1	1		−50	0	+50	mV
ΔV_{OC} (C)	Output DC voltage color control dependency	12 13 14	V_{21} MIN→MAX	1	2	2	1	1	2	1	2	3	3	4	1	1	1		−30	0	+30	mV
ΔV_{OC} (CD)	Output-to-output DC voltage color control dependency		ΔV_{OC13}-ΔV_{OC12} ΔV_{OC13}-ΔV_{OC14}	1	2	2	1	1	2	1	2	3	3	4	1	1	1		−30	0	+30	mV
V_{CT2} (P→S)	Crosstalk between systems (PAL to SECAM)	12	EXTAC1 SG7 1V_{P-P}	1	2	2	2	2	2	1	3	3	3	4	1	1	1		–	1	10	mV
		14					1															
V_{CT2} (S→P)	Crosstalk between systems (SECAM to PAL)	12	EXTAC2 SG6 1.5V_{P-P}	1	2	1	2	2	2	2	2	1	3	4	1	1	1		–	3	15	mV
V_{OCL}	Carrier leak	12	EXTAC2 SG5 1.5V_{P-P}	1	2	3	2	2	2	2	2	1	3	4	1	1	1		–	100	260	mV_{P-P}
		14																				
Bv (Note21)	Output amplifier frequency characteristics	12	EXTAC1 SG8 100mV_{P-P}	1	1	2	2	2	2	1	2	3	3	4	1	1	1	24	2.4	3	4.5	MHz
		14					1															
$V_{OC\theta}$	Output clamp level temperature dependency	12 13 14	–	1	2	2	1	2	2	1	2	3	3	4	1	1	1		−2	−1	0	mV/℃
V_{OCV}	Output clamp level supply voltage dependency	12 13 14	–	1	2	2	1	2	2	1	2	3	3	4	1	1	1		0.4	0.6	0.8	mV/V
$\Delta V_{OC\theta}$	Output-to-output differential voltage temperature dependency	12 13 14	$V_{OC\theta}$ (13-12) $V_{OC\theta}$ (13-14)	1	2	2	1	2	2	1	2	3	3	4	1	1	1		−1	0	+1	mV/℃

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test point	Input	Test conditions															Limits			Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	Note	Min.	Typ.	Max.	
Δ Vocv	Output-to-output differential voltage-supply voltage dependency	12 13 14		1	2	2	1	2	2	1	2	3	3	4	1	1	1		− 25	0	+ 25	mV/V
TDL (Note22)	Delay time	12	C IN SG4 100mVP-P	1	2	2	1	2	2	1	2	3	3	4	1	1	1	25	550	650	750	nsec
BGP ON	Burst gate pulse	27	C IN SGO 100mVP-P VEXT1 variable	1	2	2	1	2	2	1	2	2	1	4	1	1	1	26	5.4	5.9	−	Vo-P
BGP OFF (Note23)																			−	4.1	4.6	Vo-P
VVTH (Note24)	V pulse	3	C IN SGO 100mVP-P VEXT1 variable	1	2	2	1	2	2	1	2	2	3	4	2	1	1	27	0.9	1.1	1.3	Vo-P
VBLK (Note25)	Blanking	12	C IN SGO 100mVP-P VEXT1 variable	1	2	2	1	2	2	1	2	2	3	2	1	1	1	28	3.2	3.7	4.2	Vo-P
VFF (Note26)	FF drive	12	C IN SGO 100mVP-P VEXT1 variable	1	2	2	1	2	2	1	2	2	3	3	1	1	1	29	6.2	6.7	7.2	Vo-P

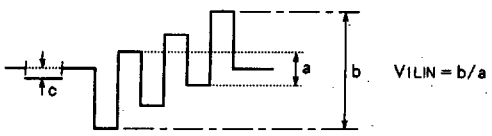
ELECTRICAL CHARACTERISTICS TEST METHOD

Note1. Lower the SG1 level, and measure the input voltage at which V_{O32} is −3dB.

Note2. Reduce the SG0 level (pin ⑨ input waveform) and assume the input voltage at which the killer is effective to be Vkill (v):

$$I/K = 20 \log \frac{Vkill\ (v)}{0.1}$$

Note3.



Note4. Assuming the carrier leak level at pin ① to be VmVP-P, V_{1CL} is calculated as follows for B–Y amplitude V_{1B} of FM demodulator relative amplitude:

$$V_{ICL} = 20 \log \frac{V}{V_{1B}}\ (dB)$$

Note5. In pin ⑫ output waveform, define the blanking period and black level shift C as a step difference.

Note6. Remove the BLK pulse and measure the amplitude at pin 7A with SG3 as ±75kHz dev FM: it should be taken as V_{FM}. Next, with SG3 as 30% AM, assume its amplitude to be V_{AM}: AMR is determined by:

$$AMR = 20 \log \frac{V_{FM}}{V_{AM}}$$

Note7. Input SGO and assume the output at pin ⑫ to be VB. Next, input SG2 and assume 156kHz beat P and beat component with OSC outputted during other periods than BLK to be V_{BEAT}: V_{CTB} is found by:

$$V_{CTB} = 20 \log \frac{VB}{V_{BEAT}}$$

Also measure R–Y in the same manner.

Note8. Measure B–Y component outputted during other periods than BLK at pin ⑭ and assume it to be V_{CB-Y}: V_{CTH} is found by:

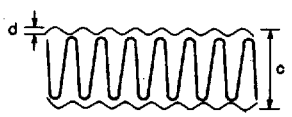
$$V_{CTH} = 20 \log \frac{VB}{V_{CB-Y}}$$

Note9. Change the voltage of VEXT3 and define pin ㉖ voltage when 4.25MHz carrier starts to generate from pin ㉕ as V_{26TH}.

Note10. Change SG5 output and define the SG5 output level when the waveform at pin ㉕ starts to be distorted as V_{26DR}.

Note11. Observe pin ㉕. CT_{1P} is found by:

$$CT_{1P} = 20 \log \frac{c}{d}$$



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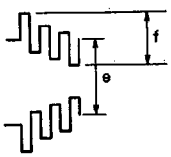
Note12. Measure 4.25MHz leaking to pin ㉕ and assume it to be $XV_{P\text{-}P}$. CT_{1S} is determined by:

$$CT_{1S} = 20 \log \frac{z}{x}$$

Note13. Observe pin ㉕ and increase VEXT2 from 0V, then measure the VEXT2 voltage when 4.25MHz is absent.

Note14. $M_{AM} = \frac{f}{e} \times 100\%$



Note15. Set VEXT3 to 5.7V. Change VEXT1 so that the average voltage on pin ⑫ becomes 7.2V. At this time, measure the distortion at pins ⑫, ⑭.

Note16. Assume the output level at pins ⑫, ⑭ in Note14 above to be $XV_{P\text{-}P}$. G_{CAM} is found by:

$$G_{CAM} = 20 \log \frac{x}{Input} \text{ (dB)}$$

Note17. Change VEXT1 so that the average voltage on pin ⑫ becomes 7.2V. At this time, measure the output level.

Note18. Set VEXT1 in the same manner as in Note17 above and measure the output level as $XV_{P\text{-}P}$.

$$CC_1 = 20 \log \frac{x}{V_{O12}} \text{ or } 20 \log \frac{x}{V_{O14}} \text{ (dB)}$$

Note19. Measure the output level as $XV_{P\text{-}P}$.

$$G_{MAX} = 20 \log \frac{x}{0.7} \text{ (dB)}$$

However, set VEXT1 in the same manner as in Note16 above.

Note20. Measure the voltage difference between the output clamp period and other periods.

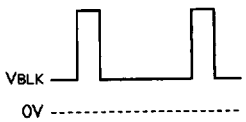
Note21. Change SG8 from 100kHz so that the output amplitude at pins ⑫, ⑭ is –3dB from the level of 100kHz.

Note22. With the delay of output waveform (direct side) at pin ⑫ for SG4 inputted to C IN as T_{DL}, measure the condition at rise.

Note23. Increase VEXT1 from 4V and define it as V_{BGPON} when pin ㉗ voltage is 0.6V or less. Decrease it further from V_{BGPON} and define VEXT1 as V_{BGPOFF} when it is 0.6V or more.

Note24. Increase VEXT1 from 0V, and define it as V_{VTH} when pin ③ voltage is approx. 3V.

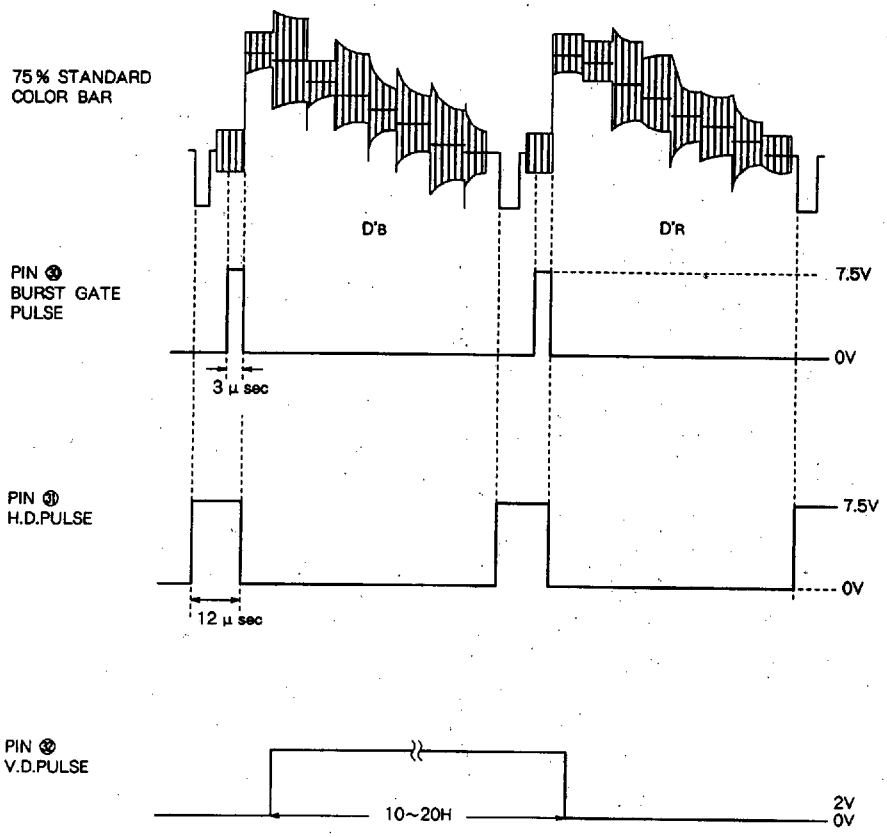
Note25. Increase VEXT1 from 0V and define pin ㉛ voltage as V_{BLK} when the waveform on pin ⑫ disappears.



Note26. Decrease VEXT1 from V_{CC}, and define the maximum voltage on pin ㉛ as V_{FF} when the waveform on pin ⑫ disappears.

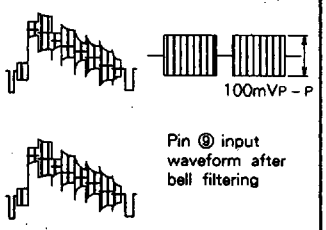
Point of Caution in Electrical Characteristic Testing:

1) For this IC to operate normally, it is necessary to input each pulse with timing and pulse width as shown below. (when Vcc=12V)



2) When SECAM signal is input, adjust the IDENT coil so that IDENT filter pin (pin ㉙) voltage becomes maximum. (when Vcc=12V and V_{29}=approx.9.6V)

INPUT SIGNAL

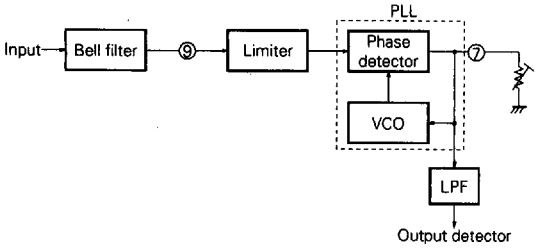
SG No.	Signal name	Signal contents
SG0	75% standard color bar	
SG1	4.328MHz CW	100mVP-P
SG2	Monochrome signal	
SG3	fo = 4.25 MHz	75kHz dev FM fm = 400Hz
		30% AM fm = 400Hz
SG4		Signal in which only R-Y is monochrome from 75% standard color bar signal
SG5	4.0MHz CW	
SG6	fo = 4.3MHz	50% AM fm = 400Hz
SG7	500kHz CW	
SG8	100mVP-P CW	Frequency variable

PRECAUTIONS FOR APPLICATION

1. Colour signal demodulator

The M52026SP uses a phase locked loop (PLL) for FM detection of colour signals.

The chroma signal is input through a bell filter and passed, via pin 9, to the input of a limiter amplifier (DC gain = 64 dB) which limits the signal amplitude. The signal is then input to the PLL detector. The following figure outlines the structure of the FM detector.

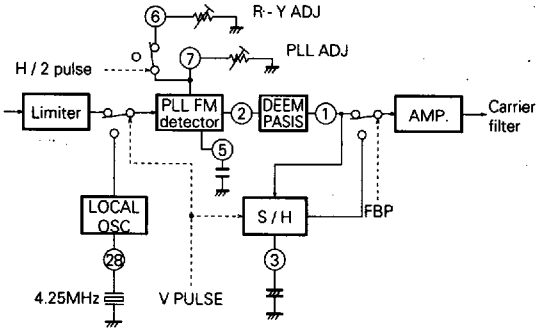


The PLL consists of an emitter coupled multivibrator VCO and double balanced multiplier. The output of the VCO is multiplied by the limiter output, and this is fed back to the VCO. When the PLL is locked on to the input of the FM detector, the output of the PLL becomes the phase detector output, which is passed on to the LPF.

The loop time constant for the PLL is designed to be sufficiently short in order to respond well to the chroma signal. The VCO control characteristics show good linearity compared with Quadrature type FM demodulators.

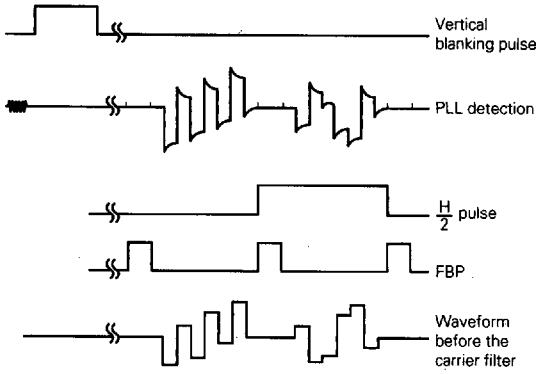
It is possible to adjust the freerun frequency of the VCO by varying the resistor at pin 7, as follows: for good linearity adjust the DC output voltage at pin 7, using VR, to the non-signal level of 3V DC when the input to the VCO is at 4.33MHz.

The B-Y black level is determined by the frequency of the local oscillator; therefore, during the vertical blanking period the local oscillator is switched to the input of the PLL FM detector in place of the limiter output; this input is demodulated to the black level voltage. This voltage is then input to the sample and hold circuit. The S/H circuit stores the black level which, during the horizontal blanking period, is switched to the amplifier preceding the carrier filter.

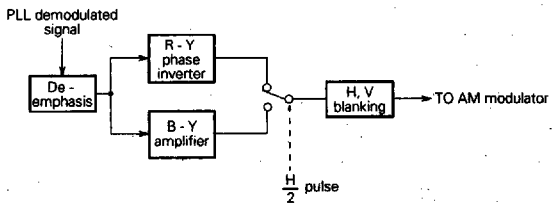


The R-Y black level is adjusted to the B-Y black level by varying the external resistor at pin 6.

Pin 7's external resistor adjusts the VCO free-run frequency; this, however, does not affect the B-Y black level.



2. B–Y & R–Y amps



The signal obtained by the PLL FM demodulator is input the amplifier circuit after de-emphasis by external parts. Then R–Y is phase inverted, and the gain ratio of R–Y and B–Y is

$$\frac{R-Y}{B-Y} = -0.7$$

The colour difference signals are passed alternately (switched by the H/2 pulse) to the H and V blanking circuits.

3. Ident Detector

The ident detector uses Quadrature FM detection. During the H/2 pulse, the detection output is reversed every 1H and is sampled during the gate pulse, the value being held for one line period, and then the voltage is output at pin 29.

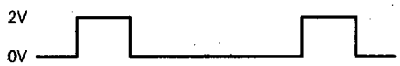
Ident and killer detection are performed by means of comparison with this DC voltage.

When ident is normal, the voltage at pin 29 rises above that of the non-signal level.

The ident technique employed by the M52026SP is the Line ident system, which requires a line burst gate pulse; but it is possible to add field ident gate pulses without affecting normal operation.

During the V blanking pulse, which is input at pin 32, the B-Y blank-level is sampled and held.

The V blanking pulse is approximately 2V relative to the ground.

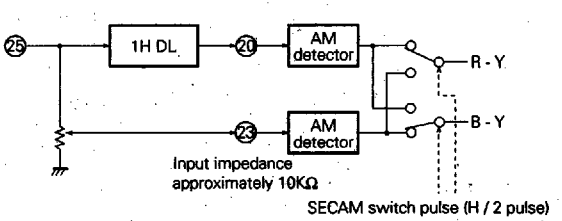


4. AM modulator and oscillator

The colour difference signal, after passing through the LPF, is amplitude modulated and output from pin 25. The modulation depth is fixed. The local oscillator is connected to the crystal, via pin 28; the other side of the crystal is connected to the ground.

5. AM detector, SECAM switch

The following figure shows how the AM modulated signal, output from pin 25, is demodulated to colour difference signals.



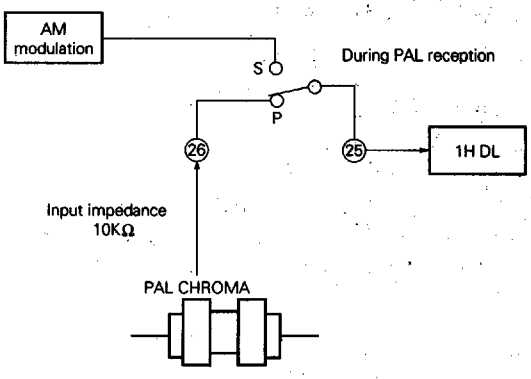
Pin 25 outputs the chroma signal, and the direct signal is input to pin 23, the delayed signal to pin 20. After each signal is AM detected, R–Y and B–Y are obtained by switching between detector outputs every 1H.

6. System switches

There are two PAL/SECAM switching systems

System switch I

This switch is used to switch input signals of 1HDL



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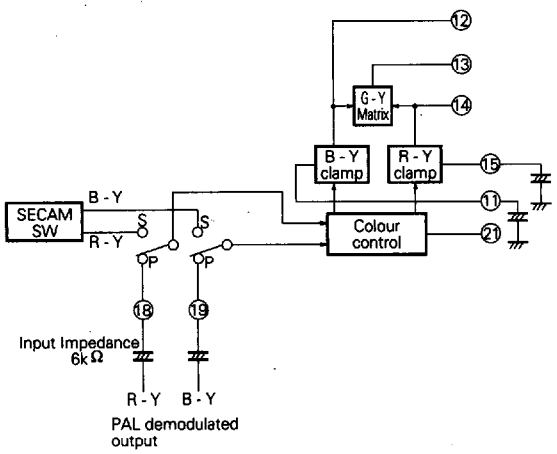
System switch II

This switch is used to switch between R–Y and B–Y signals.

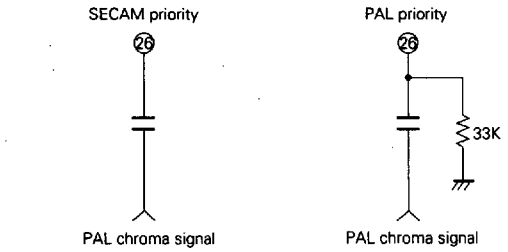


The R–Y signal and B–Y signal pass through this system switch and are routed to the colour control circuit, where clamping takes place; G–Y is obtained.

7. System Identification

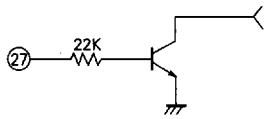
This IC can be operated in both SECAM priority mode and PAL priority mode. In both cases, the system is prevented from malfunctioning by the killer output applied to pin 16.

Input Condition	SECAM ID	PAL ID	SECAM priority system identification	PAL priority system identification
Monochrome or weak electric field	NOT SECAM	NOT PAL	PAL	SECAM
PAL receiving	NOT SECAM	PAL	PAL	PAL
SECAM receiving	SECAM	NOT PAL	SECAM	SECAM
Misoperation	SECAM	PAL	Previous system	Previous system



Pin 16 is the input of the PAL killer signal from the PAL IC. If this signal is high (threshold voltage is 1.5V), then PAL is present (PAL); if low, then PAL is not present (NOT PAL).

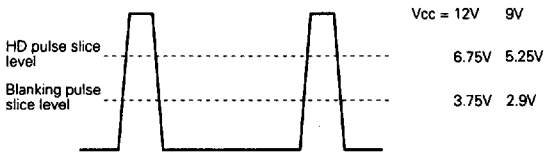
Pin 27 is the output of the SECAM killer signal. If it is high (0.9V), then SECAM is not present (NOT SECAM); if low, then SECAM is present (SECAM).



How SECAM killer signal output is obtained.

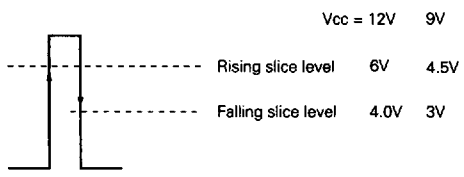
8. H, V pulse

HD pulse and blanking pulse are input from pin 31.



9. Burst gate pulse

Burst gate pulse is input from pin 30.

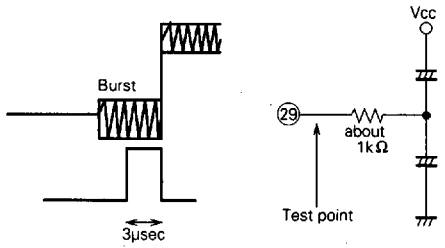


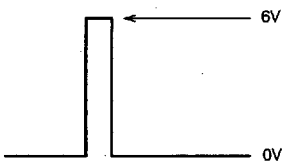
Note

This IC requires a 4.25MHz crystal with a parallel resonance point. The crystal should have good temperature characteristics.

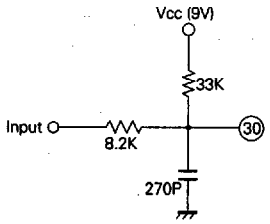
The following figure shows how to adjust the location of the bust gate pulse at pin 29.

The width should be approximately 3μsec. The location and width can be varied by adding external circuitry at pin 30.

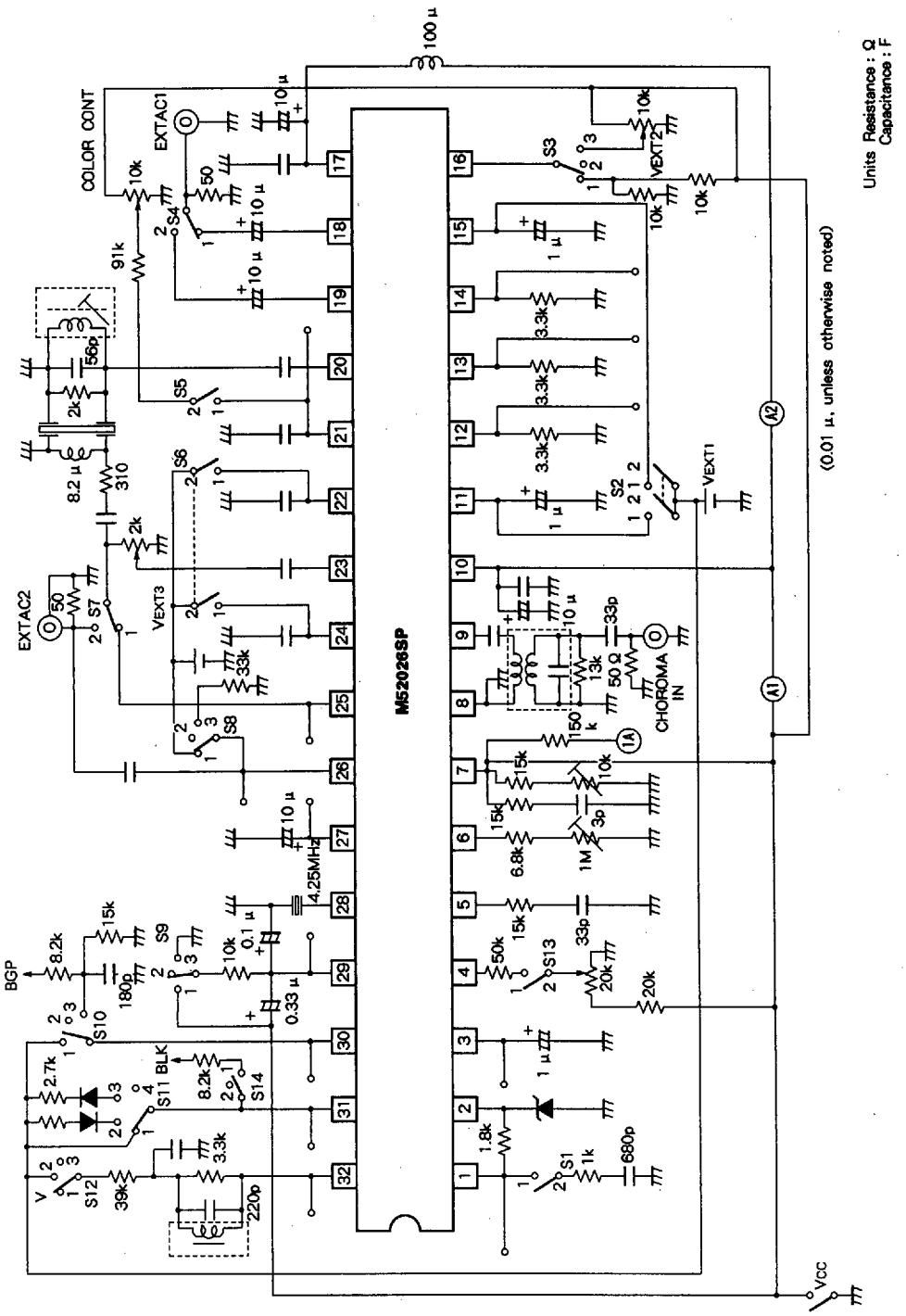




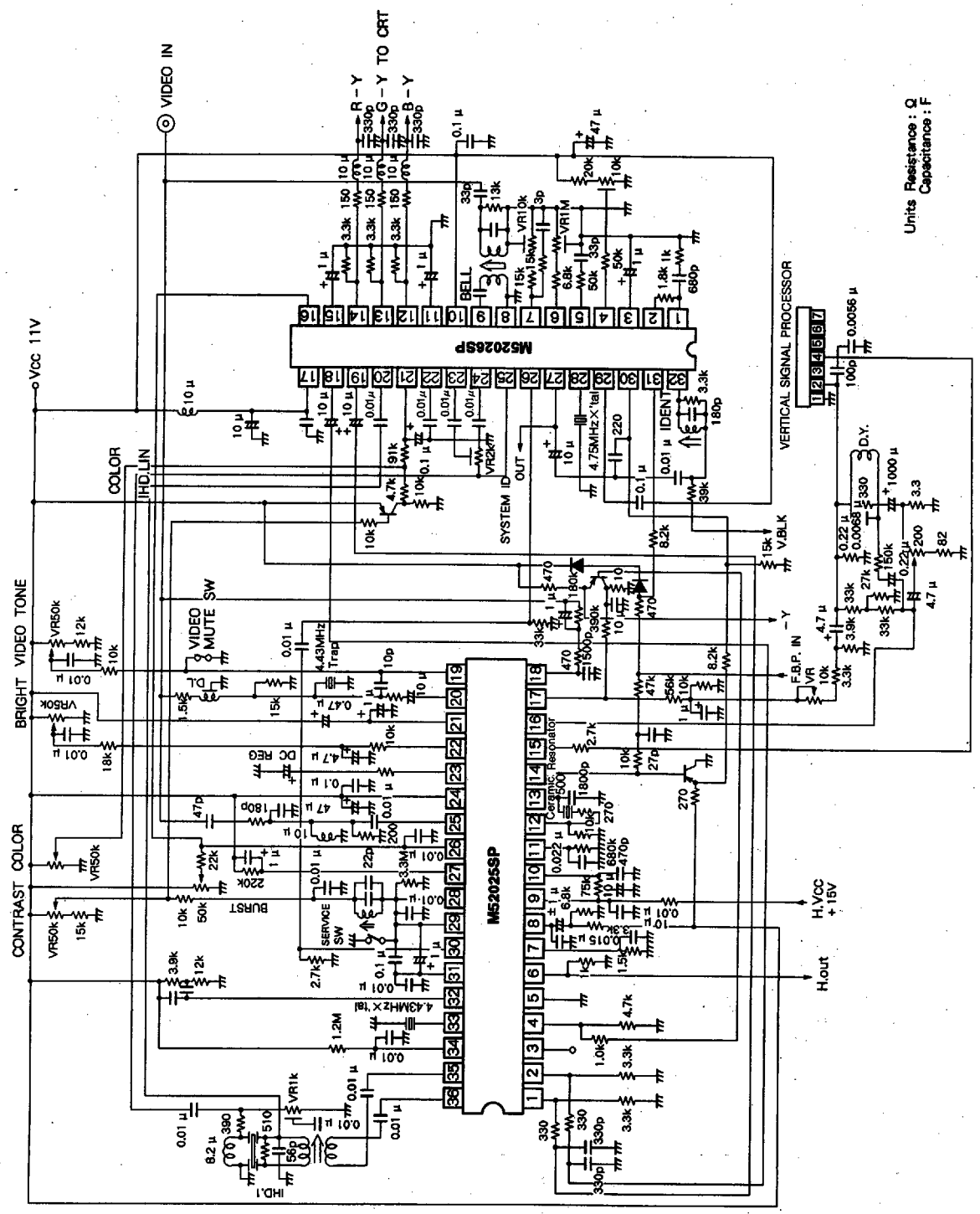
BGP in the figure to the left is soldered externally as shown below.



TEST CIRCUIT



APPLICATION EXAMPLE



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