FAIRCHILD
SEMICONDUCTOR ™

March 1996

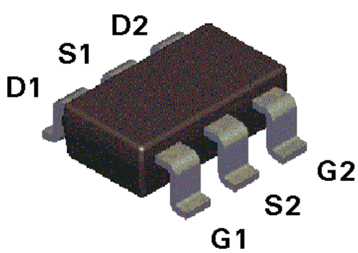
NDC7001C
Dual N & P-Channel Enhancement Mode Field Effect Transistor

General Description

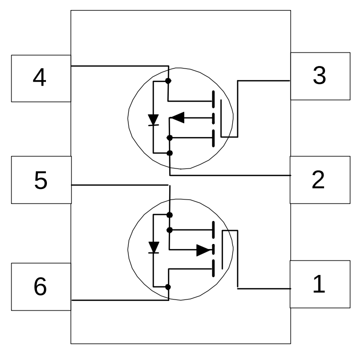
These dual N and P-channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. These devices is particularly suited for low voltage, low current, switching, and power supply applications.

Features

- N-Channel 0.51A, 50V, $R_{DS(ON)}$ = 2Ω @ V_{GS}=10V
- P-Channel -0.34A, -50V. $R_{DS(ON)}$= 5Ω @ V_{GS}=-10V.
- High density cell design for low $R_{DS(ON)}$.
- Proprietary SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High saturation current.



SuperSOT™-6



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		50	-50	V
V_{GSS}	Gate-Source Voltage - Continuous		20	-20	V
I_D	Drain Current - Continuous	(Note 1a)	0.51	-0.34	A
	- Pulsed		1.5	-1	
P_D	Maximum Power Dissipation	(Note 1a)	0.96		W
		(Note 1b)	0.9		
		(Note 1c)	0.7		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	130		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	60		°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)							
Symbol	**Parameter**	**Conditions**	**Type**	**Min**	**Typ**	**Max**	**Units**
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	50			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-50			
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V	N-Ch			1	µA
		T_J = 125°C				500	
		V_{DS} = -40 V, V_{GS} = 0 V	P-Ch			-1	
		T_J = 125°C				-500	
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.9	2.5	V
		T_J = 125°C		0.8	1.5	2.2	
		V_{DS} = V_{GS}, I_D = -250 µ.A	P-Ch	-1	-2.5	-3.5	
		T_J = 125°C		-0.8	-2.2	-3	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.51 A	N-Ch		1	2	Ω
		T_J = 125°C			1.7	3.5	
		V_{GS} = 4.5 V, I_D = 0.35 A			1.6	4	
		V_{GS} = -10 V, I_D = -0.34 A	P-Ch		2.5	5	
		T_J = 125°C			4	10	
		V_{GS} = -4.5 V, I_D = -0.25 A			5.3	7.5	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	N-Ch	1.5			A
		V_{GS} = -10 V, V_{DS} = -10 V	P-Ch	-1			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 0.51 A	N-Ch		400		mS
		V_{DS} = -10 V, I_D = -0.34 A	P-Ch		250		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		20		pF
			P-Ch		40		
C_{oss}	Output Capacitance		N-Ch		13		pF
		P-Channel V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		13		
C_{rss}	Reverse Transfer Capacitance		N-Ch		5		pF
			P-Ch		4		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameters	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 25 V, I_D = 0.25 A, V_{GS} = 10 V, R_{GEN} = 25 Ω	N-Ch		6	20	nS
			P-Ch		14	20	
t_r	Turn - On Rise Time		N-Ch		6	20	
			P-Ch		6	20	
$t_{D(off)}$	Turn - Off Delay Time	P-Channel V_{DD} = -25 V, I_D = -0.25 A, V_{GS} = -10 V, R_{GEN} = 25 Ω	N-Ch		11	20	
			P-Ch		13	20	
t_f	Turn - Off Fall Time		N-Ch		5	20	
			P-Ch		6	20	
Q_g	Total Gate Charge	N-Channel V_{DS} = 25 V, I_D = 0.51 A, V_{GS} = 10 V	N-Ch		1		nC
			P-Ch		1.3		
Q_{gs}	Gate-Source Charge	P-Channel V_{DS} = -25 V, I_D = -0.34 A, V_{GS} = -10 V	N-Ch		0.19		nC
			P-Ch		0.23		
Q_{gd}	Gate-Drain Charge		N-Ch		0.33		nC
			P-Ch		0.38		
DRAIN-SOURCE DIODE CHARACTERISTICS							
I_S	Maximum Continuous Source Current		N-Ch			0.51	A
			P-Ch			-0.34	
I_{SM}	Maximum Pulse Source Current (Note 2)		N-Ch			1.5	A
			P-Ch			-1	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.51 A (Note 2)	N-Ch		0.8	1.2	V
		V_{GS} = 0 V, I_S = -0.34 A (Note 2)	P-Ch		-0.8	-1.2	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

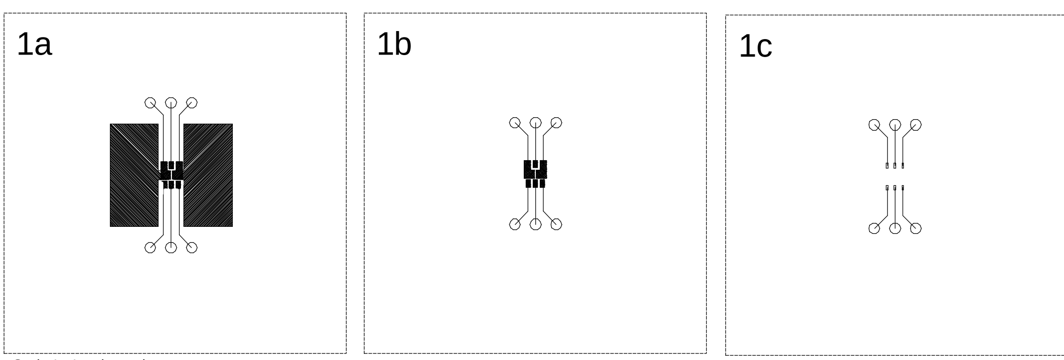
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)} @ T_J$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 130°C/W when mounted on a 0.125 in^2 pad of 2oz cpper.

b. 140°C/W when mounted on a 0.005 in^2 pad of 2oz cpper.

c. 180°C/W when mounted on a 0.0015 in^2 pad of 2oz cpper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

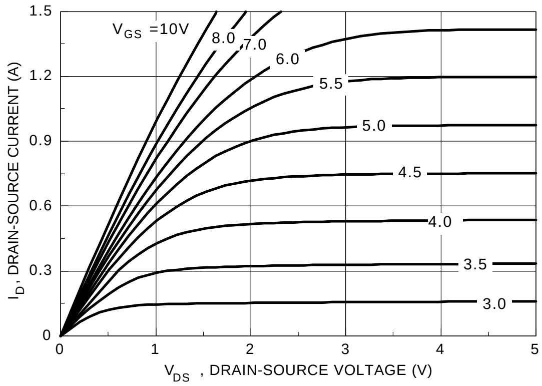


Figure 1. N-Channel On-Region Characteristics.

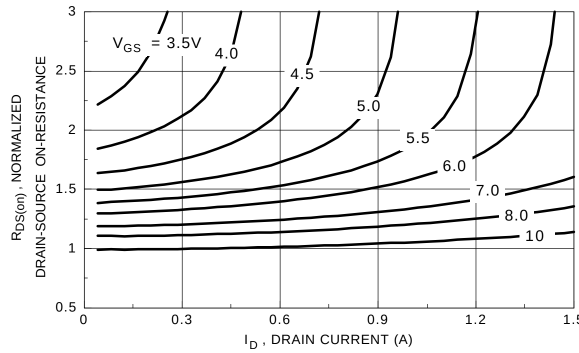


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

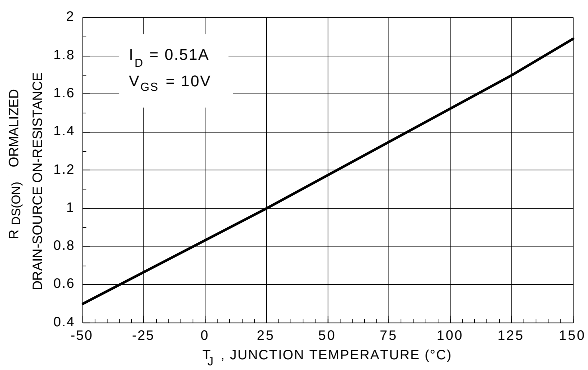


Figure 3. N-Channel On-Resistance Variation with Temperature.

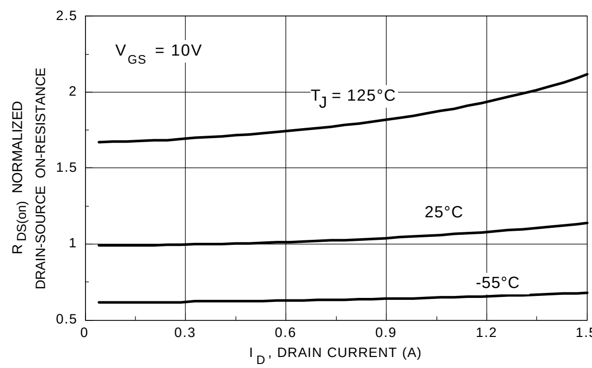


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

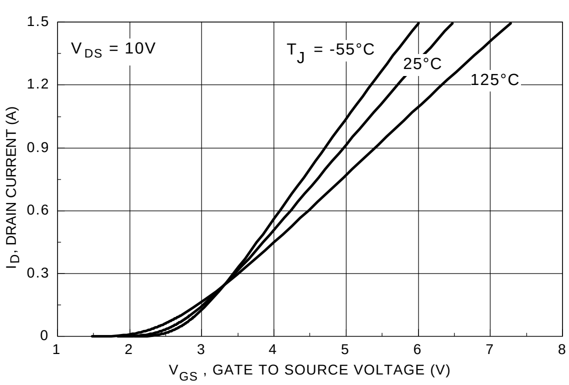


Figure 5. N-Channel Transfer Characteristics.

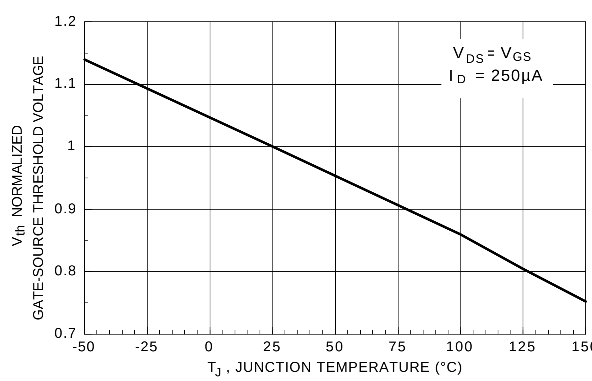


Figure 6. N-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

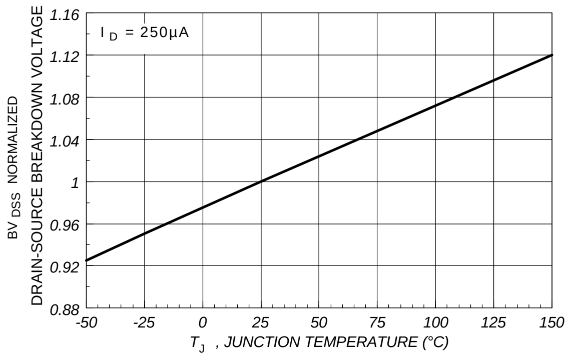


Figure 7. N-Channel Breakdown Voltage Variation with Temperature.

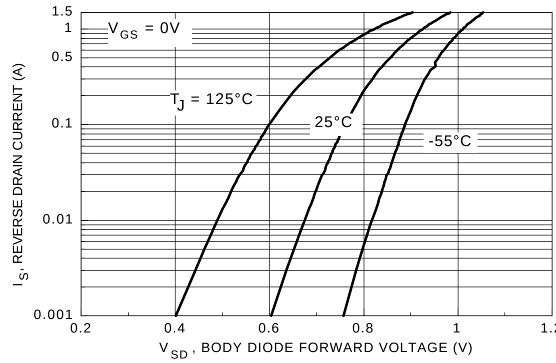


Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

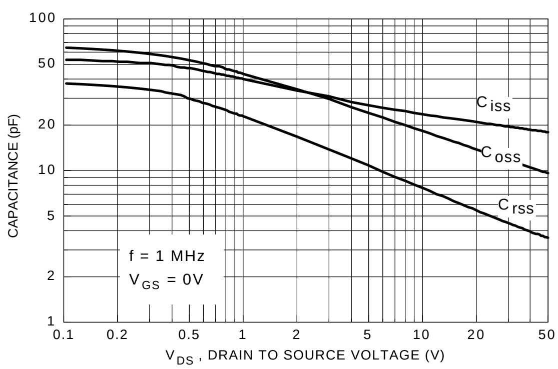


Figure 9. N-Channel Capacitance Characteristics.

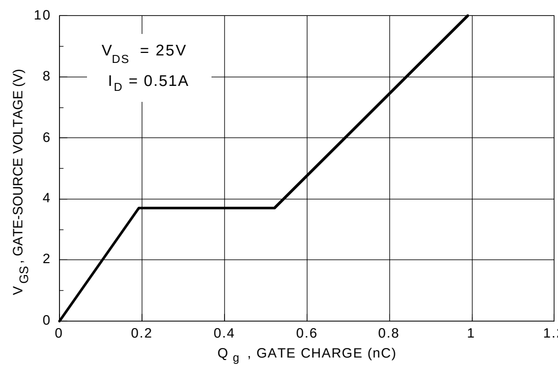


Figure 10. N-Channel Gate Charge Characteristics.

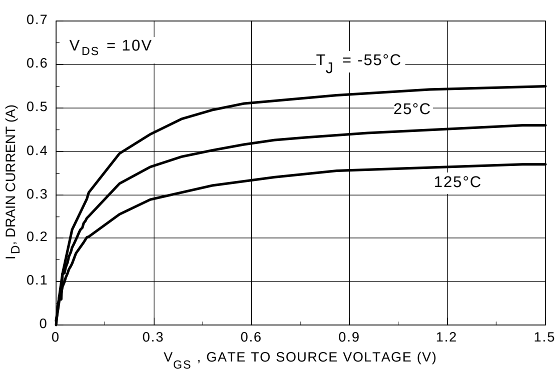


Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

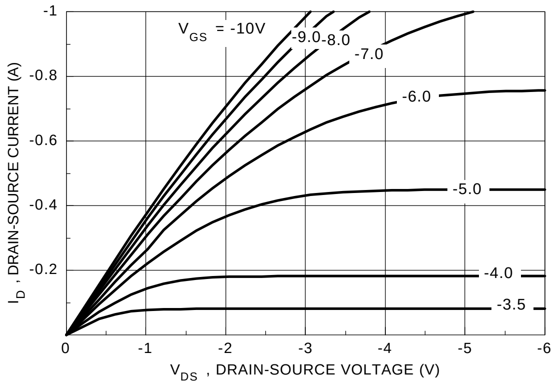


Figure 12. P-Channel On-Region Characteristics.

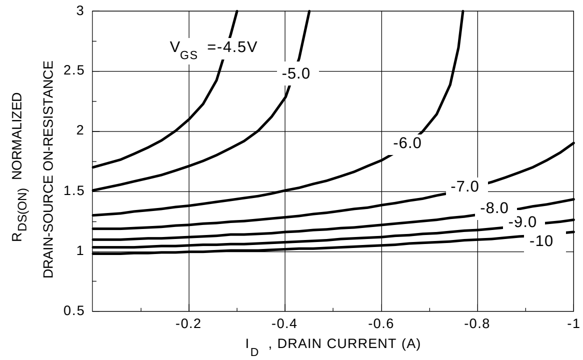


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

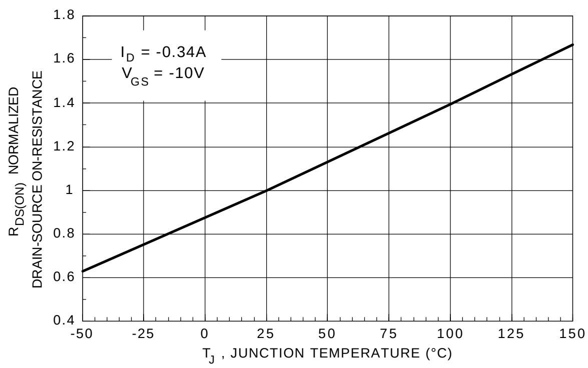


Figure 14. P-Channel On-Resistance Variation with Temperature.

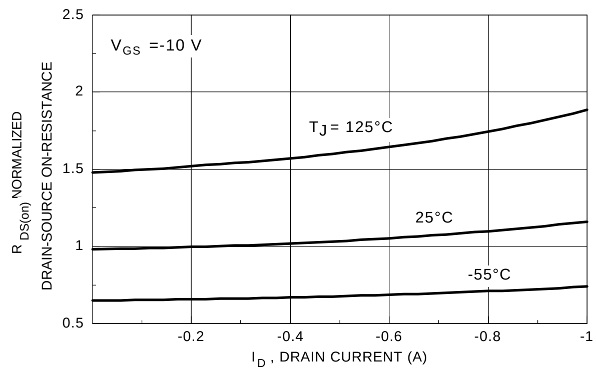


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

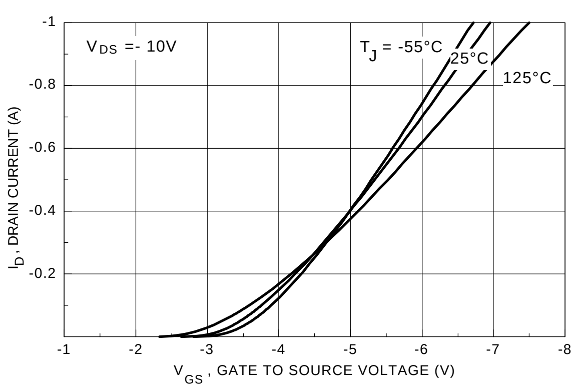


Figure 16. P-Channel Transfer Characteristics.

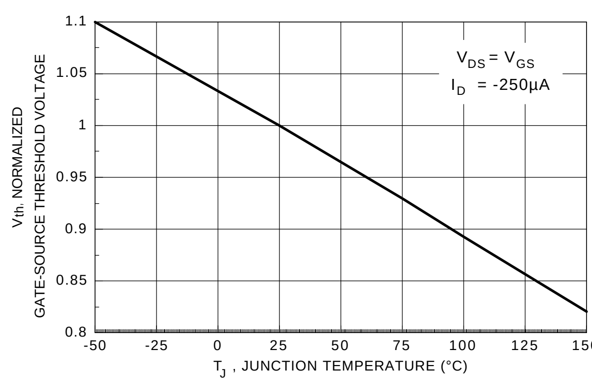


Figure 17. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

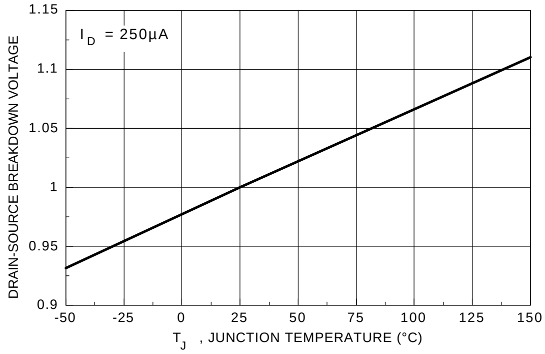


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

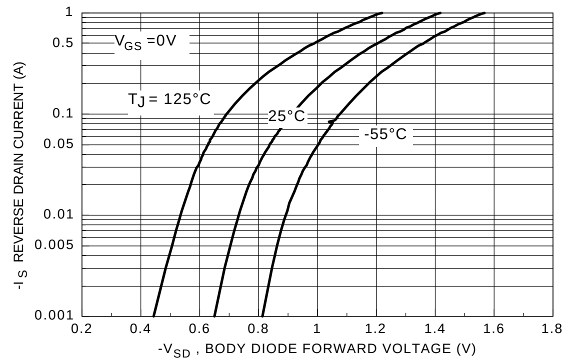


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

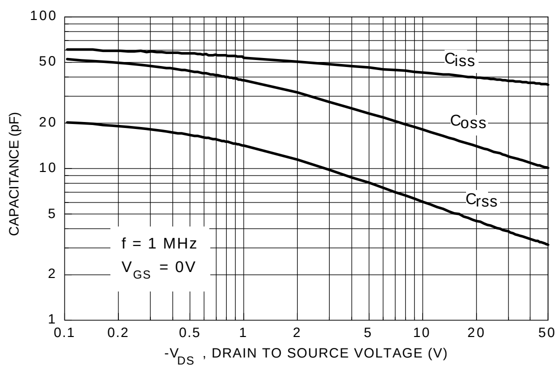


Figure 20. P-Channel Capacitance Characteristics.

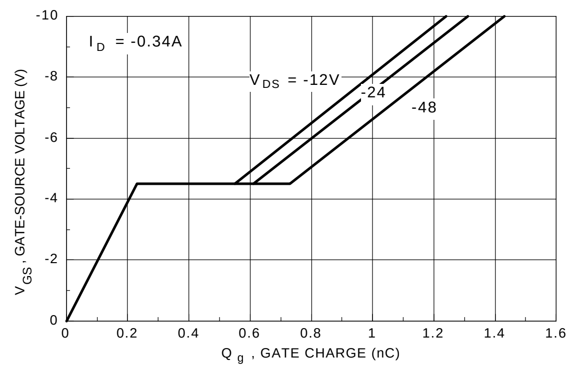


Figure 21. P-Channel Gate Charge Characteristics.

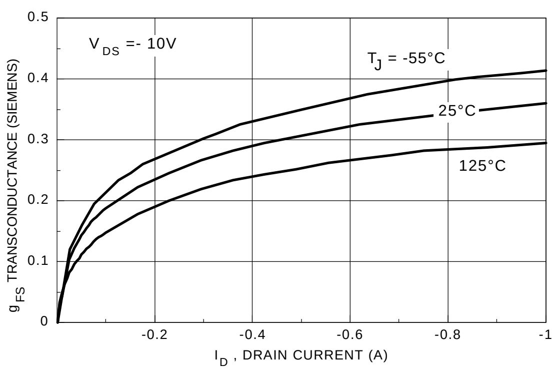


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics: N & P-Channel

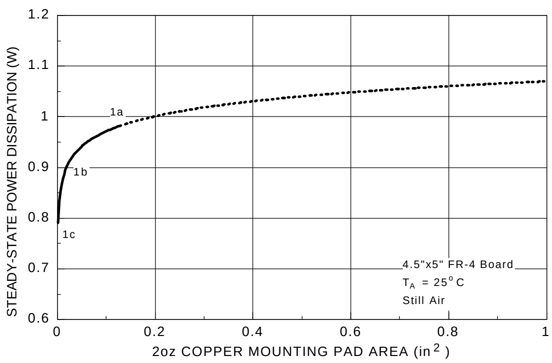


Figure 23. SOT-6 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

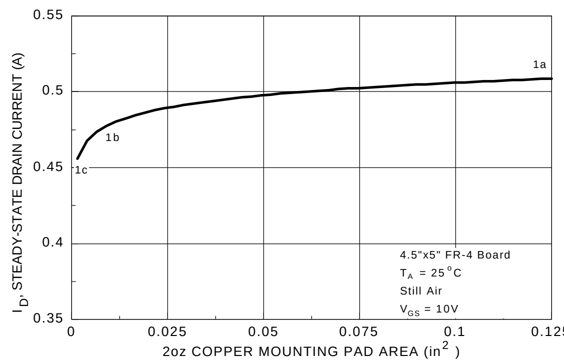


Figure 24. N-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

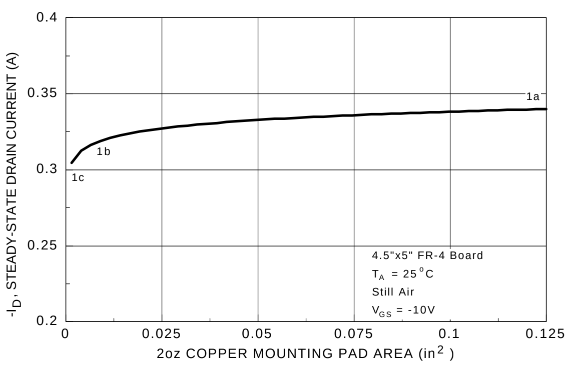


Figure 25. P-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

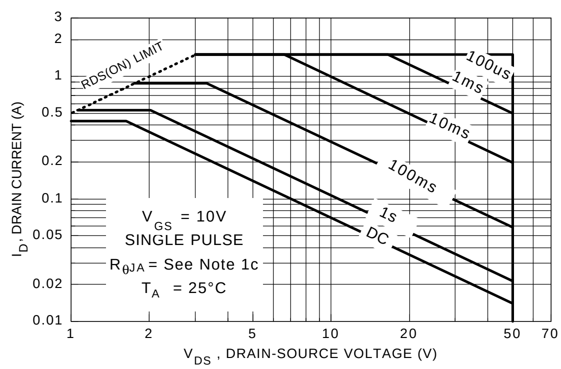


Figure 26. N-Channel Maximum Safe Operating Area.

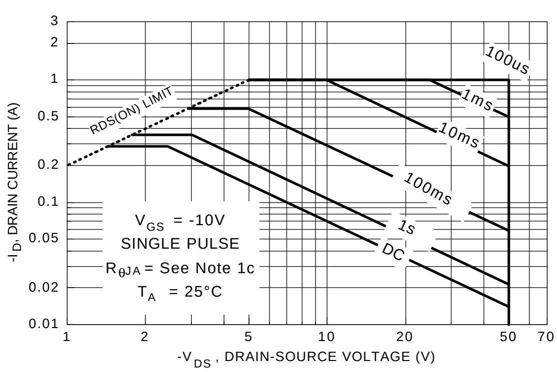


Figure 27. P-Channel Maximum Safe Operating Area.

Typical Thermal Characteristics: N & P-Channel

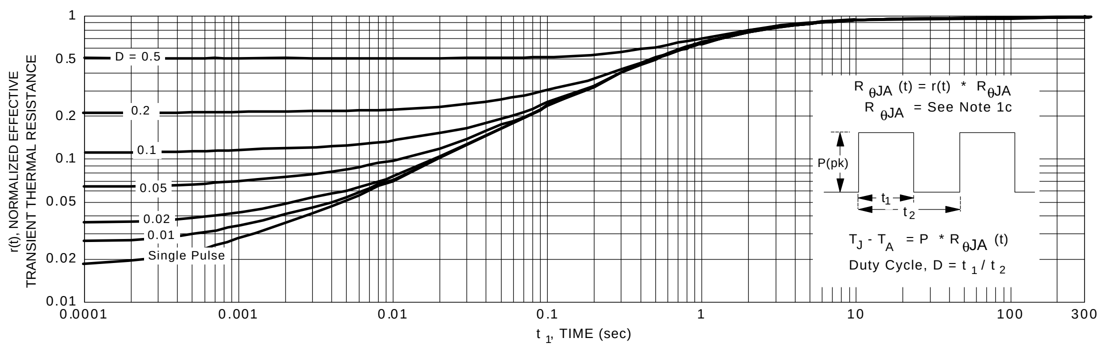


Figure 28. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

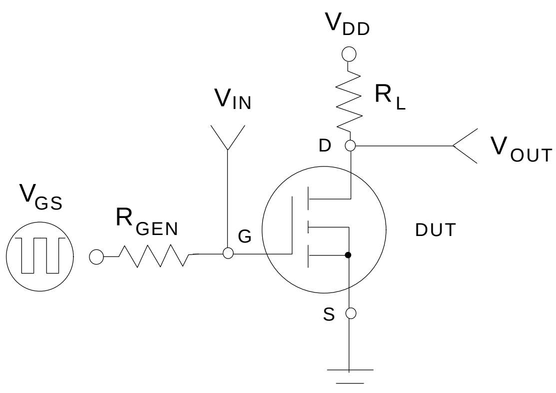


Figure 29. N or P-Channel Switching Test Circuit.

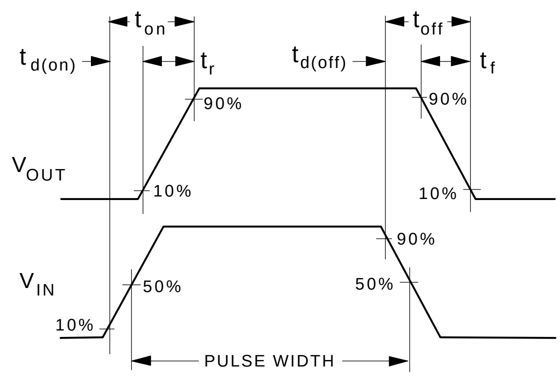
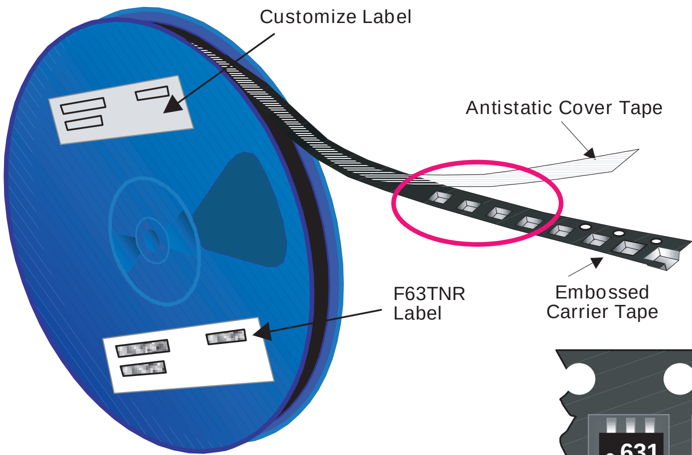


Figure 30. N or P-Channel Switching Waveforms.

SuperSOT™-6 Tape and Reel Data and Package Dimensions

SSOT-6 Packaging
Configuration: Figure 1.0

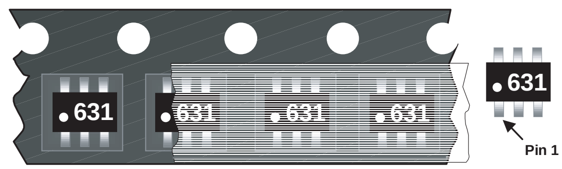


Packaging Description:

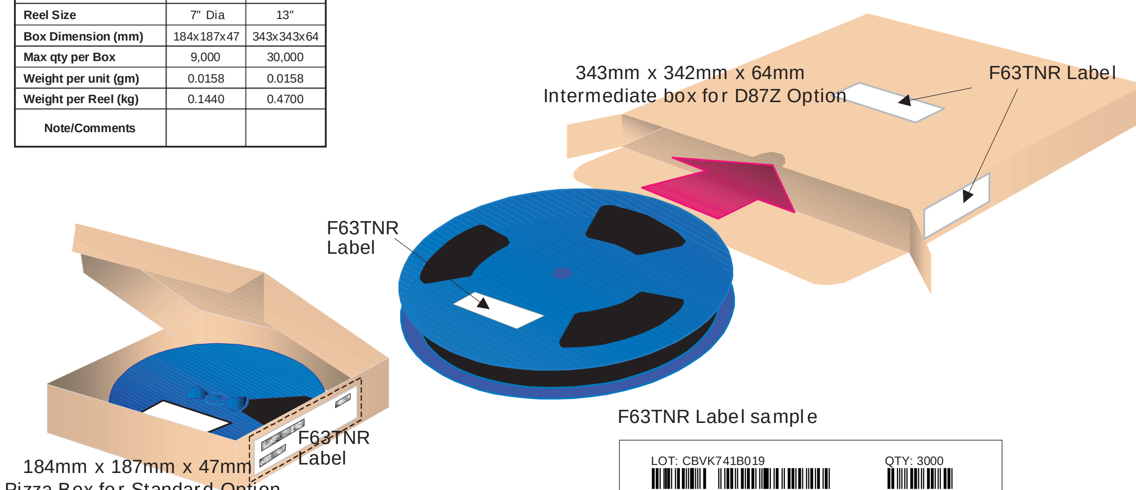
SSOT-6 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 7" or 177cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 10,000 units per 13" or 330cm diameter reel. This and some other options are described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a pizza box (illustrated in figure 1.0) made of recyclable corrugated brown paper with a Fairchild logo printing. One pizza box contains three reels maximum. And these pizza boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

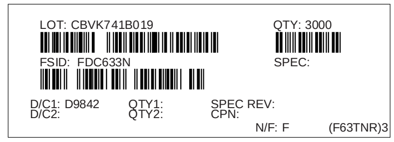
SSOT-6 Packaging Information		
Packaging Option	Standard (no flow code)	D87Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	10,000
Reel Size	7" Dia	13"
Box Dimension (mm)	184x187x47	343x343x64
Max qty per Box	9,000	30,000
Weight per unit (gm)	0.0158	0.0158
Weight per Reel (kg)	0.1440	0.4700
Note/Comments		



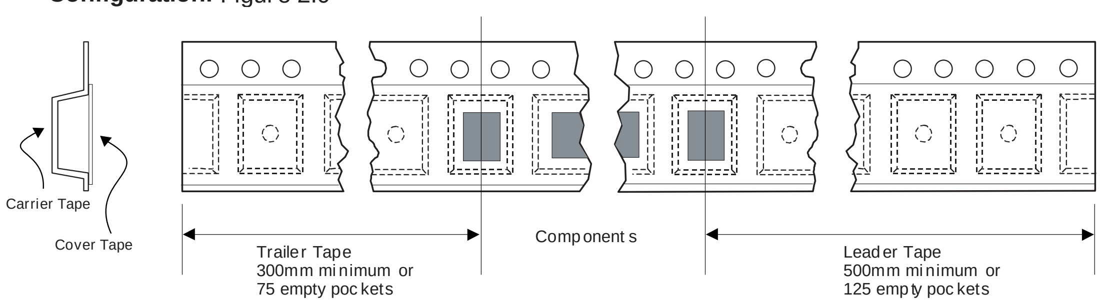
SSOT-6 Unit Orientation



F63TNR Label sample

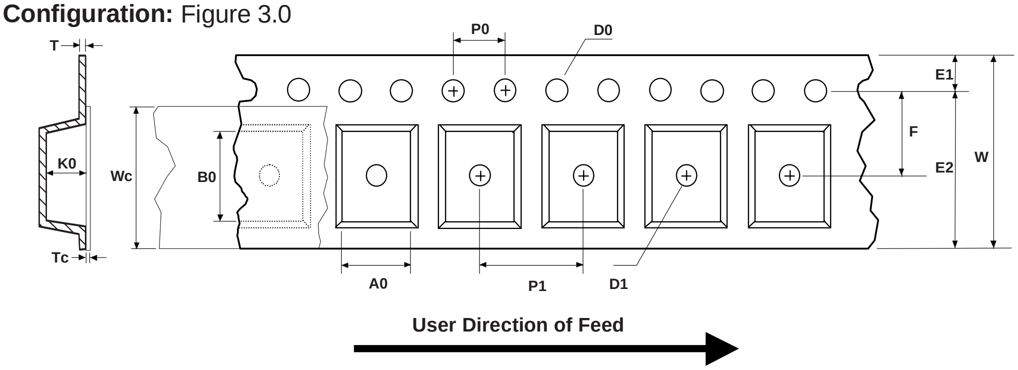


SSOT-6 Tape Leader and Trailer
Configuration: Figure 2.0



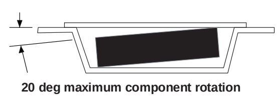
SuperSOT™-6 Tape and Reel Data and Package Dimensions, continued

SSOT-6 Embossed Carrier Tape Configuration: Figure 3.0

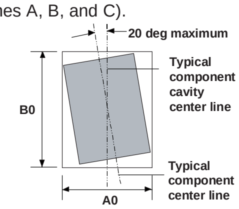


Dimensions are in millimeter													
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SSOT-6 (8mm)	3.23 +/-0.10	3.18 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.255 +/-0.150	5.2 +/-0.3	0.06 +/-0.02

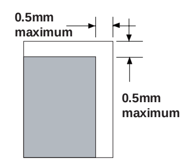
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

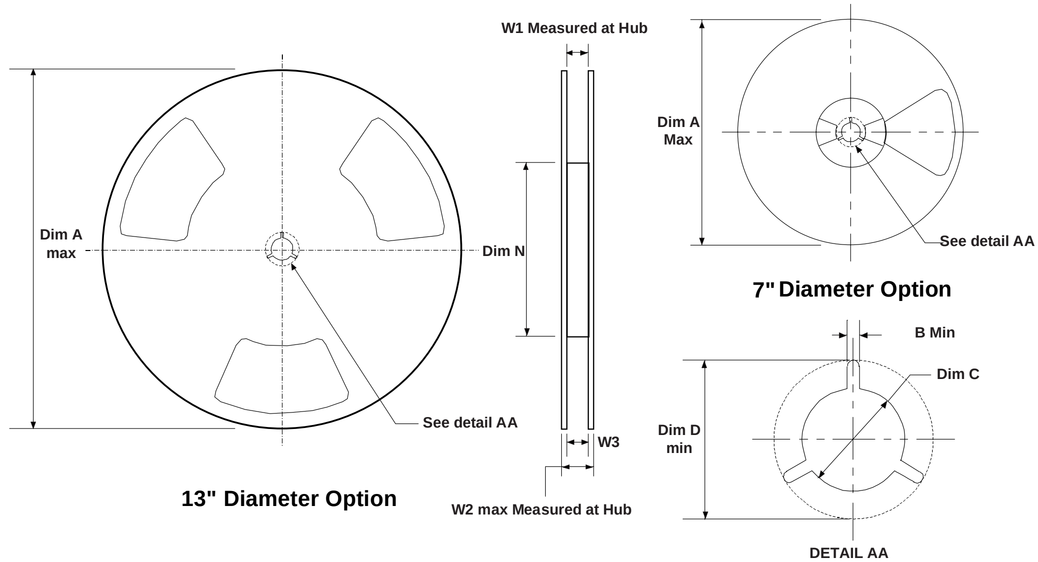


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

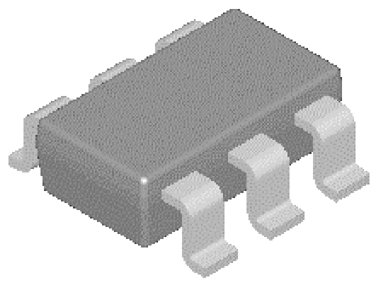
SSOT-6 Reel Configuration: Figure 4.0

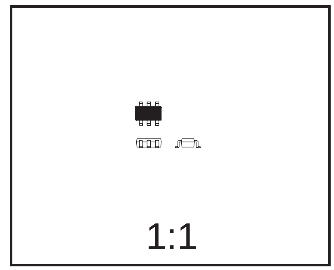


Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 – 0.429 7.9 – 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 – 0.429 7.9 – 10.9

SuperSOT™-6 Tape and Reel Data and Package Dimensions, continued

SuperSOT -6 (FS PKG Code 31, 33)

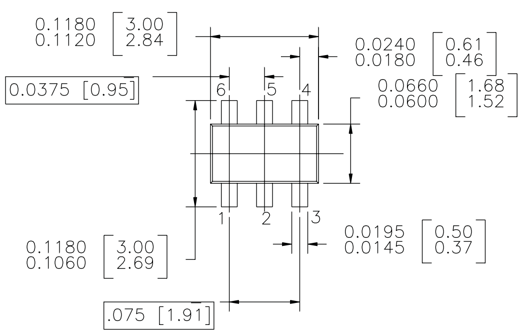


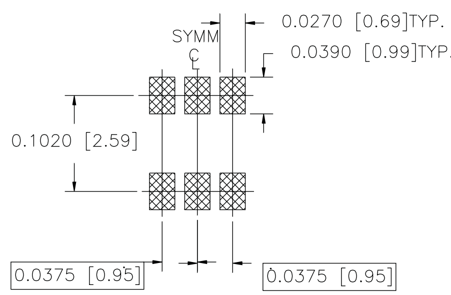


Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

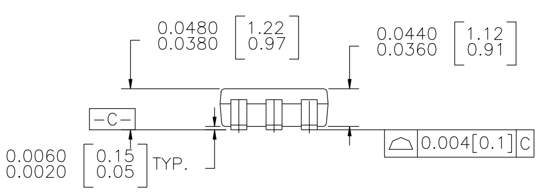
Part Weight per unit (gram): 0.0158

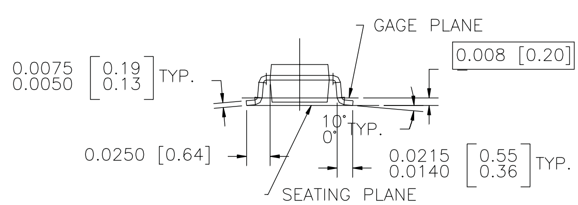




LAND PATTERN RECOMMENDATION

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS





NOTES : UNLESS OTHERWISE SPECIFIED

1.0 STANDARD LEAD FINISH : 150 MICROINCHES 93.81 MICROMETERS)
MINIMUM TIN / LEAD (SOLDER) ON COPPER.

2.0 NO JEDEC REGISTRATION AS OF JULY 1996

SUPER SOT 6 LEADS

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FACT™	QFET™	
FACT Quiet Series™	QS™	
FAST®	Quiet Series™	
FASTr™	SuperSOT™-3	
GTO™	SuperSOT™-6	
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