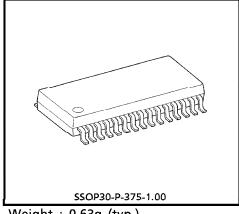
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT MULTI-CHIP

TA8490F

3-PHASE FULL WAVE BRUSHLESS DC MOTOR DRIVER IC FOR **CD-ROM DRIVES**

This 3-phase, full-wave, brushless DC motor driver IC has been developed for use in CD-ROM drive spindle motors. The TA8490F contains in its upper stage a discrete power transistor which, thanks to its low-saturation characteristic, enables the IC to provide superior thermal efficiency.

Furthermore, the multi-chip structure of this device facilitates dispersion of the heat generated inside the package, making it possible to suppress heat concentration.



Weight: 0.63g (typ.)

FEATURES

- Multi-chip structure (3 RN6006 chips built-in)
- 3-phase, full-wave, semi-linear drive
- Current drive / current control
- Built-in current limiter : $I_{IIM} = 0.6A$ (typ.) (at $R_F = 0.3\Omega$)
- Built-in reversing brake/short brake functions
- FG signal output (using hall element output signal)
- Built-in switching regulator controller
- Built-in hall bias
- Built-in thermal shutdown circuit
- Package: MFP-30

operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

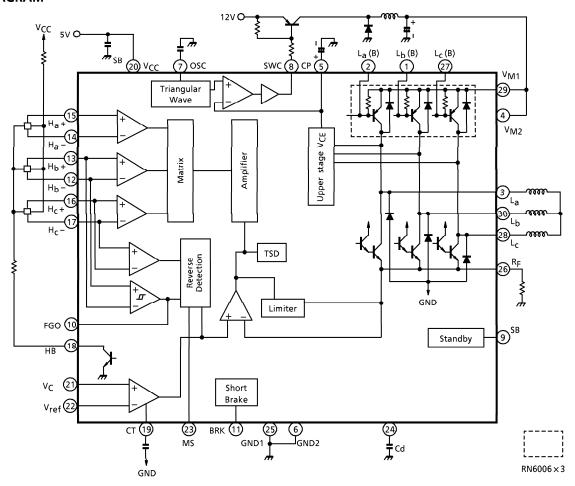
The products described in this document are subject to foreign exchange and foreign trade control laws.

The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.

The information contained herein is subject to change without notice.

TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions

BLOCK DIAGRAM



PIN ASSIGNMENT

TERMINAL No.	TERMINAL SYMBOL	FUNCTION	REMARKS
1	L _b (B)	b-phase upper side power transistor (base) output terminal	Keep open.
2	L _a (B)	a-phase upper side power transistor (base) output terminal	Keep open.
3	L _a	a-phase output terminal	Connect to the coil.
4	V_{M2}	Supply voltage terminal for motor drive	Connect to V _{M1} externally.
5	СР	Switching power source system phase compensator terminal	Connect a capacitor between this terminal and GND.
6	GND2	GND	_
7	OSC	Triangular wave oscillation terminal	Connect a capacitor between this terminal and GND.
8	SWC	Switching regulator control signal output terminal	Connect to the base of the switching external transistor.
9	SB	RUN/STOP control terminal	H: RUN, L: STOP
10	FGO	FG amplifier output terminal	Outputs a signal whose frequency is determined by the CD rotation frequency.
11	BRK	Brake mode select terminal	Output mode when V _C >V _{ref}
12	H _b ⁻	b-phase negative hall signal input terminal	Connect to hall element output terminal.
13	H _b +	b-phase positive hall signal input terminal	Connect to hall element output terminal.
14	H _a -	a-phase negative hall signal input terminal	Connect to hall element output terminal.
15	H _a +	a-phase positive hall signal input terminal	Connect to hall element output terminal.
16	H _C ⁺	c-phase positive hall signal input terminal	Connect to hall element output terminal.
17	H _C -	a-phase negative hall signal input terminal	Connect to hall element output terminal.
18	НВ	Hall element bias terminal	Open collector output. Connect to the negative side of hall element bias line.
19	СТ	Control system phase compensator terminal	Connect a capacitor between this terminal and GND.
20	V _C C	Supply voltage terminal for control circuits	V _{CC} (opr) = 4.5~5.5V

TERMINAL No.	TERMINAL SYMBOL	FUNCTION	REMARKS
21	٧c	Control amplifier input terminal	Use the control signal as input.
22	V _{ref}	Control amplifier reference voltage input terminal	Use the reference voltage for the control amplifier as input.
23	MS	Mode select terminal	Determines output mode.
24	Cd	Forward / reverse changeover gain adjustment terminal	Adjust a rotation direction changeover gain
25	GND1	GND	_
26	R _F	Output current detection terminal	Sets limiter current value and current gain.
27	L _C (B)	c-phase upper side power transistor (base) output terminal	Keep open.
28	L _C	c-phase output terminal	Connect to the coil.
29	V _{M1}	Supply voltage terminal for motor drive	Connect to V _{M2} externally.
30	Lb	b-phase output terminal	Connect to the coil.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V _C C	7	V
Fower supply voltage	٧M	16	\ \ \
Output Current	Ō	1.2	Α
Power Dissipation	P _D (Note 1)	1.0	W
Junction Temperature	Tj	150	°C
Operating Temperature	T _{opr}	- 20∼75	°C
Storage Temperature	T _{stg}	- 55∼150	°C

(Note 1) unmounted

OPERATING VOLTAGE RANGE

CHARACTERISTIC	SYMBOL	OPERATING RANGE	UNIT	
Bower Supply Voltage	Vcc	4.5~5.5	V	
Power Supply Voltage	٧ _M	3~14	V	

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $V_{M} = 12V$, Ta = 25°C)

CH	ARACTERISTIC	SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	
Supply Voltage		l _{CC1}	1	Stop mode	_	2	4.5	A	
Supply V	orrage	lCC2	'	Run mode, output open	_	7	15	mA	
	Input Current	INH		V _{CMRH} = 2.5V	_	_	2	μΑ	
Hall Amp	Common Mode Input Voltage Range	V _{CMRH}	2	_	1.5	_	4.0	٧	
	Input Amplitude	VΗ	_	_	60	_	_	mV _{p-p}	
Hall Elem Voltage	nent Bias Saturation	V _{HB}	2	I _{HB} = 10mA	_	1.3	2.0	V	
	Common Mode Input Voltage Range	VCMRC	2	_	1.0	_	4.0	٧	
	Input Current	INC	2	V _C = V _{ref} = 2.5V	_	_	5.0	μΑ	
Control Amp.	Dead Zone Voltage Width	V _{DZ}	_	$V_{REF} = 2.5V$, $R_F = 0.3\Omega$	_	100	_	mV	
	Input Offset Voltage	△VOFF (F)	3	CW mode, $V_{ref} = 2.5V$, $R_F = 0.3\Omega$	20	50	150	mV	
		△VOFF (R)	3	CCW mode, $V_{ref} = 2.5V$, $R_F = 0.3\Omega$	20	50	150	IIIV	
Current Limit Am	p. Limit Current	^I LIM	3	$R_F = 0.3\Omega$	480	600	720	mΑ	
RUN/	Input Voltage (H)	V _{INS} (H)		(RUN)	3.0	_	Vcc	V	
STOP	Input Voltage (L)	V _{INS} (L)	1	(STOP)	GND	_	1.0)	
Control Circuit	Input Current	INS (L)	!	V _{INS} = GND	_	_	1	μΑ	
	Saturation Voltage (Upper Side)	V _{sat} (U)	4	I _O = 0.6A	_	0.1	1.3	\ \ \	
Output	Saturation Voltage (Lower Side)	V _{sat (L)}	4	I _O = 0.6A	_	0.6	1.0		
Circuit	Cut-off Current (Upper Side)	^I L (U)	5	V _L = 16V	_	_	10		
	Cut-off Current (Lower Side)	I _L (L)	5	V _L = 16V	_		10	μΑ	
Mode	Input Voltage (H)	V _{IMS (H)}	6	CCW mode V _C >V _{ref} , BRK : L	3.0	l	VCC	\	
Select Circuit	Input Voltage (L)	V _{MS} (L)	6	Reversing brake mode V _C >V _{ref} , BRK : L	_		0.5		
	Input Current	INMS	6	V _{MS} = GND	_		1	μΑ	

CHA	RACTERISTIC	SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	
	Hysteresis Voltage	V_{HYS}	6	_	5	20	45	mV _{p-p}	
FG	Output Voltage (H)	V _{OFG} (H)	7	Source current : $10\mu A$	V _C C - 0.5		_	v	
Amp.	Output Voltage (L)	V _{OFG} (L)	7	Sink current : 10μA	_		0.5		
Short	Input Voltage (H)	V _{BRK} (H)	6	_	3.0		V _C C	v	
Brake Circuit	Input Voltage (L)	V _{BRK} (L)	6	_	_	_	0.5		
	Input Current	INBRK	6	V _{BRK} = GND	_	_	1	μΑ	
Triangula	Oscillation r Frequency	fosc	_	C = 250pF (Note)	_	100	_	kHz	
Oscillation	Charge Current	losc [†]	7	V _{OSC} = 1.8V	50	100	200	μΑ	
Circuit	Discharge Current	losc =	7	V _{OSC} = 3.2V	- 200	- 100	- 50	μΑ	
SW-REG Control Circuit	Saturation Voltage	V _{sat-sw}	8	I _{SW} = 20mA	_	1.0	3.0	V	
Thermal Shut-down Operating Temperature		T _{SD}		Junction temperature (according to design specification) (Note)	_	175		°C	

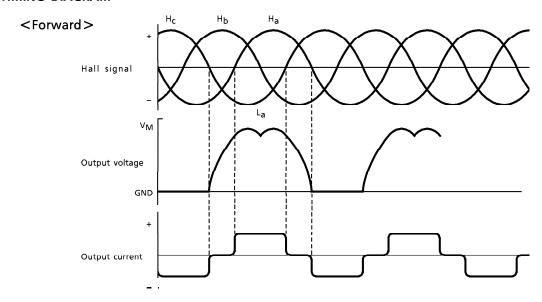
(Note) this is not tested.

FUNCTION TABLE

			FORWARD				REVERSE	
Ha	H _b	H _C	L _a	Lb	L _C	L _a	Lb	L _C
Н	L	L	Н	L	М	L	Н	М
Н	Н	L	Н	М	L	L	М	Н
L	Н	L	М	Н	L	М	L	Н
L	Н	Н	L	Н	М	Н	L	М
L	L	Н	L	М	Н	Н	M	L
Н	L	Н	М	L	Н	М	Н	L

 $\begin{array}{lll} <& Forward > & <& Reverse > \\ L_a = -(H_c - H_a) & L_a = (H_c - H_a) \\ L_b = -(H_a - H_b) & L_b = (H_a - H_b) \\ L_c = -(H_b - H_c) & L_c = (H_b - H_c) \end{array}$

TIMING DIAGRAM

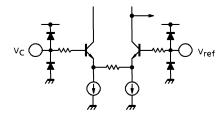


FUNCTIONAL DESCRIPTION

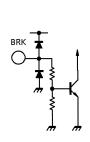
This IC is a 3-phase, full-wave brushless DC motor driver of the current-control/current-drive type. It contains in its upper stage a PNP discrete power transistor, which, because of the Multi-Chip Package (MCP) structures provides high torque and thermal efficiency.

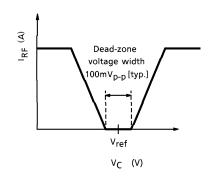
In addition, when combined with a switching regulator, its efficiency can be increased still further.

• Control amp input circuit



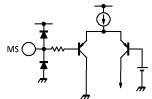
The Common mode input voltage ranges for both V_C and V_{ref} are 1.0 to 4.0V. The control input-to-drive output gain is 1.0A/V (typ.), whose characteristic is shown below. The input is provided with a dead-zone area whose voltage width is 100mV (typ.).

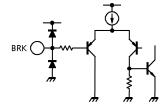




$$g_{m} = \frac{\Delta I_{RF}}{\Delta V_{C}} = 1.0 \text{ [A/V] (typ.)} \text{ (at } R_{F} = 0.3\Omega)$$

• Mode select/short brake circuit





When V_C>V_{ref}, one of three modes (Reverse Rotation, Reversing Brake or Short Brake mode) can be selected by setting the MS and BRK pins appropriately.

<Function>

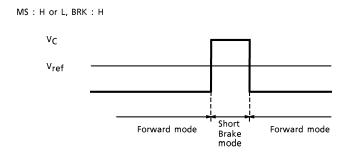
$V_C < V_{ref}$							
BRK							
		Н	L				
MS	Н	Forward	Forward				
IVIS	L	Forward	Forward				

$V_C > V_{ref}$						
		BF	₹K			
		Н	L			
MS	Н	Short	Reverse			
	П	brake	Reverse			
		Short	Reversing			
	_	brake	brake			

In Short Brake mode, the upper-stage power transistor is turned on and the lower-stage power transistor is turned off.

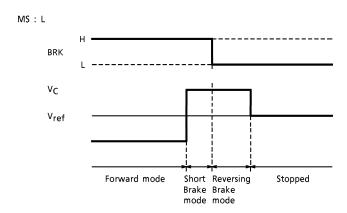
In Reversing Brake mode, all outputs are cut off after detection of reverse rotation, causing the motor to stop.

(Short brake)



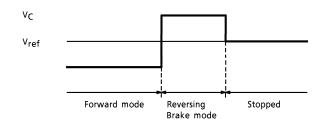
(Reversing brake)

① When stopping the motor by applying a reversing brake after a short brake



2 When stopping the motor using Reversing Brake mode

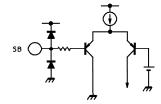
MS: L, BRK: L



(*) For an explanation of the Reversing Brake mode stopping sequence, refer to the explanation of the reverse rotation detection circuit.

The short brake generates less heat than the reversing brake. Therefore Toshiba recommends a combined use of the short and reversing brakes when stopping the motor.

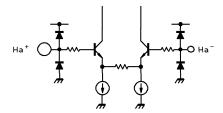
• Run/stop control circuit



When the driver IC is standing by, all of its circuits except the FG amp and the hall amp are turned off.

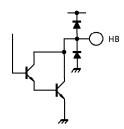
H: start
L: standby

• Hall amp circuit



The common mode input voltage range for V_{CMRH} is 1.5 to 4.0V.

• Hall element bias circuit



The hall element bias current is turned off when the driver IC is in standby state.

Make sure that the negative hall bias line is connected to the HB pin.

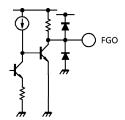
The remaining voltage is as follows:

$$V_{HB} = 1.2 [V] (typ.)$$
 at $I_{HB} = 10 mA$

Furthermore, this circuit cannot be used if FG output is necessary in standby state.

When the HB terminal is not used, the negative hall bias line must be connected to GND with a resistor in between.

• FG amp circuit



This circuit uses a hall element signal which is output to FGO after a Schmitt stage.

The FG amp has a hysteresis of 20 $[mV_{p-p}]$ (typ.) and its output voltages are

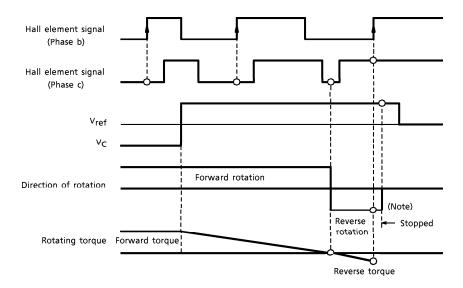
High level : $V_{CC} - 0.5 \sim V_{CC}$ [V]

Low level : GND~0.5 [V] at IOFG = 10μ A

The FG amp is active when it is in standby state. When the hall element signal is input, the FG signal is output.

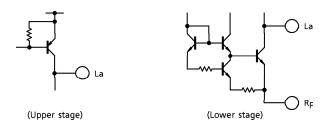
• Reverse rotation detection circuit

By comparing the two phases of the Hall element signal, this circuit detects a state where the phases are inverted, at which time the torque is reduced to 0. The detection accuracy is determined by the number of pulses per rotation of Hall element output.



(Note) Due to its inertial force, the motor does not stop immediately after the torque is reduced to 0.

• Output circuit



This circuit uses the power transistor's base current to regulate the circuit's output current. The upper-stage power transistor consists of a PNP discrete transistor (RN6006), which gives high torque efficiency.

• Current limiter circuit

The current limit value is determined by the equation below.

$$I_{LIM} = \frac{0.24}{R_F + 0.1}$$
 [A] (typ.)

• Triangular wave oscillator circuit

Triangular waves are generated by connecting a capacitor between the OSC pin and GND. The charging / discharging currents are $\pm 50\mu$ A, and the oscillation frequency is as follows :

$$f_{OSC} = \frac{100 (\mu A)}{2 \times C (pF)} [Hz]$$



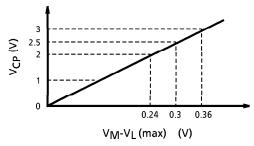
Taking into account efficiency considerations and the effects of noise, Toshiba recommends using the IC with an oscillation frequency of more or less 100kHz.

• V_M output voltage (3-phase maximum) detection circuit

This circuit selects the highest voltage from the three phases of output voltages and then outputs the voltage difference between the selected voltage and V_M as a voltage referenced to GND (V_{CE} for the upper output stage).

This voltage is filtered by a capacitor at the CP pin and compared with the triangular wave before being output on the SWC pin.

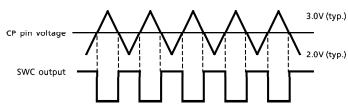
When using a switching regulator, the driver IC operates in a closed loop with a V_{CE} of 0.3V (typ.) for the upper output stage.



Switching regulator control signal output circuit

This circuit outputs the result of comparison between V_{CE} for the upper stage and the triangular wave from one of the open-collector output terminals. By controlling an external PNP transistor in this way, the circuit controls V_{M} .

The output function is as follows:



Thermal shut down circuit

This circuit turns off output when $T_i = 175^{\circ}C$ (typ.) (according to design specification).

EXTERNAL PARTS

TERMINAL No.	FUNCTION	RECOMMENDED VALUE	REMARKS
C ₁	Control system phase correction	0.01 <i>μ</i> F	Note 1
C ₂	Triangular wave oscillation	250pF	See Page 12.
C ₃	Power supply line oscillation prevention	0.22 μ F	_
C ₄	Filter	1 μ F (Electrolytic capacitor)	Note 2
C ₅	Forward / reverse changeover gain adjustment	0.01μF	Note 3
c ₆	For switching regulator	100 μ F (Electrolytic capacitor)	_
R ₁	Hall element bias	_	Note 4
R ₂	Control amp reference voltage	_	Note 5
R ₃	Output current detection	0.3Ω	See Page 11.
R ₄	Base current control for switching regulator PNP transistor	1kΩ	Note 6
R ₅	Leakage absorption of switching regulator PNP transistor	10k Ω	Note 7
L ₁	For switching regulator	68/4H	_

- Note 1: Check carefully to see that there is no output oscillation.
- Note 2: This is used to filter the output of the difference between the three-phase output voltage and $V_{\mbox{\scriptsize M}}$.
- Note 3: This is used to adjust the rotation direction changeover gain.

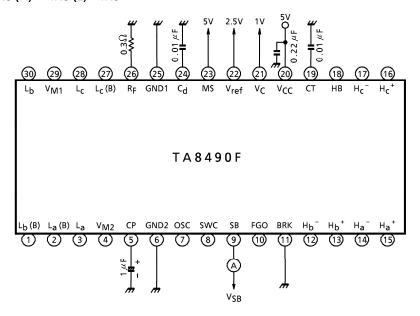
 The capacitance valve and the gain are in inverse.

 This capacitance is to prevent from output through current.
- Note 4: Be sure to set this bias so that the hall element output amplitude and common mode input voltage fall within the ranges specified in the table of electrical characteristics.
- Note 5: This voltage must be set to fall within the Common mode input voltage range of the control amp. Toshiba recommends setting it to $V_{CC/2}$. Also, consider the Vref pin's input current: $1.3\mu A$ (typ.) (when $V_C \ll V_{ref}$) when setting the resistance value.
- Note 6: The SWC pin is an open-collector, so that when the internal transistor saturates, its switching characteristic is degraded. Toshiba recommends that when SWC is low, its pin voltage should be 2V or above.
- Note 7: The external PNP transistor used for the switching regulator has its offset voltage determined by this resistance. Use a resistance of between several $k\Omega$ and $10k\Omega$ according to the switching characteristics.

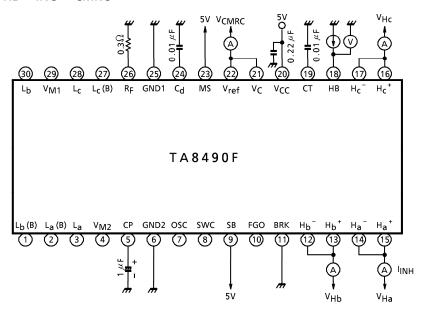
(*) Tr.1 : 2SA1241 D1 : U1GWJ44

TEST CIRCUIT

1. ICC1, ICC2, VINS (H), VINS (L), IINS



2. I_{INH}, I_{CMRH}, V_{HB}, I_{INC}, V_{CMRC}



• I_{INH} : Total of a phase negative and positive input current.

 $V_{Ha} = V_{Hb} = V_{Hc} = 2.5V$

• V_{CMRH} : Measure the I_{INH} gap between $V_{Ha} = 1.5V$ and $V_{Ha} = 4.0V$.

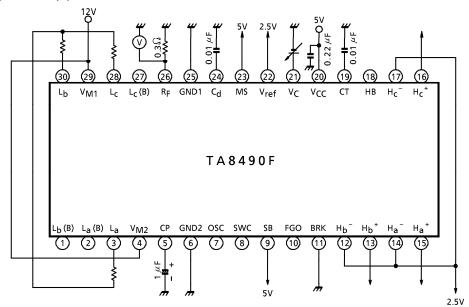
b and c phase are measured the same method.

• V_{HB} : $I_{HB} = 10 \text{mA}$

• V_{INC} : Total of V_C and V_{ref} input current. At $V_{CMRC} = 2.5V$.

V_{CMRC}: Measure the I_{INC} gap between V_{CMRC} = 1.0V and V_{CMRC} = 4.0V.

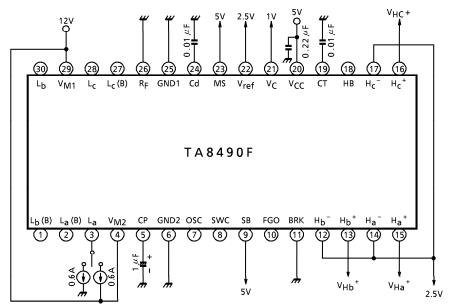
3. $\Delta V_{OFF}(F)$, $\Delta V_{OFF}(R)$, I_{LIM}



• $\Delta V_{OFF}(F)$: Measure V_{RF} at $V_{C} = 2.48 V / 2.35 V$. • $\Delta V_{OFF}(R)$: Measure V_{RF} at $V_{C} = 2.52 V / 2.65 V$.

• I_{LIM} : Change to current value after measuring V_{RF} at $V_{C} = 1.0V$

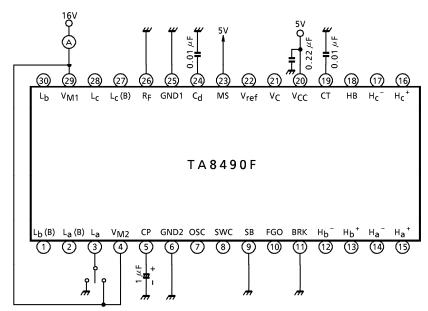
4. V_{sat} (U), V_{sat} (L)



V_{sat} (U) : Determined output function by V_{Ha}⁺, V_{Hb}⁺, V_{Hc}⁺ (2.4V / 2.6V).
 Measure voltage value between V_M and L_a. b phase and c phase are measured the same method.

V_{sat (L)}: Determined output function by V_{Ha}⁺, V_{Hb}⁺, V_{Hc}⁺ (2.4V/2.6V).
 Measure voltage value between L_a and GND. b phase and c phase are measured the same method.

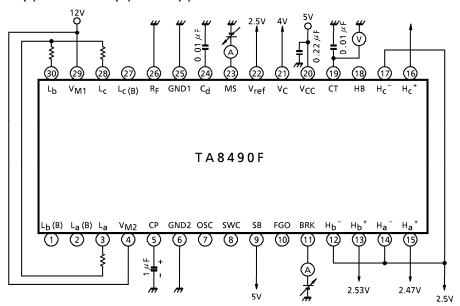
5. IL (U), IL (L)



 I_L(U): Measure I_M when L_a and GND are shortted. b phase and c phase are measured the same method.

 I_L (L) : Measure I_M when V_M and L_a are shortted. b phase and c phase are measured the same method.

6. VMS (H), VMS (L), IINS, VBRK (H), VBRK (L), IINBRK



V_{MS} (H): V_{MS} = 3.0V, V_{BRK} = 0V, verify that output function is reverse mode.

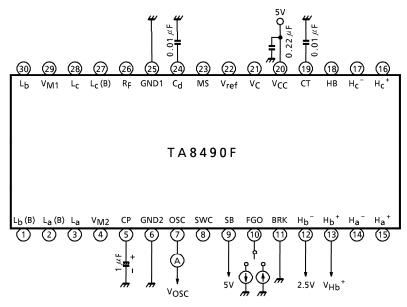
• $V_{MS}(L)$: $V_{MS} = 0.5V$, $V_{BRK} = 0V$, verify that $V_{CT} = 0V$

I_{MS} (L) : V_{MS} = 0V , V_{BRK} = 0V

• $V_{BRK}(H)$: $V_{MS} = 5V$, $V_{BRK} = 3.0V$, verify that $L_a = L_b = L_c$: H

• V_{BRK} (L): V_{MS} = 5V, V_{BRK} = 0.5V, verify that output function is reverse mode.

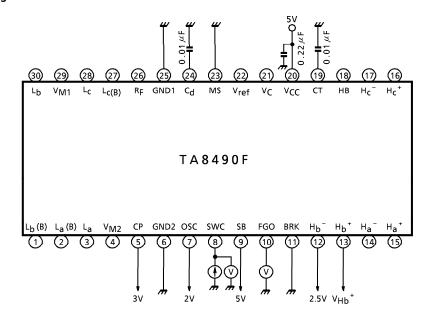
7. VOFG (H), VOFG (L), IOSC⁺, IOSC⁻



• VOFG (H): VHb⁺ = 2.53V, IFGO = 10μ A (source) • VOFG (L): VHb⁺ = 2.47V, IFGO = 10μ A (sink)

IOSC⁺ : VOSC = 2V
 IOSC⁻ : VOSC = 3V

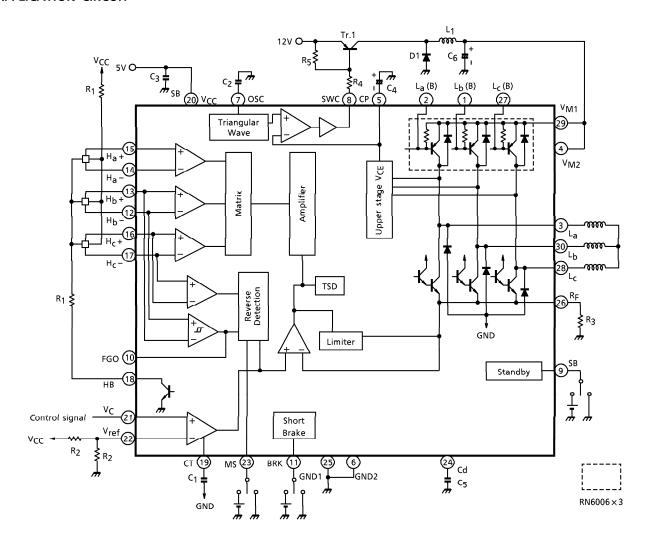
8. V_{sat-sw}, V_{HYS}



• V_{sat-sw} : $I_{swc} = 20mA$

VHYS
 Switch the VHb⁺ from high (H) to low (L) and from L to H.
 Measure the VHb⁺ at the point when FGO function changes.

APPLICATION CIRCUIT



Weight: 0.63g (Typ.)

0.92±0.2