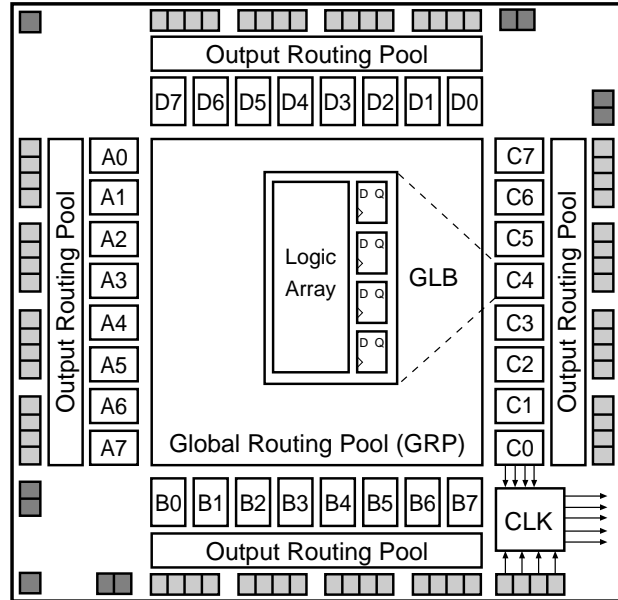


## Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - High Speed Global Interconnect
  - 6000 PLD Gates
  - 64 I/O Pins, Eight Dedicated Inputs
  - 192 Registers
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Fast Random Logic
  - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E<sup>2</sup>C<sup>2</sup>MOS<sup>®</sup> TECHNOLOGY**
  - $f_{max} = 60$  MHz Maximum Operating Frequency
  - $t_{pd} = 20$  ns Propagation Delay
  - TTL Compatible Inputs and Outputs
  - Electrically Erasable and Reprogrammable
  - Non-Volatile E<sup>2</sup>C<sup>2</sup>MOS Technology
  - 100% Tested
- **IN-SYSTEM PROGRAMMABLE**
  - In-System Programmable<sup>™</sup> (ISP<sup>™</sup>) 5-Volt Only
  - Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality
  - Reprogram Soldered Devices for Faster Prototyping
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - Complete Programmable Device Can Combine Glue Logic and Structured Designs
  - Four Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Flexible Pin Placement
  - Optimized Global Routing Pool Provides Global Interconnectivity
- **ispDesignEXPERT<sup>™</sup> – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - Superior Quality of Results
  - Tightly Integrated with Leading CAE Vendor Tools
  - Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER<sup>™</sup>
  - PC and UNIX Platforms

## Functional Block Diagram



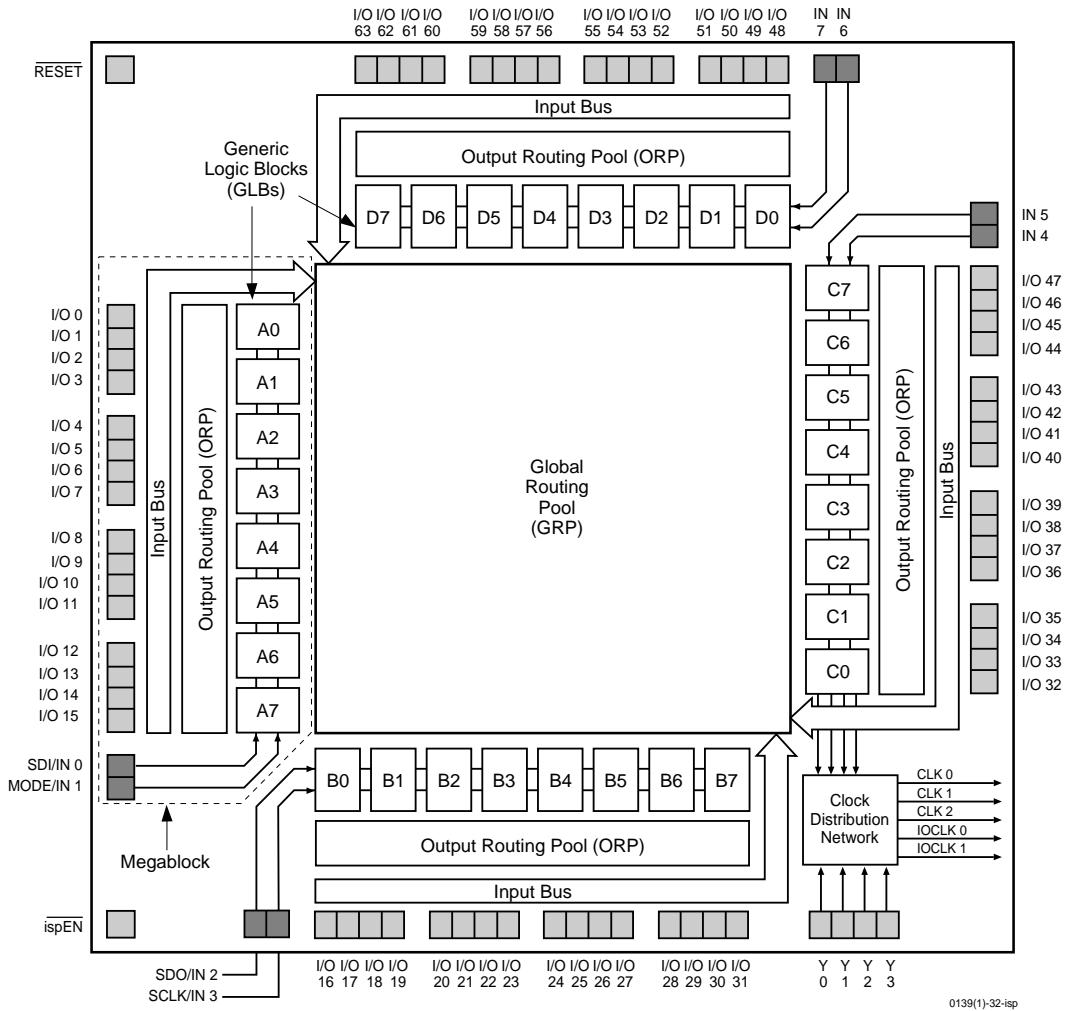
## Description

The ispLSI 1032/883 is a High-Density Programmable Logic Device processed in full compliance to MIL-STD-883. This military grade device contains 192 Registers, 64 Universal I/O pins, eight Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1032/883 features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 1032/883 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7 (see figure 1). There are a total of 32 GLBs in the ispLSI 1032/883 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

**Functional Block Diagram**

Figure 1. ispLSI 1032/883 Functional Block Diagram



The device also has 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The I/O cells within the Megablock also share a common Output Enable (OE) signal. The ispLSI 1032/883 device contains four of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 1032/883 device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (C0 on the ispLSI 1032/883 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

**Absolute Maximum Ratings <sup>1</sup>**

Supply Voltage  $V_{CC}$  ..... -0.5 to +7.0V  
 Input Voltage Applied ..... -2.5 to  $V_{CC} + 1.0V$   
 Off-State Output Voltage Applied ..... -2.5 to  $V_{CC} + 1.0V$   
 Storage Temperature ..... -65 to 150°C  
 Case Temp. with Power Applied ..... -55 to 125°C  
 Max. Junction Temp. ( $T_J$ ) with Power Applied ... 150°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

**DC Recommended Operating Conditions**

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
$V_{CC}$	Supply Voltage	Military/883 $T_C = -55^\circ C$ to $+125^\circ C$	4.5	5.5	
$V_{IL}$	Input Low Voltage		0	0.8	V
$V_{IH}$	Input High Voltage		2.0	$V_{CC} + 1$	V

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**Capacitance ( $T_A=25^\circ C$ ,  $f=1.0$  MHz)**

SYMBOL	PARAMETER	MAXIMUM <sup>1</sup>	UNITS	TEST CONDITIONS
$C_1$	Dedicated Input Capacitance	10	pf	$V_{CC}=5.0V$ , $V_{IN}=2.0V$
$C_2$	I/O and Clock Capacitance	10	pf	$V_{CC}=5.0V$ , $V_{I/O}$ , $V_Y=2.0V$

1. Characterized but not 100% tested.

Table 2- 0006mil

**Data Retention Specifications**

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	—	Years
Erase/Reprogram Cycles	10000	—	Cycles

Table 2- 0008B

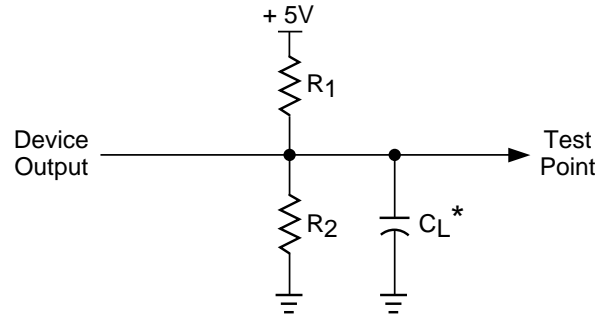
**Switching Test Conditions**

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

Table 2- 0003

**Figure 2. Test Load**



\*CL includes Test Fixture and Probe Capacitance.

**Output Load Conditions (see figure 2)**

Test Condition		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at $V_{OH} - 0.5V$	∞	390Ω	5pF
	Active Low to Z at $V_{OL} + 0.5V$	470Ω	390Ω	5pF

**DC Electrical Characteristics**

**Over Recommended Operating Conditions**

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. <sup>3</sup>	MAX.	UNITS
<b>VOL</b>	Output Low Voltage	$I_{OL} = 8 \text{ mA}$	–	–	0.4	V
<b>VOH</b>	Output High Voltage	$I_{OH} = -4 \text{ mA}$	2.4	–	–	V
<b>IIL</b>	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	–	–	-10	μA
<b>IIH</b>	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	–	–	10	μA
<b>IIL-isp</b>	isp Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	–	–	-150	μA
<b>IIL-PU</b>	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$	–	–	-150	μA
<b>IOS1</b>	Output Short Circuit Current	$V_{CC} = 5V, V_{OUT} = 0.5V$	–	–	-200	mA
<b>ICC<sup>2,4</sup></b>	Operating Power Supply Current	$V_{IL} = 0.5V, V_{IH} = 3.0V$ $f_{TOGGLE} = 1 \text{ MHz}$	–	135	220	mA

1. One output at a time for a maximum duration of one second.  $V_{out} = 0.5V$  was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using six 16-bit counters.
3. Typical values are at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$ .
4. Maximum  $I_{CC}$  varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum  $I_{CC}$ .

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**External Timing Parameters**

**Over Recommended Operating Conditions**

PARAMETER	TEST <sup>5</sup> COND.	# <sup>2</sup>	DESCRIPTION <sup>1</sup>	-60		UNITS
				MIN.	MAX.	
t <sub>pd1</sub>	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	-	20	ns
t <sub>pd2</sub>	A	2	Data Propagation Delay, Worst Case Path	-	25	ns
f <sub>max</sub> (Int.)	A	3	Clock Frequency with Internal Feedback <sup>3</sup>	60	-	MHz
f <sub>max</sub> (Ext.)	-	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	38	-	MHz
f <sub>max</sub> (Tog.)	-	5	Clock Frequency, Max Toggle <sup>4</sup>	83	-	MHz
t <sub>su1</sub>	-	6	GLB Reg. Setup Time before Clock, 4PT bypass	9	-	ns
t <sub>co1</sub>	A	7	GLB Reg. Clock to Output Delay, ORP bypass	-	13	ns
t <sub>h1</sub>	-	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	-	ns
t <sub>su2</sub>	-	9	GLB Reg. Setup Time before Clock	13	-	ns
t <sub>co2</sub>	-	10	GLB Reg. Clock to Output Delay	-	16	ns
t <sub>h2</sub>	-	11	GLB Reg. Hold Time after Clock	0	-	ns
t <sub>r1</sub>	A	12	Ext. Reset Pin to Output Delay	-	22.5	ns
t <sub>rw1</sub>	-	13	Ext. Reset Pulse Duration	13	-	ns
t <sub>en</sub>	B	14	Input to Output Enable	-	24	ns
t <sub>dis</sub>	C	15	Input to Output Disable	-	24	ns
t <sub>wh</sub>	-	16	Ext. Sync. Clock Pulse Duration, High	6	-	ns
t <sub>wl</sub>	-	17	Ext. Sync. Clock Pulse Duration, Low	6	-	ns
t <sub>su5</sub>	-	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.5	-	ns
t <sub>h5</sub>	-	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	8.5	-	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit counter using GRP feedback.
4. f<sub>max</sub> (Toggle) may be less than 1/(t<sub>wh</sub> + t<sub>wl</sub>). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Table 2-0030-32/60C

**Internal Timing Parameters<sup>1</sup>**

PARAMETER	# <sup>2</sup>	DESCRIPTION	-60		UNITS
			MIN.	MAX.	
<b>Inputs</b>					
<b>t</b> iobp	20	I/O Register Bypass	–	2.7	ns
<b>t</b> iolat	21	I/O Latch Delay	–	4.0	ns
<b>t</b> iosu	22	I/O Register Setup Time before Clock	7.3	–	ns
<b>t</b> ioh	23	I/O Register Hold Time after Clock	1.3	–	ns
<b>t</b> ioco	24	I/O Register Clock to Out Delay	–	4.0	ns
<b>t</b> ior	25	I/O Register Reset to Out Delay	–	3.3	ns
<b>t</b> din	26	Dedicated Input Delay	–	5.3	ns
<b>GRP</b>					
<b>t</b> grp1	27	GRP Delay, 1 GLB Load	–	2.0	ns
<b>t</b> grp4	28	GRP Delay, 4 GLB Loads	–	2.7	ns
<b>t</b> grp8	29	GRP Delay, 8 GLB Loads	–	4.0	ns
<b>t</b> grp12	30	GRP Delay, 12 GLB Loads	–	5.0	ns
<b>t</b> grp16	31	GRP Delay, 16 GLB Loads	–	6.0	ns
<b>t</b> grp32	32	GRP Delay, 32 GLB Loads	–	10.6	ns
<b>GLB</b>					
<b>t</b> 4ptbp	33	4 Product Term Bypass Path Delay	–	8.6	ns
<b>t</b> 1ptxor	34	1 Product Term/XOR Path Delay	–	9.3	ns
<b>t</b> 20ptxor	35	20 Product Term/XOR Path Delay	–	10.6	ns
<b>t</b> xoradj	36	XOR Adjacent Path Delay <sup>3</sup>	–	12.7	ns
<b>t</b> gbp	37	GLB Register Bypass Delay	–	1.3	ns
<b>t</b> gsu	38	GLB Register Setup Time before Clock	1.3	–	ns
<b>t</b> gh	39	GLB Register Hold Time after Clock	6.0	–	ns
<b>t</b> gco	40	GLB Register Clock to Output Delay	–	2.7	ns
<b>t</b> gr	41	GLB Register Reset to Output Delay	–	3.3	ns
<b>t</b> ptre	42	GLB Product Term Reset to Register Delay	–	13.3	ns
<b>t</b> ptoe	43	GLB Product Term Output Enable to I/O Cell Delay	–	12.0	ns
<b>t</b> ptck	44	GLB Product Term Clock Delay	4.6	9.9	ns
<b>ORP</b>					
<b>t</b> orp	45	ORP Delay	–	3.3	ns
<b>t</b> orpbp	46	ORP Bypass Delay	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.  
 2. Refer to Timing Model in this data sheet for further details.  
 3. The XOR Adjacent path can only be used by Lattice Hard Macros.

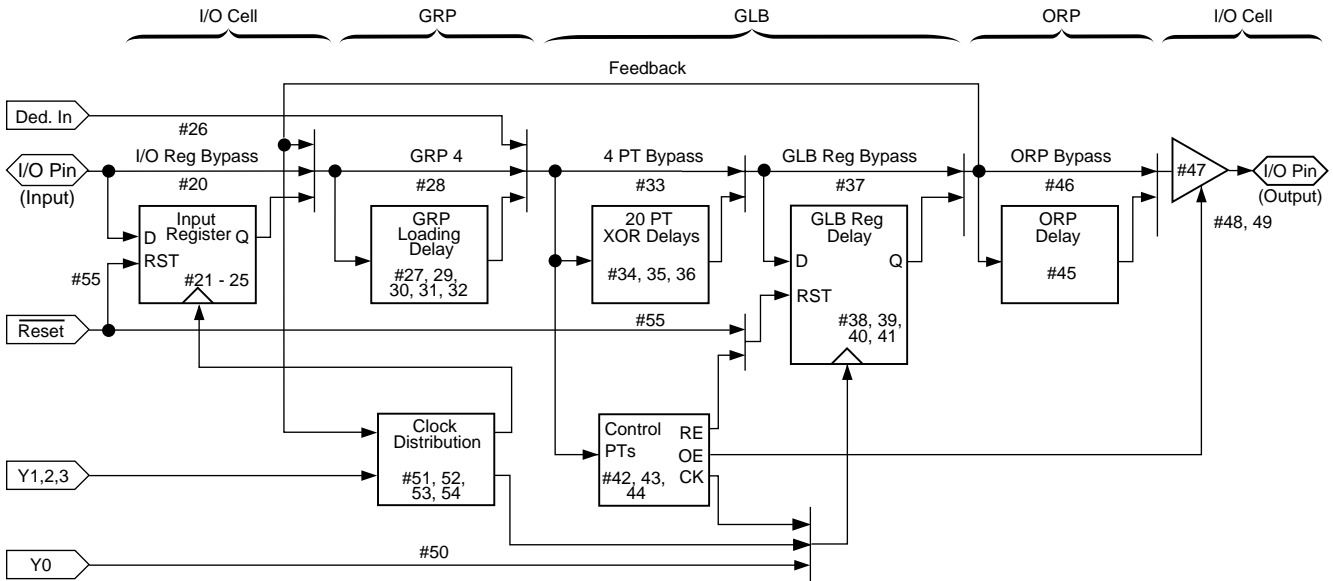
**Internal Timing Parameters<sup>1</sup>**

PARAMETER	# <sup>2</sup>	DESCRIPTION	-60		UNITS
			MIN.	MAX.	
<b>Outputs</b>					
<b>t<sub>ob</sub></b>	47	Output Buffer Delay	–	4.0	ns
<b>t<sub>oen</sub></b>	48	I/O Cell OE to Output Enabled	–	6.7	ns
<b>t<sub>odis</sub></b>	49	I/O Cell OE to Output Disabled	–	6.7	ns
<b>Clocks</b>					
<b>t<sub>gy0</sub></b>	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.0	6.0	ns
<b>t<sub>gy1/2</sub></b>	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.6	7.3	ns
<b>t<sub>gcp</sub></b>	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
<b>t<sub>ioy2/3</sub></b>	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	4.6	7.3	ns
<b>t<sub>iocp</sub></b>	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
<b>Global Reset</b>					
<b>t<sub>gr</sub></b>	55	Global Reset to GLB and I/O Registers	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.

2. Refer to Timing Model in this data sheet for further details.

**ispLSI 1032/883 Timing Model**



**Derivations of  $t_{su}$ ,  $t_h$  and  $t_{co}$  from the Product Term Clock<sup>1</sup>**

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)}) \\
 &= (\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44) \\
 7.3 \text{ ns} &= (2.7 + 2.7 + 10.6) + (1.3) - (2.7 + 2.7 + 4.6) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35) \\
 5.3 \text{ ns} &= (2.7 + 2.7 + 9.9) + (6.0) - (2.7 + 2.7 + 10.6) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47) \\
 25.3 \text{ ns} &= (2.7 + 2.7 + 9.9) + (2.7) + (3.3 + 4.0)
 \end{aligned}$$

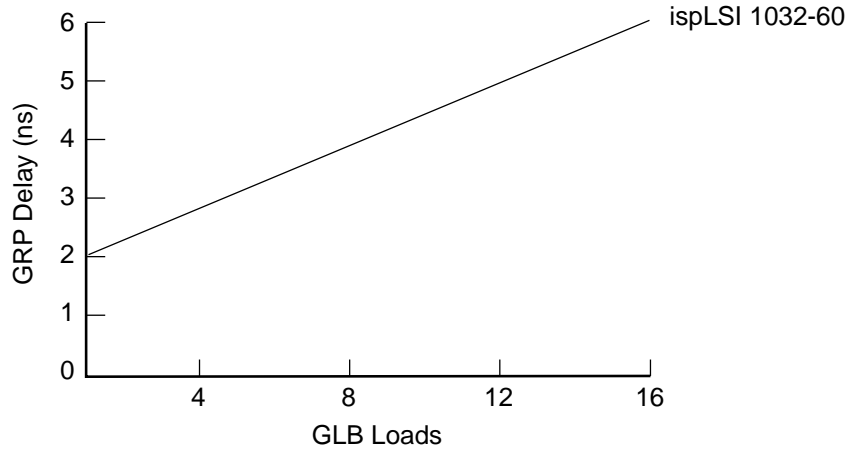
**Derivations of  $t_{su}$ ,  $t_h$  and  $t_{co}$  from the Clock GLB<sup>1</sup>**

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)}) \\
 &= (\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52) \\
 7.3 \text{ ns} &= (2.7 + 2.7 + 10.6) + (1.3) - (6.0 + 2.7 + 1.3) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35) \\
 5.3 \text{ ns} &= (6.0 + 2.7 + 6.6) + (6.0) - (2.7 + 2.7 + 10.6) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47) \\
 25.3 \text{ ns} &= (6.0 + 2.7 + 6.6) + (2.7) + (3.3 + 4.0)
 \end{aligned}$$

1. Calculations are based upon timing specifications for the ispLSI 1032-60.



**Maximum GRP Delay vs GLB Loads**



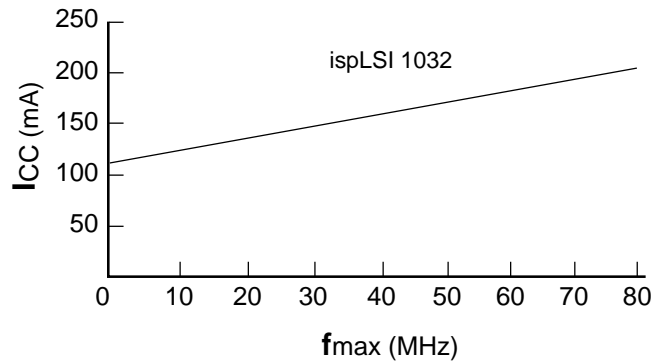
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**Power Consumption**

Power consumption in the ispLSI 1032/883 device depends on two primary factors: the speed at which the device is operating, and the number of Product Terms

used. Figure 3 shows the relationship between power and operating speed.

**Figure 3. Typical Device Power Consumption vs fmax**



Notes: Configuration of eight 16-bit Counters  
Typical Current at 5V, 25°C

ICC can be estimated for the ispLSI 1032 using the following equation:

$$I_{CC} = 52 + (\# \text{ of PTs} * 0.30) + (\# \text{ of nets} * \text{Max. freq} * 0.009) \text{ where:}$$

# of PTs = Number of Product Terms used in design

# of nets = Number of Signals used in device

Max. freq = Highest Clock Frequency to the device

The ICC estimate is based on typical conditions (VCC = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

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## Pin Description

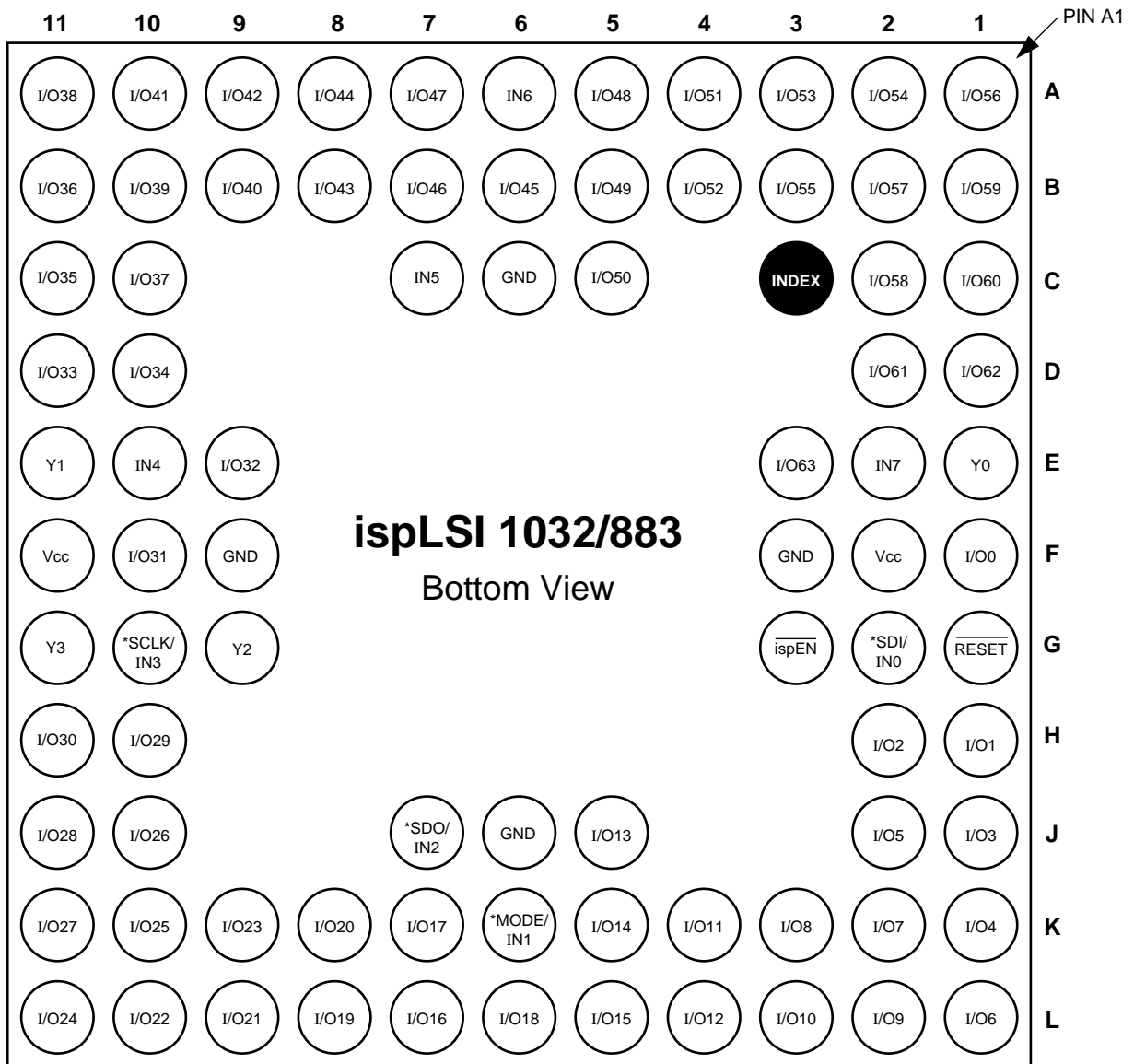
Name	CPGA Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	F1, H1, H2, J1, K1, J2, L1, K2, K3, L2, L3, K4, L4, J5, K5, L5, L7, K7, L6, L8, K8, L9, L10, K9, L11, K10, J10, K11, J11, H10, H11, F10, E9, D11, D10, C11, B11, C10, A11, B10, B9, A10, A9, B8, A8, B6, B7, A7, A5, B5, C5, A4, B4, A3, A2, B3, A1, B2, C2, B1, C1, D2, D1, E3	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 7	E10, C7, A6, E2	Dedicated input pins to the device.
$\overline{\text{ispEN}}$	G3	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0 <sup>1</sup>	G2	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 1 <sup>1</sup>	K6	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 2 <sup>1</sup>	J7	Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK/IN 3 <sup>1</sup>	G10	Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	G1	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	E1	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	E11	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	G9	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	G11	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
NC <sup>2</sup>	G3	No Connect
GND V <sub>CC</sub>	C6, F3, F9, J6 F2, F11	Ground (GND) V <sub>CC</sub>

1. Pins have dual function capability.

2. NC pins are not to be connected to any active signals, V<sub>cc</sub> or GND.

**Pin Configuration**

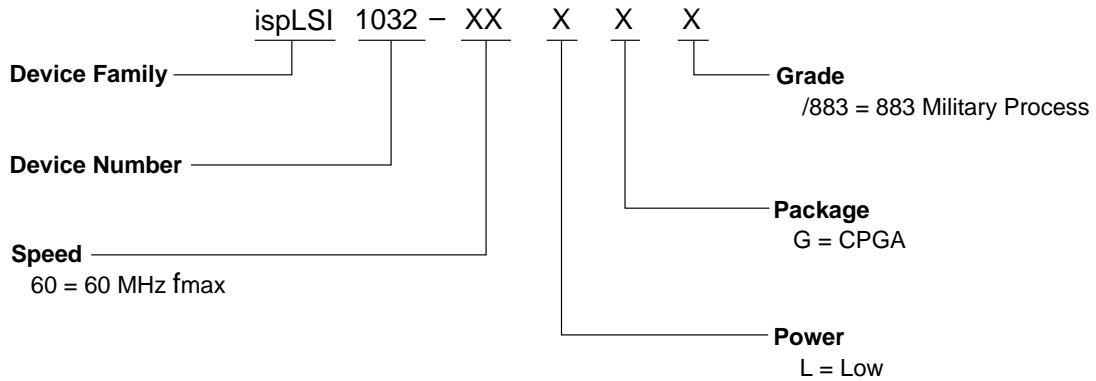
ispLSI 1032/883/883 84-Pin CPGA Pinout Diagram



\*Pins have dual function capability.

0488A-32-isp/883

**Part Number Description**



0212-80B-isp1032

**Ordering Information**

**MILITARY/883**

Family	f <sub>max</sub> (MHz)	t <sub>pd</sub> (ns)	Ordering Number	SMD Number	Package
ispLSI	60	20	ispLSI 1032-60LG/883	5962-9308501MXC	84-Pin CPGA

**Note:** Lattice Semiconductor recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number is recommended.

Table 2- 0041A-32-ispmil