

FEATURES

Infinite Sample-and-Hold Capability to $\pm 0.018\%$ Accuracy
High Integration: 32-Channel SHA in $12 \times 12 \text{ mm}^2$ LFBGA
Per Channel Acquisition Time of $16 \mu\text{s}$ max
Adjustable Voltage Output Range
Output Voltage Span 10 V
Output Impedance 0.5Ω
Readback Capability
DSP-/Microcontroller-Compatible Serial Interface
Parallel Interface
Temperature Range -40°C to $+85^\circ\text{C}$

APPLICATIONS

Level Setting
Instrumentation
Automatic Test Equipment
Industrial Control Systems
Data Acquisition
Low Cost I/O

GENERAL DESCRIPTION

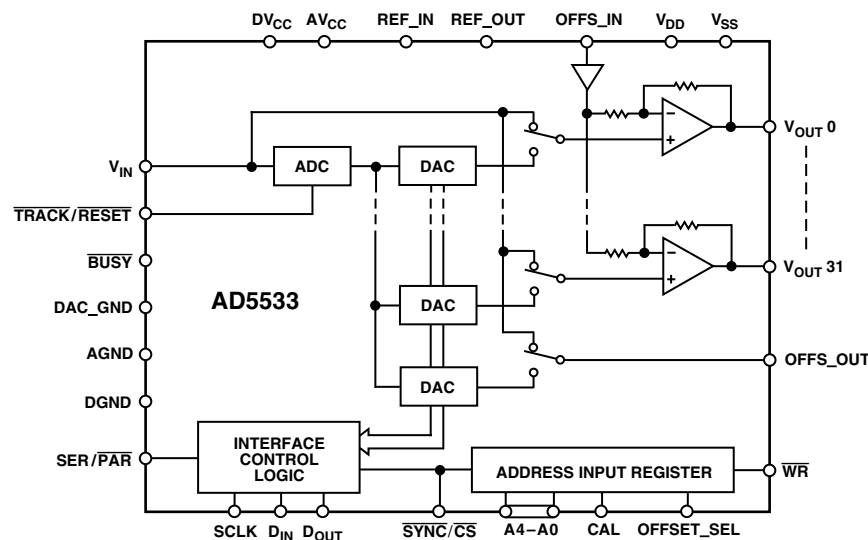
The AD5533 combines a 32-channel voltage translation function with an infinite output hold capability. An analog input voltage on the common input pin, V_{IN} , is sampled and its digital representation transferred to a chosen DAC register. V_{OUT} for this DAC is then updated to reflect the new contents of the DAC register. Channel selection is accomplished via the parallel address inputs A0–A4 or via the serial input port. The output voltage range is determined by the offset voltage at the OFFS_IN pin and the gain of the output amplifier. It is restricted to a range from $V_{SS} + 2 \text{ V}$ to $V_{DD} - 2 \text{ V}$ because of the headroom of the output amplifier.

The device is operated with $AV_{CC} = 5 \text{ V} \pm 5\%$, $DV_{CC} = 2.7 \text{ V}$ to 5.25 V , $V_{SS} = -4.75 \text{ V}$ to -16.5 V and $V_{DD} = 8 \text{ V}$ to 16.5 V and requires a stable 3 V reference on REF_IN as well as an offset voltage on OFFS_IN.

PRODUCT HIGHLIGHTS

1. Infinite Droopless Sample-and-Hold Capability.
2. The AD5533 is available in a 74-lead LFBGA package with a body size of $12 \text{ mm} \times 12 \text{ mm}$.

FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent No. 5,969,657; other patents pending.

REV. 0

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AD5533—SPECIFICATIONS

($V_{DD} = 8\text{ V to }16.5\text{ V}$, $V_{SS} = -4.75\text{ V to }-16.5\text{ V}$; $AV_{CC} = 4.75\text{ V to }5.25\text{ V}$; $DV_{CC} = 2.7\text{ V to }5.25\text{ V}$; $AGND = DGND = DAC_GND = 0\text{ V}$; $REF_IN = 3\text{ V}$; Output Range from $V_{SS} + 2\text{ V to }V_{DD} - 2\text{ V}$. All outputs unloaded. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter ¹	A Version ²	Unit	Conditions/Comments	
ANALOG CHANNEL				
V_{IN} to V_{OUT} Nonlinearity	± 0.018	% max	Input Range 100 mV to 2.96 V After Gain and Offset Adjustment 3.52 typ	
Gain	± 0.006	% typ		
Offset Error	3.46/3.6	min/max		
	± 50	mV max		
ANALOG INPUT (V_{IN})				
Input Voltage Range	0 to 3	V	Nominal Input Range 50 mV typ. Referred to V_{IN} . See Figure 5 12 mV typ. Referred to V_{IN} . See Figure 5 100 nA typ. V_{IN} Being Acquired on One Channel	
Input Lower Deadband	70	mV max		
Input Upper Deadband	40	mV max		
Input Current	1	μA max		
Input Capacitance ³	20	pF typ		
ANALOG INPUT (OFFS_IN)				
Input Current	1	μA max	100 nA typ	
VOLTAGE REFERENCE				
REF_IN				
Nominal Input Voltage	3.0	V	<1 nA typ	
Input Voltage Range ³	2.85/3.15	V min/max		
Input Current	1	μA max		
REF_OUT				
Output Voltage	3	V typ		
Output Impedance ³	280	k Ω typ		
Reference Temperature Coefficient ³	60	ppm/ $^{\circ}\text{C}$ typ		
ANALOG OUTPUTS (V_{OUT} 0–31)				
Output Temperature Coefficient ^{3, 4}	20	ppm/ $^{\circ}\text{C}$ typ	100 μA Output Load $V_{DD} = +15\text{ V} \pm 5\%$ $V_{SS} = -15\text{ V} \pm 5\%$	
DC Output Impedance	0.5	Ω typ		
Output Range	$V_{SS} + 2/V_{DD} - 2$	V min/max		
Resistive Load ^{3, 5}	5	k Ω min		
Capacitive Load ^{3, 5}	500	pF max		
Short-Circuit Current ³	10	mA typ		
DC Power Supply Rejection Ratio ³	-70	dB typ		
	-70	dB typ		
DC Crosstalk ³	250	μV max		
ANALOG OUTPUT (OFFS_OUT)				
Output Temperature Coefficient ^{3, 4}	20	ppm/ $^{\circ}\text{C}$ typ	Source Current	
DC Output Impedance ³	1.3	k Ω typ		
Output Range	50 to $REF_IN - 12$	mV typ		
Output Current	10	μA max		
Capacitive Load	100	pF max		
DIGITAL INPUTS³				
Input Current	± 10	μA max	5 μA typ $DV_{CC} = 5\text{ V} \pm 5\%$ $DV_{CC} = 3\text{ V} \pm 10\%$ $DV_{CC} = 5\text{ V} \pm 5\%$ $DV_{CC} = 3\text{ V} \pm 10\%$	
Input Low Voltage	0.8	V max		
	0.4	V max		
Input High Voltage	2.4	V min		
	2.0	V min		
Input Hysteresis (\overline{SCLK} and \overline{CS} Only)	200	mV typ		
Input Capacitance	10	pF max		
DIGITAL OUTPUTS (\overline{BUSY}, $DOUT$)³				
Output Low Voltage	0.4	V max	$DV_{CC} = 5\text{ V}$. Sinking 200 μA $DV_{CC} = 5\text{ V}$. Sourcing 200 μA $DV_{CC} = 3\text{ V}$. Sinking 200 μA $DV_{CC} = 3\text{ V}$. Sourcing 200 μA	
Output High Voltage	4.0	V min		
Output Low Voltage	0.4	V max		
Output High Voltage	2.4	V min		
High Impedance Leakage Current	± 1	μA max		
High Impedance Output Capacitance	15	pF typ		
			D_{OUT} Only D_{OUT} Only	

Parameter ¹	A Version ²	Unit	Conditions/Comments
POWER REQUIREMENTS			
Power-Supply Voltages			
V _{DD}	8/16.5	V min/max	
V _{SS}	-4.75/-16.5	V min/max	
AV _{CC}	4.75/5.25	V min/max	
DV _{CC}	2.7/5.25	V min/max	
Power-Supply Currents ⁶			
I _{DD}	15	mA max	10 mA typ. All Channels Full Scale
I _{SS}	15	mA max	10 mA typ. All Channels Full Scale
AI _{CC}	33	mA max	26 mA typ
DI _{CC}	1.5	mA max	1 mA typ
Power Dissipation ⁶	280	mW typ	V _{DD} = +10 V, V _{SS} = -5 V

NOTES

¹See Terminology.²A Version: Industrial temperature range -40°C to +85°C; typical at +25°C.³Guaranteed by design and characterization, not production tested.⁴AD780 as reference for the AD5533.⁵Ensure that you do not exceed T_J (max). See maximum ratings.⁶Outputs unloaded.

Specifications subject to change without notice.

AC CHARACTERISTICS (V_{DD} = 8 V to 16.5 V, V_{SS} = -4.75 V to -16.5 V; AV_{CC} = 4.75 V to 5.25 V; DV_{CC} = 2.7 V to 5.25 V; AGND = DGND = DAC_GND = 0 V; REF_IN = 3 V; Output Range from V_{SS} + 2 V to V_{DD} - 2 V. All outputs unloaded. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version ¹	Unit	Conditions/Comments
Output Settling Time ²	3	μs max	
Acquisition Time	16	μs max	
OFFS_IN Settling Time ²	10	μs max	500 pF, 5 kΩ Load; 0 V-3 V Step
Digital Feedthrough ²	0.2	nV-s typ	
Output Noise Spectral Density @ 1 kHz ²	400	nV/(√Hz) typ	
AC Crosstalk ²	5	nV-s typ	

NOTES

¹A version: Industrial temperature range -40°C to +85°C; typical at 25°C.²Guaranteed by design and characterization, not production tested

Specifications subject to change without notice.

AD5533

TIMING CHARACTERISTICS

PARALLEL INTERFACE

Parameter ^{1, 2}	Limit at T _{MIN} , T _{MAX} (A Version)	Unit	Conditions/Comments
t ₁	0	ns min	\overline{CS} to \overline{WR} Setup Time
t ₂	0	ns min	\overline{CS} to \overline{WR} Hold Time
t ₃	50	ns min	\overline{CS} Pulsewidth Low
t ₄	50	ns min	\overline{WR} Pulsewidth Low
t ₅	20	ns min	A4–A0, CAL, OFFS_SEL to \overline{WR} Setup Time
t ₆	0	ns min	A4–A0, CAL, OFFS_SEL to \overline{WR} Hold Time

NOTES

¹See Interface Timing Diagram.

²Guaranteed by design and characterization, not production tested.

Specifications subject to change without notice.

SERIAL INTERFACE

Parameter ^{1, 2}	Limit at T _{MIN} , T _{MAX} (A Version)	Unit	Conditions/Comments
f _{CLKIN}	20	MHz max	SCLK Frequency
t ₁	20	ns min	SCLK High Pulsewidth
t ₂	20	ns min	SCLK Low Pulsewidth
t ₃	10	ns min	\overline{SYNC} Falling Edge to SCLK Falling Edge Setup Time
t ₄	50	ns min	\overline{SYNC} Low Time
t ₅	10	ns min	D _{IN} Setup Time
t ₆	5	ns min	D _{IN} Hold Time
t ₇	5	ns min	\overline{SYNC} Falling Edge to SCLK Rising Edge Setup Time
t ₈ ³	20	ns max	SCLK Rising Edge to D _{OUT} Valid
t ₉ ³	60	ns max	SCLK Falling Edge to D _{OUT} High Impedance
t ₁₀	400	ns min	10th SCLK Falling Edge to \overline{SYNC} Falling Edge for Readback

NOTES

¹See Serial Interface Timing Diagrams.

²Guaranteed by design and characterization, not production tested.

³These numbers are measured with the load circuit of Figure 2.

Specifications subject to change without notice.

PARALLEL INTERFACE TIMING DIAGRAM

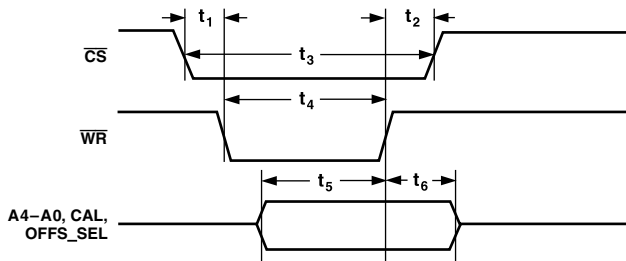


Figure 1. Parallel Write (SHA Mode Only)

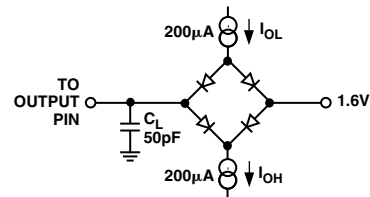


Figure 2. Load Circuit for D_{OUT} Timing Specifications

SERIAL INTERFACE TIMING DIAGRAMS

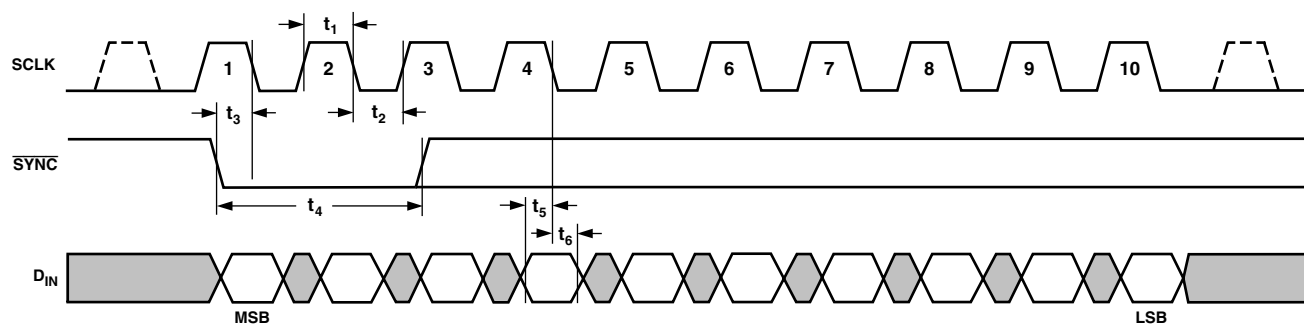


Figure 3. 10-Bit Write (SHA Mode and Both Readback Modes)

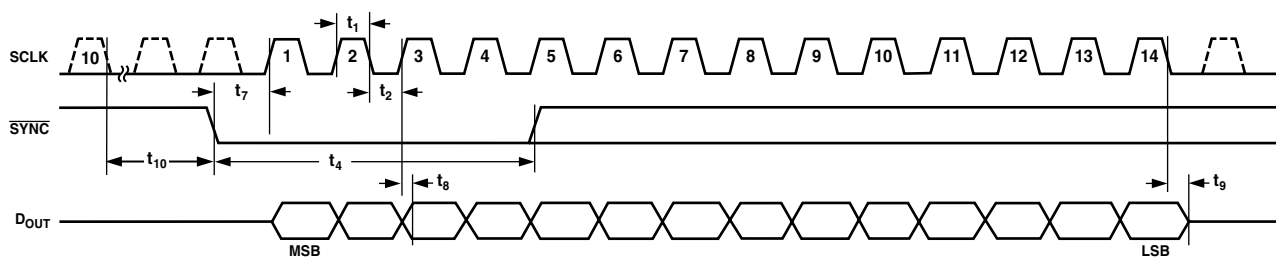


Figure 4. 14-Bit Read (Both Readback Modes)

AD5533

ABSOLUTE MAXIMUM RATINGS^{1, 2}

(T_A = 25°C unless otherwise noted)

V _{DD} to AGND	−0.3 V to +17 V
V _{SS} to AGND	+0.3 V to −17 V
AV _{CC} to AGND, DAC_GND	−0.3 V to +7 V
DV _{CC} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV _{CC} + 0.3 V
Digital Outputs to DGND	−0.3 V to DV _{CC} + 0.3 V
REF_IN to AGND, DAC_GND	−0.3 V to +7 V
V _{IN} to AGND, DAC_GND	−0.3 V to +7 V
V _{OUT0–31} to AGND	V _{SS} − 0.3 V to V _{DD} + 0.3 V
V _{OUT0–31} to V _{SS}	−0.3 V to +24 V
OFFS_IN to AGND	V _{SS} − 0.3 V to V _{DD} + 0.3 V
OFFS_OUT to AGND	AGND − 0.3 V to AV _{CC} + 0.3 V

AGND to DGND. −0.3 V to +0.3 V

Operating Temperature Range

Industrial −40°C to +85°C

Storage Temperature Range −65°C to +150°C

Junction Temperature (T_J max) 150°C

74-Lead LFBGA Package, θ_{JA} Thermal Impedance . . . 41°C/W

Reflow Soldering

Peak Temperature 220°C

Time at Peak Temperature 10 sec to 40 sec

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Transient currents of up to 100 mA will not cause SCR latch-up.

ORDERING GUIDE

Model	Function	Output Impedance	Output Voltage Span	Package Description	Package Option
AD5533ABC-1	32-Channel SHA Only	0.5 Ω typ	10 V	74-Lead LFBGA	BC-74
AD5532ABC-1*	32 DACs, 32-Channel SHA	0.5 Ω typ	10 V	74-Lead LFBGA	BC-74
AD5532ABC-2*	32 DACs, 32-Channel SHA	0.5 Ω typ	20 V	74-Lead LFBGA	BC-74
AD5532ABC-3*	32 DACs, 32-Channel SHA	500 Ω typ	10 V	74-Lead LFBGA	BC-74
AD5532ABC-5*	32 DACs, 32-Channel SHA	1 kΩ typ	10 V	74-Lead LFBGA	BC-74
EVAL-AD5532EB	AD5532/AD5533 Evaluation Board				

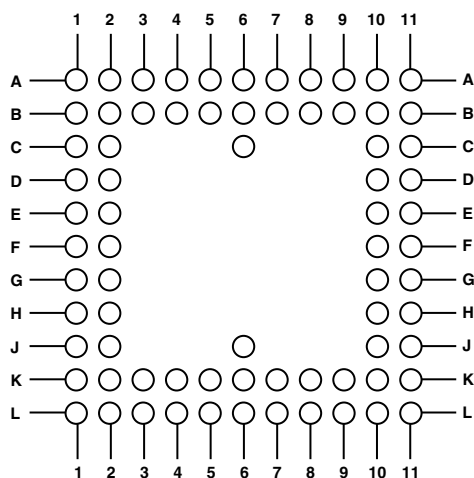
*Separate Data Sheet.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5533 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION



74-Lead LFBGA Ball Configuration

LFBGA Number	Ball Name	LFBGA Number	Ball Name	LFBGA Number	Ball Name
A1	N/C	C10	AVCC1	J10	VO9
A2	A4	C11	REF_OUT	J11	VO11
A3	A2	D1	VO20	K1	VO17
A4	A0	D2	DAC_GND2	K2	VO15
A5	$\overline{\text{CS/SYNC}}$	D10	AVCC2	K3	VO27
A6	DVCC	D11	OFFS_OUT	K4	VSS3
A7	SCLK	E1	VO26	K5	VSS1
A8	OFFSET_SEL	E2	VO14	K6	VSS4
A9	$\overline{\text{BUSY}}$	E10	AGND1	K7	VDD2
A10	$\overline{\text{TRACK/RESET}}$	E11	OFFS_IN	K8	VO2
A11	N/C	F1	VO25	K9	VO10
B1	VO16	F2	VO21	K10	VO13
B2	N/C	F10	AGND2	K11	VO12
B3	A3	F11	VO6	L1	N/C
B4	A1	G1	VO24	L2	VO28
B5	$\overline{\text{WR}}$	G2	VO8	L3	VO29
B6	DGND	G10	VO5	L4	VO30
B7	DIN	G11	VO3	L5	VDD3
B8	CAL	H1	VO23	L6	VDD1
B9	$\overline{\text{SER/PAR}}$	H2	VIN	L7	VDD4
B10	DOUT	H10	VO4	L8	VO31
B11	REF_IN	H11	VO7	L9	VO0
C1	VO18	J1	VO22	L10	VO1
C2	DAC_GND1	J2	VO19	L11	N/C
C6	N/C	J6	VSS2		

PIN FUNCTION DESCRIPTIONS

Pin	Function
AGND(1–2)	Analog GND Pins.
AV _{CC} (1–2)	Analog Supply Pins. Voltage range from 4.75 V to 5.25 V.
V _{DD} (1–4)	V _{DD} Supply Pins. Voltage range from 8 V to 16.5 V.
V _{SS} (1–4)	V _{SS} Supply Pins. Voltage range from –4.75 V to –16.5 V.
DGND	Digital GND Pins.
DV _{CC}	Digital Supply Pins. Voltage range from 2.7 V to 5.25 V.
DAC_GND(1–2)	Reference GND Supply for All the DACs.
REF_IN	Reference Voltage for Channels 0–31.
REF_OUT	Reference Output Voltage.
V _{OUT} (0–31)	Analog Output Voltages from the 32 Channels.
V _{IN}	Analog Input Voltage. Connect this to AGND if operating in DAC mode only.
A4–A1 ¹ , A0 ²	Parallel Interface: 5-Address Pins for 32 Channels. A4 = MSB of Channel Address. A0 = LSB.
CAL ¹	Parallel Interface: Control input that allows all 32 channels to acquire V _{IN} simultaneously.
$\overline{\text{CS}}/\text{SYNC}$	This pin is both the active low Chip Select pin for the parallel interface and the Frame Synchronization pin for the serial interface.
$\overline{\text{WR}}$ ¹	Parallel Interface: Write pin. Active low. This is used in conjunction with the $\overline{\text{CS}}$ pin to address the device using the parallel interface.
OFFSET_SEL ¹	Parallel Interface: Offset Select Pin. Active high. This is used to select the offset channel.
SCLK ²	Serial Clock Input for Serial Interface. This operates at clock speeds up to 20 MHz.
D _{IN} ²	Data Input for Serial Interface. Data must be valid on the falling edge of SCLK.
D _{OUT}	Output from the DAC Registers for readback. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
SER/ $\overline{\text{PAR}}$ ¹	This pin allows the user to select whether the serial or parallel interface will be used. If the pin is tied low, the parallel interface will be used. If it is tied high, the serial interface will be used.
OFFS_IN	Offset Input. The user can supply a voltage here to offset the output span. OFFS_OUT can also be tied to this pin if the user wants to drive this pin with the Offset Channel.
OFFS_OUT	Offset Output. This is the acquired/programmed offset voltage which can be tied to the OFFS_IN pin to offset the span.
$\overline{\text{BUSY}}$	This output tells the user when the input voltage is being acquired. It goes low during acquisition and returns high when the acquisition operation is complete.
$\overline{\text{TRACK}}/\overline{\text{RESET}}$ ²	If this input is held high, V _{IN} is acquired once the channel is addressed. While it is held low, the input to the gain/offset stage is switched directly to V _{IN} . The addressed channel begins to acquire V _{IN} on the rising edge of $\overline{\text{TRACK}}$. See $\overline{\text{TRACK}}$ Input section for further information. This input can also be used as a means of resetting the complete device to its power-on-reset conditions. This is achieved by applying a low-going pulse of between 50 ns and 150 ns to this pin. See section on $\overline{\text{RESET}}$ Function for further details.

NOTES

¹Internal pull-down devices on these logic inputs. Therefore, they can be left floating and will default to a logic low condition.

²Internal pull-up devices on these logic inputs. Therefore, they can be left floating and will default to a logic high condition.

TERMINOLOGY

V_{IN} to V_{OUT} Nonlinearity

This is a measure of the maximum deviation from a straight line passing through the endpoints of the V_{IN} versus V_{OUT} transfer function. It is expressed as a percentage of the full-scale span.

Offset Error

This is a measure of the output error when $V_{IN} = 70$ mV. Ideally, with $V_{IN} = 70$ mV:

$$V_{OUT} = (Gain \times 70) - ((Gain - 1) \times V_{OFFS_IN}) \text{ mV}$$

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal). It is expressed in mV and can be positive or negative. See Figure 5.

Gain Error

This is a measure of the span error of the analog channel. It is the deviation in slope of the transfer function. See Figure 5. It is calculated as:

$$\text{Gain Error} = \text{Actual Full-Scale Output} - \text{Ideal Full-Scale Output} - \text{Offset Error}$$

where

$$\text{Ideal Full-Scale Output} = \text{Ideal Gain} \times 2.96 - ((\text{Ideal Gain} - 1) \times V_{OFFS_IN})$$

$$\text{Ideal Gain} = 3.52$$

Output Temperature Coefficient

This is a measure of the change in analog output with changes in temperature. It is expressed in ppm/ $^{\circ}$ C.

DC Power-Supply Rejection Ratio

DC Power-Supply Rejection Ratio (PSRR) is a measure of the change in analog output for a change in supply voltage (V_{DD} and V_{SS}). It is expressed in dBs. V_{DD} and V_{SS} are varied $\pm 5\%$.

DC Crosstalk

This is the dc change in the output level of one channel in response to a full-scale change in the output of all other channels. It is expressed in μ V.

Output Settling Time

This is the time taken from when $\overline{\text{BUSY}}$ goes high to when the output has settled to $\pm 0.018\%$.

Acquisition Time

This is the time taken for the V_{IN} input to be acquired. It is the length of time that $\overline{\text{BUSY}}$ stays low.

OFFS_IN Settling Time

This is the time taken from a 0 V–3 V step change in input voltage on OFFS_IN until the output has settled to within $\pm 0.35\%$.

Digital Feedthrough

This is a measure of the impulse injected into the analog outputs from the digital control inputs when the part is not being written to, i.e., CS/SYNC is high. It is specified in nV-secs and is measured with a worst-case change on the digital input pins, e.g., from all 0s to all 1s and vice versa.

Output Noise Spectral Density

This is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per root Hertz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in $\text{nV}/(\sqrt{\text{Hz}})^{1/2}$.

AC Crosstalk

This is the area of the glitch that occurs on the output of one channel while another channel is acquiring. It is expressed in nV-secs.

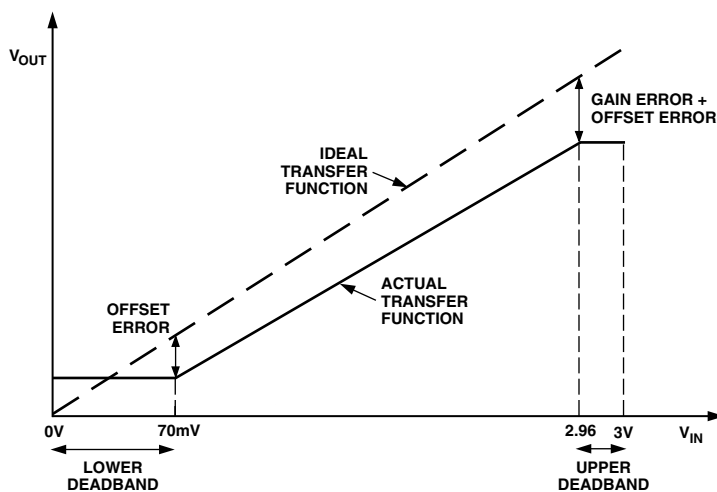


Figure 5. SHA Transfer Function

AD5533—Typical Performance Characteristics

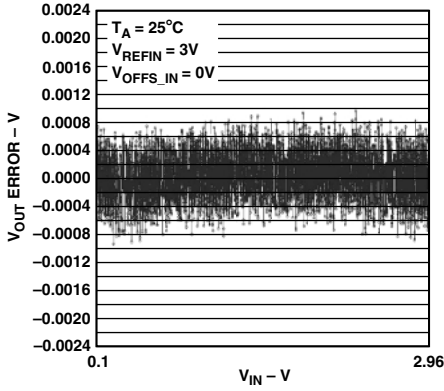


Figure 6. V_{IN} to V_{OUT} Accuracy after Offset and Gain Adjustment

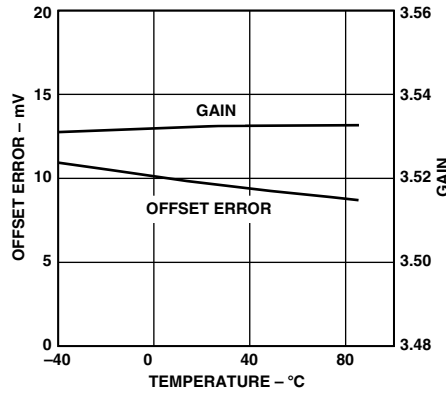


Figure 7. Offset Error and Gain vs. Temperature

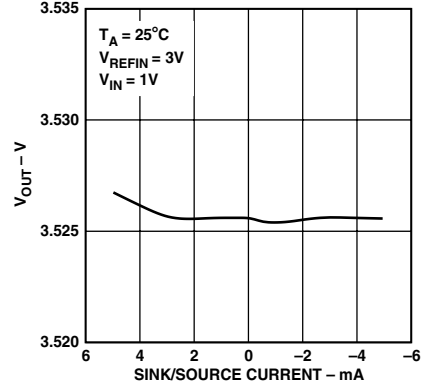


Figure 8. V_{OUT} Source and Sink Capability

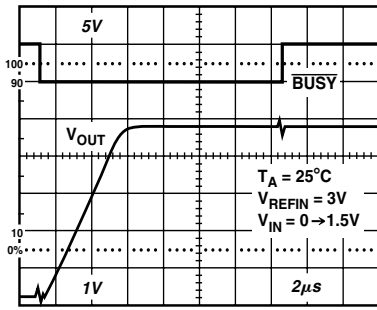


Figure 9. Acquisition Time and Output Settling Time

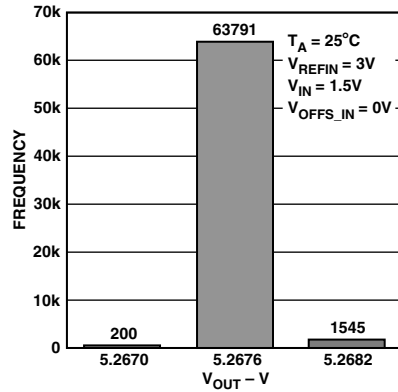


Figure 10. SHA Mode Repeatability (64K Acquisitions)

FUNCTIONAL DESCRIPTION

The AD5533 can be thought of as consisting of an ADC and 32 DACs in a single package. The input voltage V_{IN} is sampled and converted into a digital word. The digital result is loaded into one of the DAC registers and is converted (with gain and offset) into an analog output voltage (V_{OUT0} – V_{OUT31}). Since the channel output voltage is effectively the output of a DAC there is no droop associated with it. As long as power to the device is maintained, the output voltage will remain constant until this channel is addressed again.

To update a single channel's output voltage, the required new voltage level is set up on the common input pin, V_{IN} . The desired channel is then addressed via the parallel port or the serial port. When the channel address has been loaded, provided \overline{TRACK} is high, the circuit begins to acquire the correct code to load to the DAC in order that the DAC output matches the voltage on V_{IN} . The $BUSY$ pin goes low and remains so until the acquisition is complete. The noninverting input to the output buffer is tied to V_{IN} during the acquisition period to avoid spurious outputs while the DAC acquires the correct code. The acquisition is completed in 16 μ s max. The $BUSY$ pin goes high and the updated DAC output assumes control of the output voltage. The output voltage of the DAC is connected to the noninverting input of the output buffer. The held voltage will remain on the output pin indefinitely, without drooping, as long as power to the device is maintained.

On power-on, all the DACs, including the offset channel, are loaded with zeros. The outputs of the DACs are at 50 mV typical (negative full-scale). If the $OFFS_IN$ pin is driven by the on-board offset channel, the outputs V_{OUT0} to V_{OUT31} are also at 50 mV on power-on since $OFFS_IN = 50$ mV ($V_{OUT} = 3.52 \times V_{DAC} - 3.52 \times V_{OFFS_IN} = 176$ mV – 126 mV = 50 mV).

Analog Input

The equivalent analog input circuit is shown in Figure 11. The Capacitor C1 is typically 20 pF and can be attributed to pin capacitance and 32 off-channels. When a channel is selected, an extra 7.5 pF (typ) is switched in. This Capacitor C2 is charged to the previously acquired voltage on that particular channel so it must charge/discharge to the new level. It is essential that the external source can charge/discharge this additional capacitance within 1 μ s–2 μ s of channel selection so that V_{IN} can be acquired accurately. For this reason a low impedance source is recommended.

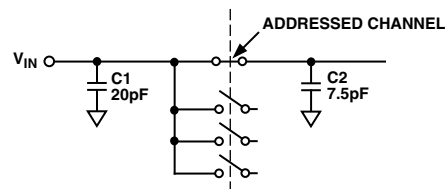


Figure 11. Analog Input Circuit

Large source impedances will significantly affect the performance of the ADC. This may necessitate the use of an input buffer amplifier.

Output Buffer Stage—Gain and Offset

The function of the output buffer stage is to translate the 0 V–3 V output of the DAC to a wider range. This is done by gaining up the DAC output by 3.52 and offsetting the voltage by the voltage on $OFFS_IN$ pin.

$$V_{OUT} = 3.52 \times V_{DAC} - 2.52 \times V_{OFFS_IN}$$

V_{DAC} is the output of the DAC.

V_{OFFS_IN} is the voltage at the $OFFS_IN$ pin.

Table I shows how the output range on V_{OUT} relates to the offset voltage supplied by the user.

Table I. Sample Output Voltage Ranges

V_{OFFS_IN} (V)	V_{DAC} (V)	V_{OUT} (V)
0.5	0 to 3	–1.26 to +9.3
1	0 to 3	–2.52 to +8.04

V_{OUT} is limited only by the headroom of the output amplifiers. V_{OUT} must be within maximum ratings.

Offset Voltage Channel

The offset voltage can be externally supplied by the user at $OFFS_IN$ or it can be supplied by an additional offset voltage channel on the device itself. The required offset voltage is set up on V_{IN} and acquired by the offset DAC. This offset channel's DAC output is directly connected to $OFFS_OUT$. By connecting $OFFS_OUT$ to $OFFS_IN$ this offset voltage can be used as the offset voltage for the 32-output amplifiers. It is important to choose the offset so that V_{OUT} is within maximum ratings.

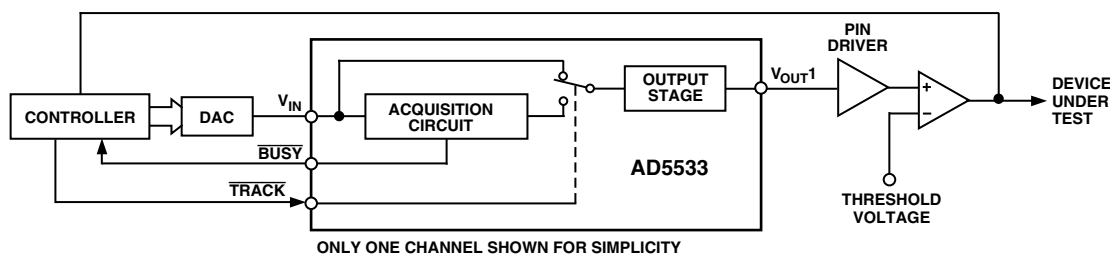


Figure 12. Typical ATE Circuit Using \overline{TRACK} Input

AD5533

Reset Function

The reset function on the AD5533 can be used to reset all nodes on this device to their power-on-reset condition. This is implemented by applying a low-going pulse of between 50 ns and 150 ns to the $\overline{\text{TRACK/RESET}}$ pin on the device. If the applied pulse is less than 50 ns it is assumed to be a glitch and no operation takes place. If the applied pulse is wider than 150 ns this pin adopts its track function on the selected channel, V_{IN} is switched to the output buffer and an acquisition on the channel will not occur until a rising edge of $\overline{\text{TRACK}}$.

$\overline{\text{TRACK}}$ Function

Normally in SHA mode of operation, $\overline{\text{TRACK}}$ is held high and the channel begins to acquire when it is addressed. However, if $\overline{\text{TRACK}}$ is low when the channel is addressed, V_{IN} is switched to the output buffer and an acquisition on the channel will not occur until a rising edge of $\overline{\text{TRACK}}$. At this stage the $\overline{\text{BUSY}}$ pin will go low until the acquisition is complete, at which point the DAC assumes control of the voltage to the output buffer and V_{IN} is free to change again without affecting this output value.

This is useful in an application where the user wants to ramp up V_{IN} until V_{OUT} reaches a particular level (Figure 12). V_{IN} does not need to be acquired continuously while it is ramping up. $\overline{\text{TRACK}}$ can be kept low and only when V_{OUT} has reached its desired voltage is $\overline{\text{TRACK}}$ brought high. At this stage, the acquisition of V_{IN} begins.

In the example shown, a desired voltage is required on the output of the pin driver. This voltage is represented by one input to a comparator. The microcontroller/microprocessor ramps up the input voltage on V_{IN} through a DAC. $\overline{\text{TRACK}}$ is kept low while the voltage on V_{IN} ramps up so that V_{IN} is not continually acquired. When the desired voltage is reached on the output of the pin driver, the comparator output switches. The $\mu\text{C}/\mu\text{P}$ then knows what code is required to be input in order to obtain the desired voltage at the DUT. The $\overline{\text{TRACK}}$ input is now brought high and the part begins to acquire V_{IN} . $\overline{\text{BUSY}}$ goes low until V_{IN} has been acquired. When $\overline{\text{BUSY}}$ goes high, the output buffer is switched from V_{IN} to the output of the DAC.

MODES OF OPERATION

The AD5533 can be used in three different modes. These modes are set by two mode bits, the first two bits in the serial word. The 01 option (DAC Mode) is not available for the AD5533. To avail of this mode refer to the AD5532 data sheet. If you attempt to set up DAC mode, the AD5533 will enter a test-mode and a 24-clock write will be necessary to clear this.

Table II. Modes of Operation

Mode Bit 1	Mode Bit 2	Operating Mode
0	0	SHA Mode
0	1	DAC Mode (Not Available)
1	0	Acquire and Readback
1	1	Readback

1. SHA Mode

In this standard mode a channel is addressed and that channel acquires the voltage on V_{IN} . This mode requires a 10-bit write to address the relevant channel ($V_{\text{OUT}0}$ – $V_{\text{OUT}31}$, offset channel or all channels). MSB is written first.

2. Acquire and Readback Mode

This mode allows the user to acquire V_{IN} and read back the data in a particular DAC register. The relevant channel is addressed (10-bit write, MSB first) and V_{IN} is acquired in 16 μs (max). Following the acquisition, after the next falling edge of $\overline{\text{SYNC}}$ the data in the relevant DAC register is clocked out onto the D_{OUT} line in a 14-bit serial format. During readback D_{IN} is ignored. The full acquisition time must elapse before the DAC register data can be clocked out.

3. Readback Mode

Again, this is a readback mode but no acquisition is performed. The relevant channel is addressed (10-bit write, MSB first) and on the next falling edge of $\overline{\text{SYNC}}$, the data in the relevant DAC register is clocked out onto the D_{OUT} line in a 14-bit serial format. The user must allow 400 ns (min) between the last SCLK falling edge in the 10-bit write and the falling edge of $\overline{\text{SYNC}}$ in the 14-bit readback. The serial write and read words can be seen in Figure 13.

This feature allows the user to read back the DAC register code of any of the channels. Readback is useful if the system has been calibrated and the user wants to know what code in the DAC corresponds to a desired voltage on V_{OUT} .

INTERFACES

SERIAL INTERFACE

The SER/PAR pin is tied high to enable the serial interface and to disable the parallel interface. The serial interface is controlled by four pins as follows:

$\overline{\text{SYNC}}$, D_{IN} , SCLK

Standard 3-wire interface pins. The $\overline{\text{SYNC}}$ pin is shared with the $\overline{\text{CS}}$ function of the parallel interface.

D_{OUT}

Data Out pin for reading back the contents of the DAC registers. The data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.

Cal Bit

When this is high all 32 channels acquire V_{IN} simultaneously. The acquisition time is then 45 μs (typ) and accuracy may be reduced.

Offset_Sel Bit

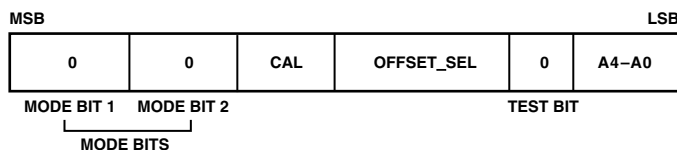
If this bit is set high, the offset channel is selected and Bits A4–A0 are ignored.

Test Bit

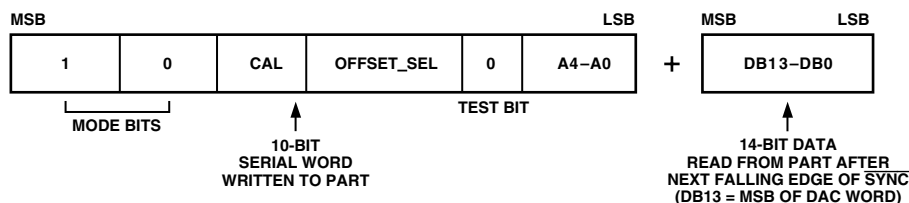
This must be set low for correct operation of the part.

A4–A0

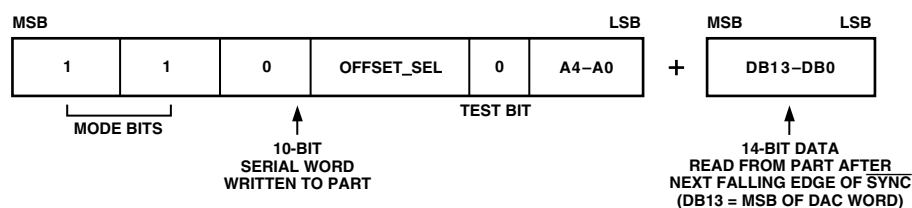
Used to address any one of the 32 channels (A4 = MSB of address, A0 = LSB).



a. 10-Bit Input Serial Write Word (SHA Mode)



b. Input Serial Interface (Acquire and Readback Mode)



c. Input Serial Interface (Readback Mode)

Figure 13. Serial Interface Formats

DB13–DB0

These are used in both readback modes to read a 14-bit word from the addressed DAC register.

The serial interface is designed to allow easy interfacing to most microcontrollers and DSPs, e.g., PIC16C, PIC17C, QSPI, SPI, DSP56000, TMS320, and ADSP-21xx, without the need for any glue logic. When interfacing to the 8051, the SCLK must be inverted. The Microprocessor/Microcontroller Interface section explains how to interface to some popular DSPs and microcontrollers.

Figures 3 and 4 show the timing diagram for a serial read and write to the AD5533. The serial interface works with both a continuous and a noncontinuous serial clock. The first falling edge of $\overline{\text{SYNC}}$ resets a counter that counts the number of serial clocks to ensure the correct number of bits are shifted in and out of the serial shift registers. Any further edges on $\overline{\text{SYNC}}$ are ignored until the correct number of bits are shifted in or out. Once the correct number of bits have been shifted in or out, the SCLK is ignored. In order for another serial transfer to take place the counter must be reset by the falling edge of $\overline{\text{SYNC}}$. In readback, the first rising SCLK edge after the falling edge of $\overline{\text{SYNC}}$ causes D_{OUT} to leave its high impedance state and data is clocked out onto the D_{OUT} line and also on subsequent SCLK rising edges. The D_{OUT} pin goes back into a high impedance state on the falling edge of the 14th SCLK. Data on the D_{IN} line is latched in on the first SCLK falling edge after the

falling edge of the $\overline{\text{SYNC}}$ signal and on subsequent SCLK falling edges. The serial interface will not shift data in or out until it receives the falling edge of the $\overline{\text{SYNC}}$ signal.

Parallel Interface

The $\text{SER}/\overline{\text{PAR}}$ bit must be tied low to enable the parallel interface and disable the serial interface. The parallel interface is controlled by nine pins.

 $\overline{\text{CS}}$

Active low package select pin. This pin is shared with the $\overline{\text{SYNC}}$ function for the serial interface.

 $\overline{\text{WR}}$

Active low write pin. The values on the address pins are latched on a rising edge of $\overline{\text{WR}}$.

A4–A0

Five address pins (A4 = MSB of address, A0 = LSB). These are used to address the relevant channel (out of a possible 32).

Offset_Sel

Offset select pin. This has the same function as the Offset_Sel bit in the serial interface. When it is high, the offset channel is addressed and the address on A4–A0 is ignored.

Cal

Same functionality as the Cal bit in the serial interface. When this pin is high, all 32 channels acquire V_{IN} simultaneously.

AD5533

MICROPROCESSOR INTERFACING

AD5533 to ADSP-21xx Interface

The ADSP-21xx family of DSPs are easily interfaced to the AD5533 without the need for extra logic.

A data transfer is initiated by writing a word to the TX register after the SPORT has been enabled. In a write sequence data is clocked out on each rising edge of the DSP's serial clock and clocked into the AD5533 on the falling edge of its SCLK. In readback 16 bits of data are clocked out of the AD5533 on each rising edge of SCLK and clocked into the DSP on the rising edge of SCLK. DIN is ignored. The valid 14 bits of data will be centered in the 16-bit RX register when using this configuration. The SPORT control register should be set up as follows:

- TFSW = RFSW = 1, Alternate Framing
- INVRFS = INVTFS = 1, Active Low Frame Signal
- DTYPE = 00, Right Justify Data
- ISCLK = 1, Internal Serial Clock
- TFSR = RFSR = 1, Frame Every Word
- IRFS = 0, External Framing Signal
- ITFS = 1, Internal Framing Signal
- SLEN = 1001, 10-Bit Data Words (SHA Mode Write)
- SLEN = 1111, 16-Bit Data Words (Readback Mode)

Figure 14 shows the connection diagram.

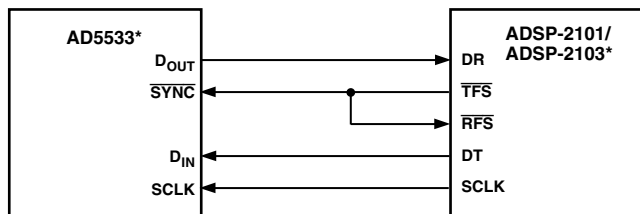


Figure 14. AD5533 to ADSP-2101/ADSP-2103 Interface

AD5533 to MC68HC11

The Serial Peripheral Interface (SPI) on the MC68HC11 is configured for Master Mode (MSTR = 1), Clock Polarity Bit (CPOL) = 0 and the Clock Phase Bit (CPHA) = 1. The SPI is configured by writing to the SPI Control Register (SPCR)—see *68HC11 User Manual*. SCK of the 68HC11 drives the SCLK of the AD5533, the MOSI output drives the serial data line (D_{IN}) of the AD5533 and the MISO input is driven from D_{OUT}. The SYNC signal is derived from a port line (PC7). When data is being transmitted to the AD5533, the SYNC line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to transmit 10-data bits in SHA mode it is important to left-justify the

data in the SPDR register. PC7 must be pulled low to start a transfer. It is taken high and pulled low again before any further read/write cycles can take place. A connection diagram is shown in Figure 15.

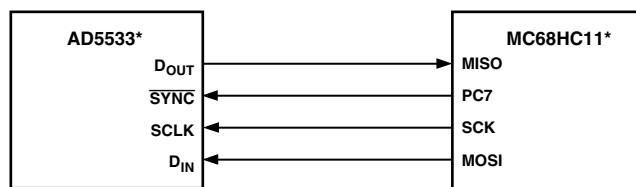


Figure 15. AD5533 to MC68HC11 Interface

AD5533 to PIC16C6x/7x

The PIC16C6x Synchronous Serial Port (SSP) is configured as an SPI Master with the Clock Polarity bit = 0. This is done by writing to the Synchronous Serial Port Control Register (SSPCON). See user PIC16/17 Microcontroller User Manual. In this example I/O port RA1 is being used to pulse SYNC and enable the serial port of the AD5533. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, two consecutive read/write operations are needed for a 10-bit write and a 14-bit readback. Figure 16 shows the connection diagram.

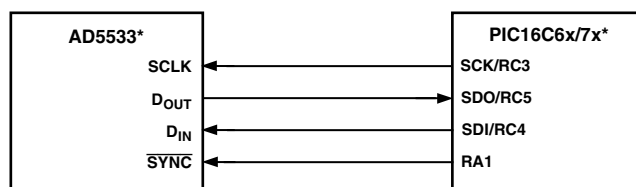


Figure 16. AD5533 to PIC16C6x/7x Interface

AD5533 TO 8051

The AD5533 requires a clock synchronized to the serial data. The 8051 serial interface must therefore be operated in Mode 0. In this mode serial data enters and exits through RxD and a shift clock is output on TxD. Figure 17 shows how the 8051 is connected to the AD5533. Because the AD5533 shifts data out on the rising edge of the shift clock and latches data in on the falling edge, the shift clock must be inverted. The AD5533 requires its data with the MSB first. Since the 8051 outputs the LSB first, the transmit routine must take this into account.

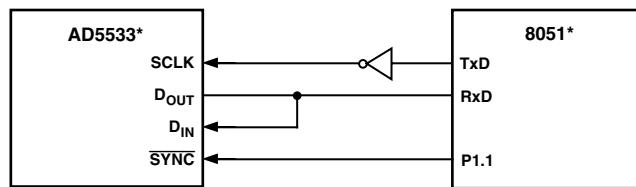


Figure 17. AD5533 to 8051 Interface

APPLICATION CIRCUITS

AD5533 in a Typical ATE System

The AD5533 Infinite Sample-and-Hold is ideally suited for use in Automatic Test Equipment. Several SHAs are required to control pin drivers, comparators, active loads, and signal timing. Traditionally, sample-and-hold devices with droop were used in this application. These required refreshing to prevent the voltage from drifting.

The AD5533 has several advantages: no refreshing is required, there is no droop, pedestal error is eliminated, and there is no need for extra filtering to remove glitches. Overall, a higher level of integration is achieved in a smaller area, see Figure 18.

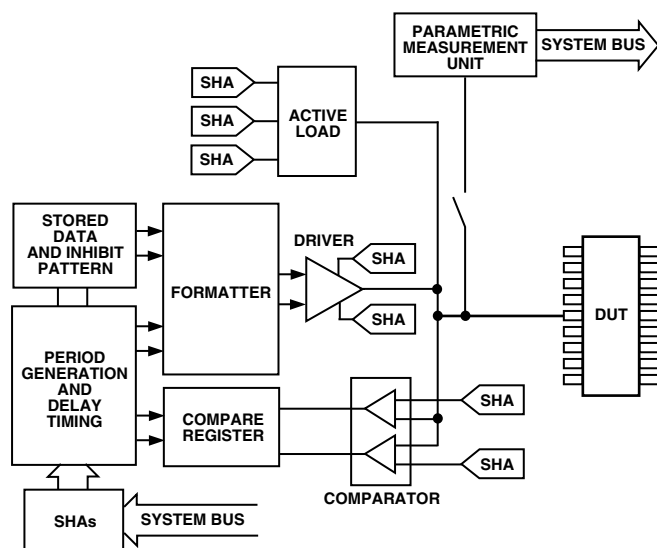


Figure 18. AD5533 in an ATE System

Typical Application Circuit

The AD5533 can be used to set up voltage levels on 32 channels as shown in the circuit below. An AD780 provides the 3 V reference for the AD5533, and for the AD5541 16-bit DAC. A simple 3-wire interface is used to write to the AD5541. The DAC output is buffered by an AD820. It is essential to minimize noise on V_{IN} and REF_{IN} when laying out this circuit.

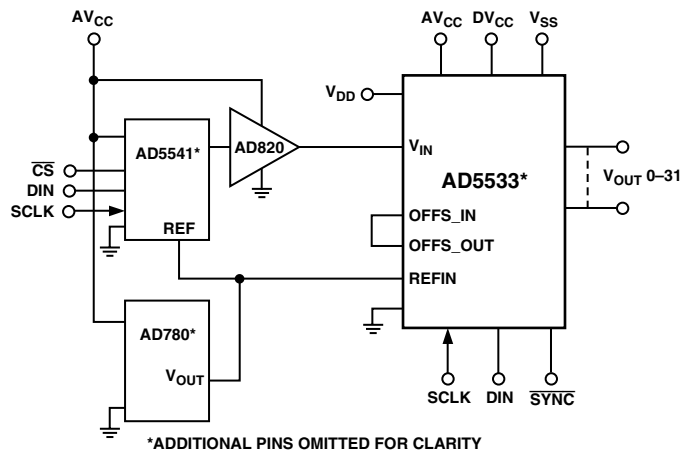


Figure 19. Typical Application Circuit

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5533 is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the AD5533 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. For supplies with multiple pins (V_{SS} , V_{DD} , AV_{CC}) it is recommended to tie those pins together. The AD5533 should have ample supply bypassing of 10 μF in parallel with 0.1 μF on each supply located as close to the package as possible, ideally right up against the device. The 10 μF capacitors are the tantalum bead type. The 0.1 μF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching.

The power supply lines of the AD5533 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. A ground line routed between the D_{IN} and $SCLK$ lines will help reduce crosstalk between them (not required on a multilayer board as there will be a separate ground plane, but separating the lines will help). It is essential to minimize noise on V_{IN} and REF_{IN} lines.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

74-Lead LFBGA
(BC-74)

