Synchronous Buck Controller with Dual Linear Regulator Controllers

ADP3171

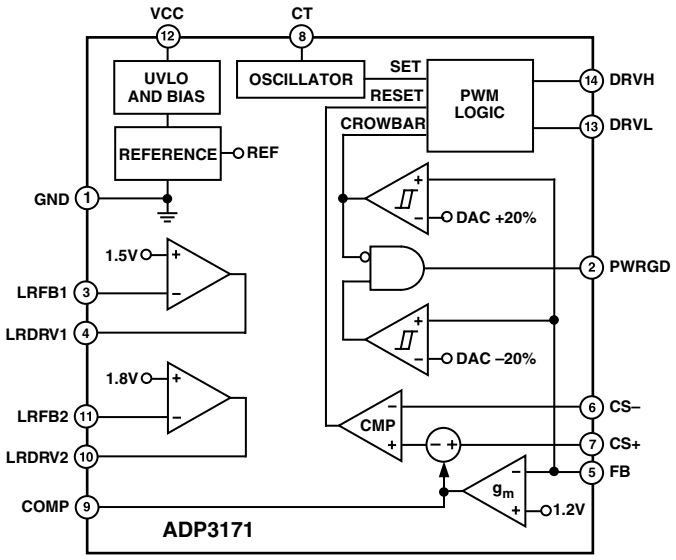
FEATURES

- Fixed 1.2 V N-Channel Synchronous Buck Driver
- Two On-Board Linear Regulator Controllers
- Total Accuracy ±1% over Temperature
- High Efficiency Current-Mode Operation
- Short Circuit Protection
- Power Good Output
- Overvoltage Protection Crowbar Protects Switching Output with No Additional External Components

APPLICATIONS

- Auxiliary System Supplies for Desktop Computer Systems
- General-Purpose Low Voltage Supplies

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3171 is a highly efficient output synchronous buck switching regulator controller optimized for converting a 5 V main supply into the auxiliary supply voltages required by processors and chipsets. The ADP3171 provides a fixed output voltage of 1.2 V at up to 15 A, depending on the power ratings of the external MOSFETs and inductor. The ADP3171 uses a current-mode, constant off time architecture to drive two N-channel MOSFETs at a programmable switching frequency that can be optimized for regulator size and efficiency.

The ADP3171 provides accurate and reliable short circuit protection and adjustable current limiting. It also includes an integrated overvoltage crowbar function to protect the load in case the output voltage exceeds the nominal programmed voltage by more than 20%.

The ADP3171 contains two fixed output voltage linear regulator controllers that are designed to drive external N-channel MOSFETs. These linear regulators are used to generate the auxiliary voltages required in most motherboard designs and have been designed to provide a high bandwidth load-transient response.

The ADP3171 is specified over the commercial temperature range of 0°C to 70°C and is available in a 14-lead SOIC package.

REV. 0

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ADP3171–SPECIFICATIONS[1] (V_{CC} = 12 V, T_A = 0°C to 70°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
FEEDBACK INPUT						
Output Accuracy	V_{FB}	Figure 1	1.188	1.2	1.212	V
Line Regulation	ΔV_{OUT}	VCC = 10 V to 14 V		0.06		%
Crowbar Trip Point	$V_{CROWBAR}$	% of Nominal FB Voltage	115	120	125	%
Crowbar Reset Point		% of Nominal FB Voltage	40	50	60	%
Crowbar Response Time	$t_{CROWBAR}$	Overvoltage to DRVL Going High		400		ns
OSCILLATOR						
Off Time		T_A = 25°C, CT = 200 pF	3.5	4	4.5	µs
CT Charge Current	I_{CT}	T_A = 25°C, V_{OUT} in Regulation	130	150	170	µA
		T_A = 25°C, V_{OUT} = 0 V	25	35	45	µA
ERROR AMPLIFIER						
Output Resistance	$R_{O(ERR)}$			130		kΩ
Transconductance	$g_{m(ERR)}$		2.05	2.2	2.35	mmho
Output Current	$I_{O(ERR)}$	FB Forced to V_{OUT} – 3%		625		µA
Maximum Output Voltage	$V_{COMP(MAX)}$	FB Forced to V_{OUT} – 3%		3.0		V
Output Disable Threshold	$V_{COMP(OFF)}$		600	750	900	mV
–3 dB Bandwidth	BW_{ERR}	COMP = Open		500		kHz
CURRENT SENSE						
Threshold Voltage	$V_{CS(TH)}$	FB Forced to V_{OUT} – 3%	69	78	87	mV
		FB ≤ 0.45 V	35	45	54	mV
		0.8 V ≤ COMP ≤ 1 V		1	5	mV
Input Bias Current	I_{CS+}, I_{CS-}	CS+ = CS– = V_{OUT}		0.5	5	µA
Response Time	t_{CS}	CS+ – (CS–) > 87 mV to DRVH Going Low		50		ns
OUTPUT DRIVERS						
Output Resistance	$R_{O(DRV(X))}$	I_L = 50 mA		6		Ω
Output Transition Time	t_R, t_F	C_L = 3000 pF		80		ns
LINEAR REGULATORS						
Feedback Current	$I_{LRFB(X)}$			0.3	1	µA
LR1 Feedback Voltage	$V_{LRFB(1)}$	Figure 2, VCC = 4.5 V to 12.6 V	1.45	1.5	1.55	V
LR2 Feedback Voltage	$V_{LRFB(2)}$	Figure 2, VCC = 4.5 V to 12.6 V	1.75	1.8	1.85	V
Driver Output Voltage	$V_{LRDRV(X)}$	VCC = 4.5 V, $V_{LRFB(X)}$ = 0 V	4.2			V
POWER GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	% of Nominal FB Voltage	75	80	85	%
Undervoltage Hysteresis		% of Nominal FB Voltage		5		%
Overvoltage Threshold	$V_{PWRGD(OV)}$	% of Nominal FB Voltage	115	120	125	%
Overvoltage Reset Point		% of Nominal FB Voltage	40	50	60	%
Output Voltage Low	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = 1 mA		250	500	mV
Response Time				250		ns
SUPPLY						
DC Supply Current[2]	I_{CC}			7	9	mA
UVLO Threshold Voltage	V_{UVLO}		6.75	7	7.25	V
UVLO Hysteresis			0.8	1	1.2	V

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).

[2]Dynamic supply current is higher due to the gate charge being delivered to the external MOSFETs.

Specifications subject to change without notice.

PIN FUNCTION DESCRIPTIONS

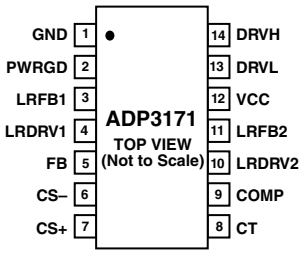
Pin	Mnemonic	Function
1	GND	Ground Reference. GND should have a low impedance path to the source of the synchronous MOSFET.
2	PWRGD	Power Good Indicator. Open-drain output that signals when the output voltage is in the proper operating range.
3, 11	LRFB1, LRFB2	Feedback connections for the fixed output voltage linear regulator controllers.
4, 10	LRDRV1, LRDRV2	Gate drives for the respective linear regulator N-channel MOSFETs.
5	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage.
6	CS–	Current Sense Negative Node. Negative input for the current comparator.
7	CS+	Current Sense Positive Node. Positive input for the current comparator. The output current is sensed as a voltage at this pin with respect to CS–.
8	CT	Timing Capacitor. An external capacitor connected from CT to ground sets the off time of the device.
9	COMP	Error Amplifier Output and Compensation Point. The voltage at this output programs the output current control level between CS+ and CS–.
12	VCC	Supply Voltage for the ADP3171.
13	DRVL	Low-Side MOSFET Drive. Gate drive for the synchronous rectifier N-channel MOSFET. The voltage at DRVL swings from GND to VCC.
14	DRVH	High-Side MOSFET Drive. Gate drive for the buck switch N-channel MOSFET. The voltage at DRVH swings from GND to VCC.

ABSOLUTE MAXIMUM RATINGS*

VCC . . . . . –0.3 V to +15 V
DRVH, DRVL, LRDRV1, LRDRV2 . . . . . –0.3 V to VCC + 0.3 V
All Other Inputs and Outputs . . . . . –0.3 V to +10 V
Operating Ambient Temperature Range . . . . . 0°C to 70°C
Operating Junction Temperature . . . . . 125°C
Storage Temperature Range . . . . . –65°C to +150°C
θ_{JA} . . . . . 105°C/W
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged. Unless otherwise specified, all voltages are referenced to GND.

PIN CONFIGURATION



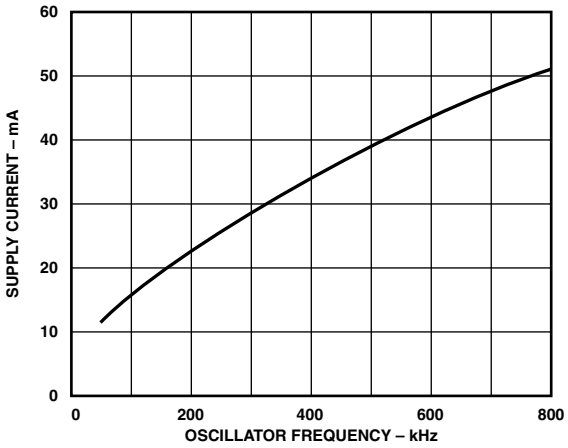
ORDERING GUIDE

Model	Temperature Range	Package Option
ADP3171JR	0°C to 70°C	SO-14

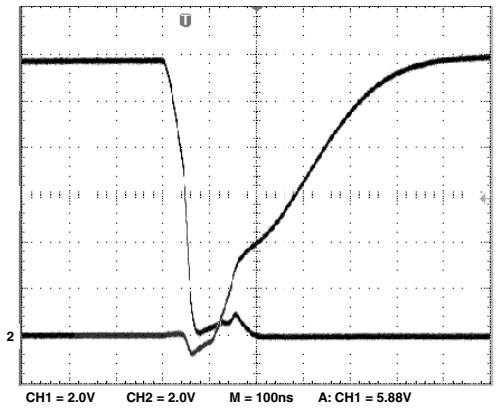
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3171 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

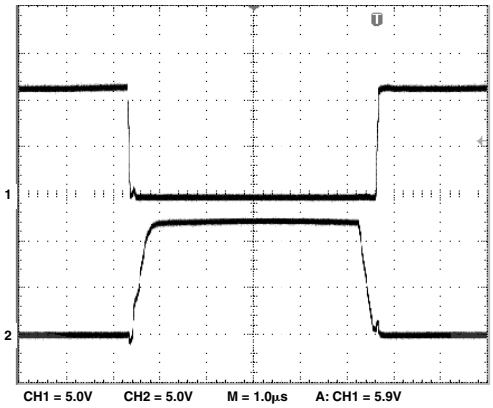
ADP3171–Typical Performance Characteristics



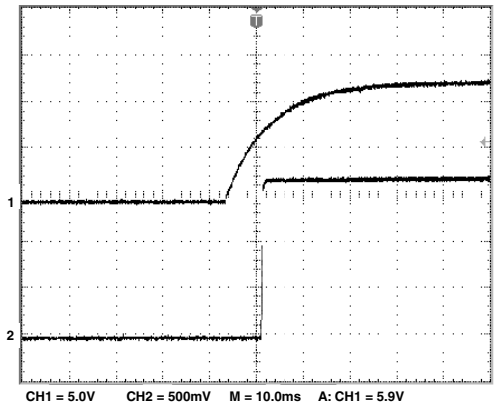
TPC 1. Supply Current vs. Operating Frequency Using MOSFETs of Figure 3



TPC 3. Driver Transition Waveforms Using MOSFETs of Figure 3



TPC 2. Gate Switching Waveforms Using MOSFETs of Figure 3



TPC 4. Power-On Start-Up Waveform

Test Circuits

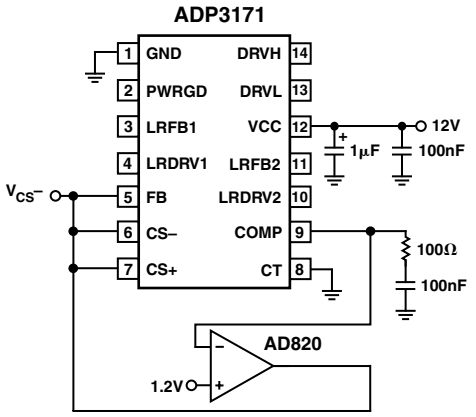


Figure 1. Closed-Loop Output Voltage Accuracy Test Circuit

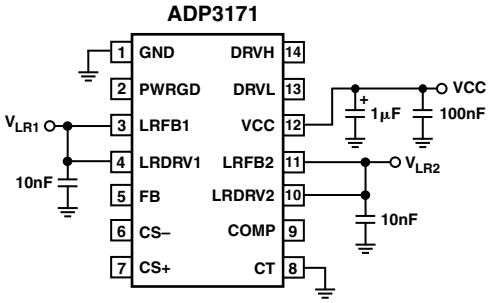


Figure 2. Linear Regulator Output Voltage Accuracy Test Circuit

THEORY OF OPERATION

The ADP3171 uses a current-mode, constant off time control technique to switch a pair of external N-channel MOSFETs in a synchronous buck topology. Constant off time operation offers several performance advantages, including the fact that no slope compensation is required for stable operation. A unique feature of the constant off time control technique is that since the off time is fixed, the converter's switching frequency is a function of the ratio of input voltage to output voltage. The fixed off time is programmed by the value of an external capacitor connected to the CT pin. The on time varies in such a way that a regulated output voltage is maintained as described below in the cycle-by-cycle operation. Under fixed operating conditions, the on time does not vary, and it varies only slightly as a function of load. This means that switching frequency is fairly constant in most applications.

Cycle-by-Cycle Operation

During normal operation (when the output voltage is regulated), the voltage error amplifier and the current comparator are the main control elements. During the on time of the high side MOSFET, the current comparator monitors the voltage between the CS+ and CS– pins. When the voltage level between the two pins reaches the threshold level, the DRVH output is switched to ground, which turns off the high side MOSFET. The timing capacitor CT is then charged at a rate determined by the off time controller. While the timing capacitor is charging, the DRVL output goes high, turning on the low side MOSFET. When the voltage level on the timing capacitor has charged to the upper threshold voltage level, a comparator resets a latch. The output of the latch forces the low side drive output to go low and the high side drive output to go high. As a result, the low side switch is turned off and the high side switch is turned on. The sequence is then repeated. As the load current increases, the output voltage starts to decrease. This causes an increase in the output of the voltage error amplifier, which, in turn, leads to an increase in the current comparator threshold, thus tracking the load current. To prevent cross conduction of the external MOSFETs, feedback is incorporated to sense the state of the driver output pins. Before the low side drive output can go high, the high side drive output must be low. Likewise, the high side drive output is unable to go high while the low side drive output is high.

Output Crowbar

An added feature of using an N-channel MOSFET as the synchronous switch is the ability to crowbar the output with the same MOSFET. If the output voltage is 20% greater than the targeted value, the ADP3171 will turn on the lower MOSFET, which will current-limit the source power supply or blow its fuse, pull down the output voltage, and thus protect the load from overvoltage destruction. The crowbar function releases at approximately 50% of the nominal output voltage. For example, if the output exceeds 1.44 V, the crowbar will turn on the lower MOSFET. If the output is then pulled down to less than 0.6 V, the crowbar will release, allowing the output voltage to recover to 1.2 V if the fault condition has been removed.

On-Board Linear Regulator Controllers

The ADP3171 includes two linear regulator controllers to provide a low cost solution for generating additional supply rails. These regulators are internally set to 1.5 V (LR1) and 1.8 V (LR2). The output voltage is sensed by the high input impedance LRFB(x) pin and compared to an internal fixed reference. The LRDRV(x) pin controls the gate of an external N-channel MOSFET, resulting in a negative feedback loop. The only additional components required are a capacitor and a resistor for stability. Higher output voltages can be generated by placing a resistor divider between the linear regulator output and its respective LRFB pin. The maximum output load current is determined by the size and thermal impedance of the external power MOSFET that is placed in series with the supply and controlled by the ADP3171.

The linear regulator controllers have been designed so that they remain active even when the switching controller is in UVLO mode to ensure that the output voltages of the linear regulators will track the 3.3 V supply as required by Intel® design specifications. By diode OR-ing the VCC input of the IC to the 5 VSB and 12 V supplies as shown in Figure 3, the switching output will

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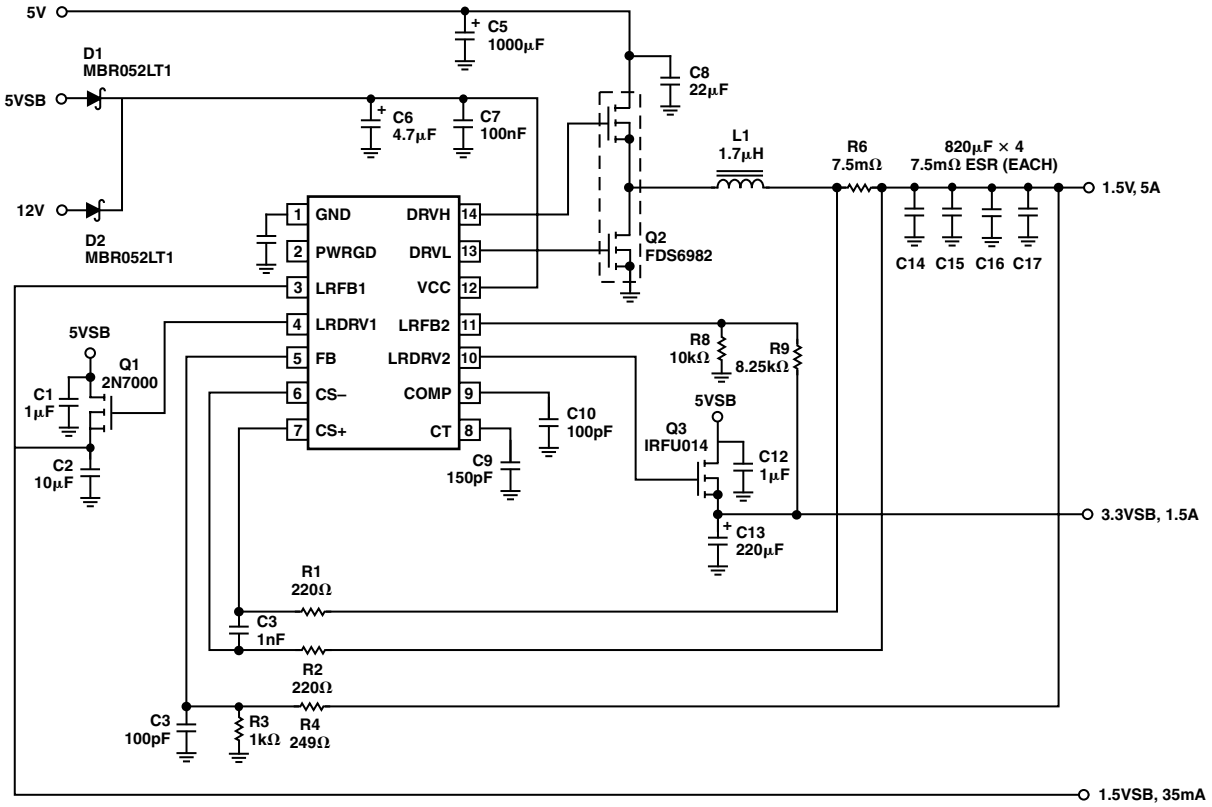

Figure 3. Pentium® III Auxiliary Supply Generating 1.5 V, 1.5 V Standby, and 3.3 V Standby

be disabled in standby mode, but the linear regulators will begin conducting once VCC rises above about 1 V. During startup, the linear outputs will track the 3.3 V supply up until they reach their respective regulation points, regardless of the state of the 12 V supply. Once the 12 V supply has exceeded the 5 VSB supply, the controller IC will track the 12 V supply. Once the 12 V supply has risen above the UVLO value, the switching regulator will begin its start-up sequence.

APPLICATION INFORMATION

Specifications for a Design Example

The design parameters for a typical auxiliary supply for a Pentium III application (shown in Figure 3) are as follows:

Input Voltage: (V_{IN}) = 5 V

Auxiliary Input: (V_{CC}) = 12 V

Main Output: (V_{OUT}) = 1.5 V @ 5 A

LDO 1 Output: (1.5 VSB) = 1.5 V @ 35 mA

LDO 2 Output: (3.3 VSB) = 3.3 V @ 1.5 A

CT Selection for Operating Frequency

The ADP3171 uses a constant off time architecture, with t_{OFF} determined by an external timing capacitor CT. Each time the high side N-channel MOSFET switch turns on, the voltage across CT is reset to approximately 0 V. During the off time, CT is charged by a constant current of 150 µA. Once CT reaches 3.0 V, a new on time cycle is initiated. The value of the off time is calculated using the continuous-mode operating frequency. Assuming a nominal operating frequency (f_{NOM}) of 200 kHz at an output voltage of 1.5 V, the corresponding off time is:

$$t_{OFF} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{1}{f_{NOM}}$$
$$t_{OFF} = \left(1 - \frac{1.5\,V}{5\,V}\right) \times \frac{1}{200\,kHz} = 3.5\,\mu s \quad (1)$$

The timing capacitor can be calculated from the equation:

$$C_T = \frac{t_{OFF} \times I_{CT}}{V_{T(TH)}} = \frac{3.5\,\mu s \times 150\,\mu A}{3V} = 175\ pF \quad (2)$$

$$f_{MIN} = \frac{1}{t_{OFF}} \times \frac{V_{IN} - I_{O(MAX)} \times (R_{DS(ON)HSF} + R_{SENSE} + R_L) - V_{OUT}}{V_{IN} - I_{O(MAX)} \times (R_{DS(ON)HSF} + R_{SENSE} + R_L - R_{DS(ON)LSF})}$$
$$f_{MIN} = \frac{1}{3.5\,\mu s} \times \frac{5V - 5\,A \times (15\,m\Omega + 7.5\,m\Omega + 3\,m\Omega) - 1.5V}{5V - 5\,A \times (15\,m\Omega + 7.5\,m\Omega + 3\,m\Omega - 28\,m\Omega)} = 192\,kHz \quad (3)$$

The nearest standard value is 150 pF. The converter operates at the nominal operating frequency only at the above specified V_{OUT} and at light load. At higher values of V_{OUT}, or under heavy load, the operating frequency decreases due to the parasitic voltage drops across the power devices. The actual minimum frequency at V_{OUT} = 1.5 V is calculated to be 192 kHz (see Equation 3), where:

$R_{DS(ON)HSF}$ is the resistance of the high side MOSFET (estimated value: 15 mΩ)

$R_{DS(ON)LSF}$ is the resistance of the low side MOSFET (estimated value: 28 mΩ)

R_{SENSE} is the resistance of the sense resistor (estimated value: 7.5 mΩ)

R_L is the resistance of the inductor (estimated value: 3 mΩ)

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Inductance Selection

The choice of inductance determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and the conduction losses in the MOSFETs but allows using smaller size inductors and, for a specified peak-to-peak transient deviation, output capacitors with less total capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but requires larger size inductors and more output capacitance for the same peak-to-peak transient deviation. The following equation shows the relationship between the inductance, oscillator frequency, peak-to-peak ripple current in an inductor, and input and output voltages:

$$L = \frac{V_{OUT} \times t_{OFF}}{I_{L(RIPPLE)}} \quad (4)$$

For 2.5 A peak-to-peak ripple current, which corresponds to approximately 50% of the 5 A full-load dc current in an inductor, Equation 4 yields an inductance of:

$$L = \frac{1.5\,V \times 3.5\,\mu s}{2.5\,A} = 2.1\,\mu H$$

A 1.7 µH inductor can be used, which gives a calculated ripple current of 3 A at no load. The inductor should not saturate at the peak current of 8 A and should be able to handle the sum of the power dissipation caused by the average current of 5 A in the winding and the core loss.

Designing an Inductor

Once the inductance is known, the next step is either to design an inductor or find a standard inductor that comes as close as possible to meeting the overall design goals. The first decision in designing the inductor is to choose the core material. There are several possibilities for providing low core loss at high frequencies. Two examples are the powder cores (e.g., Kool Mu® from Magnetics, Inc.) and the gapped soft ferrite cores (e.g., 3F3 or 3F4 from Philips). Low-frequency powdered iron cores should be avoided due to their high core loss, especially when the inductor value is relatively low and the ripple current is high.

Two main core types can be used in this application. Open magnetic loop types such as beads, beads on leads, and rods and slugs, provide lower cost but do not have a focused magnetic field in the core. The radiated EMI from the distributed magnetic field may create problems with noise interference in the circuitry surrounding the inductor. Closed-loop types such as pot cores, PQ, U, and E cores, or toroids, cost more but have much better EMI/RFI performance. A good compromise between price and performance are cores with a toroidal shape.

There are many useful references for quickly designing a power inductor. Table I gives some examples.

Table I. Magnetics Design References

Magnetic Designer Software Intusoft (www.intusoft.com)
Designing Magnetic Components for High-Frequency DC-DC Converters; by William T. McLyman, Kg Magnetics ISBN 1-883107-00-08

Selecting a Standard Inductor

The companies listed in Table II can provide design consultation and deliver power inductors optimized for high power applications upon request.

Table II. Power Inductor Manufacturers

Coilcraft (847) 639-6400 www.coilcraft.com
Coiltronics (561) 752-5000 www.coiltronics.com
Sumida Electric Company (510) 668-0660 www.sumida.com
Vishay-Dale (203) 452-5664 www.vishay.com

R_{SENSE}

The value of R_{SENSE} is based on the required maximum output current. The current comparator of the ADP3171 has a minimum threshold of 69 mV. Note that this minimum value cannot be used for the maximum specified nominal current, as headroom is needed for ripple current and transients.

The current comparator threshold sets the peak of the inductor current yielding a maximum output current, $I_{O(MAX)}$, which equals the peak value less half of the peak-to-peak ripple current. Solving for R_{SENSE} allowing a 20% margin for overhead and using the minimum current sense threshold of 69 mV yields:

$$R_{SENSE} = \frac{V_{CS(TH)(MIN)}}{I_{O(MAX)} + \frac{I_{RIPPLE}}{2}} = \frac{69\,mV}{5\,A + \frac{3\,A}{2}} = 10.6\,m\Omega \quad (5)$$

In this case, 7.5 mΩ was chosen to provide ample headroom. Once R_{SENSE} has been chosen, the maximum output current at the point where current limit is reached, $I_{OUT(CL)}$, can be calculated using the maximum current sense threshold of 87 mV:

$$I_{OUT(CL)} = \frac{V_{CS(TH)(MAX)}}{R_{SENSE}} - \frac{I_{L(RIPPLE)}}{2}$$
$$I_{OUT(CL)} = \frac{87\,mV}{7.5\,m\Omega} - \frac{3\,A}{2} = 10.1\,A \quad (6)$$

At output voltages below 450 mV, the current sense threshold is reduced to 54 mV, and the ripple current is negligible. Therefore, the worst-case dead short output current is reduced to:

$$I_{OUT(SC)} = \frac{V_{CS(SC)}}{R_{SENSE}} = \frac{54\,mV}{7.5\,m\Omega} = 7.2\,A \quad (7)$$

To safely carry the current under maximum load conditions, the sense resistor must have a power rating of at least:

$$P_{R_{SENSE}} = I_O^{\,2} \times R_{SENSE} = 5\,A^2 \times 7.5\,m\Omega = 188\,mW \quad (8)$$

Setting the Switcher Output Voltage

For this example, the resistor divider R3 and R4 set the output voltage at 1.5 V by comparing the divided-down output to the internal 1.2 V reference using:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R4}{R3}\right) \tag{9}$$

C_{OUT} Selection

The selection of C_{OUT} is driven by the required effective series resistance (ESR) and the desired output ripple. A good rule of thumb is to limit the ripple voltage to 1% of the nominal output voltage. It is assumed that the total ripple has two main contributors: 25% from the C_{OUT} bulk capacitance value and 75% from the C_{OUT} ESR value. The correct value for C_{OUT} can be determined by:

$$C_{OUT} = \frac{\Delta I_{OUT} \times t_{OFF}}{0.25 \times \Delta V_{PP}} \tag{10}$$

and:

$$ESR = \frac{0.75 \times \Delta V_{PP}}{\Delta I_{OUT}} \tag{11}$$

where:

$$\Delta I_{OUT} = \frac{V_{OUT} \times t_{OFF}}{L_{OUT}} \tag{12}$$

and:

$$\Delta V_{PP} = 0.01 \times V_{OUT} \tag{13}$$

Solving for this example:

$$\Delta V_{PP} = 0.01 \times 1.5\,V = 15\,mV$$
$$\Delta I_{OUT} = \frac{1.5\,V \times 3.5\,\mu s}{1.7\,\mu H} = 3\,A$$
$$ESR = \frac{0.75 \times 15\,mV}{3\,A} = 3.75\,m\Omega$$
$$C_{OUT} = \frac{3\,A \times 3.5\,\mu s}{0.25 \times 15\,mV} = 2800\,\mu F$$

Four OSCON 820 µF/4 V capacitors would meet these requirements, giving a total capacitance of 3280 µF and an ESR of 3 mΩ. Manufacturers such as Vishay, AVX, Elna, WIMA, and Sanyo provide good high-performance capacitors. Sanyo's OSCON capacitors have lower ESR for a given size at a somewhat higher price. Choosing sufficient capacitors to meet the ESR requirement for C_{OUT} will normally exceed the amount needed to meet the ripple current requirement.

Feedback Loop Compensation Design

Once the output capacitor C_{OUT} and ESR values have been chosen, the output circuit's pole (f_P) and zero (f_Z) frequencies can be calculated using:

$$f_P = \frac{1}{2\,\pi \times C_{OUT} \times (R_{OUT} + ESR)} \tag{14}$$

$$f_Z = \frac{1}{2\,\pi \times C_{OUT} \times ESR} \tag{15}$$

where:

$$R_{OUT} = \frac{V_{OUT}}{I_{OUT}} \tag{16}$$

For this example:

$$R_{OUT} = \frac{1.5\,V}{5\,A} = 0.3\,\Omega$$
$$f_P = \frac{1}{2\,\pi \times 3280\,\mu F \times (0.3\,\Omega + 3\,m\Omega)} = 160\,Hz$$
$$f_P = \frac{1}{2\,\pi \times 3280\,\mu F \times 3\,m\Omega} = 16.2\,kHz$$

The compensation circuit is simply a capacitor (C_C) connected to the COMP pin. This makes the converter have a fast dynamic response to load changes.

The switching frequency of the converter is 200 kHz. The crossover frequency (f_C) should be chosen at one-third the switching frequency, or 70 kHz. The total gain of the compensation circuit (K) is:

$$K = \frac{g_m}{2\,\pi \times n_i \times C \times R_S \times f_C} \tag{17}$$

where error amplifier transconductance (g_m) is 2.2 mmho, the error amplifier gain (n_i) is 25, and the sense resistor (R_S) is 7.5 mΩ. The value of K is determined using the gain of the power output circuit at f_C. The relationship between gain (G_O) at f_C, ESR, and K is:

$$G_O = ESR$$
$$K \times G_O = 1 \tag{18}$$
$$K = \frac{1}{G_O} = \frac{1}{ESR}$$

As K is now known, the value of C_C can be determined by rearranging Equation 17 as follows:

$$C_C = \frac{g_m \times ESR}{2\,\pi \times n_i \times R_S \times f_C}$$
$$C_C = \frac{2.2\,mmho \times 3\,m\Omega}{2\,\pi \times 25 \times 7.5\,m\Omega \times 70\,kHz} = 80\,pF \tag{19}$$

The closest standard value is 100 pF.

Power MOSFETs

Two external N-channel power MOSFETs must be selected for use with the ADP3171, one for the main switch and one for the synchronous switch. The main selection parameters for the power MOSFETs are the threshold voltage ($V_{GS(TH)}$), the ON resistance ($R_{DS(ON)}$), and the gate charge (Q_G). Logic level MOSFETs are highly recommended. Only logic level MOSFETs with V_{GS} ratings higher than the absolute maximum value of V_{CC} should be used.

The maximum output current $I_{O(MAX)}$ determines the $R_{DS(ON)}$ requirement for the two power MOSFETs. When the ADP3171 is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the average load current. For V_{IN} = 5 V and V_{OUT} = 1.5 V, the maximum duty ratio of the high-side FET is:

$$D_{HSF(MAX)} = 1 - \left(f_{MIN} + t_{OFF}\right)$$
$$D_{HSF(MAX)} = 1 - \left(192\,kHz \times 3.5\,\mu s\right) = 33\% \quad (20)$$

The maximum duty ratio of the low-side (synchronous rectifier) MOSFET is:

$$D_{LSF(MAX)} = 1 - D_{HSF(MAX)} = 67\% \quad (21)$$

The maximum rms current of the high-side MOSFET is:

$$I_{HSF(MAX)} = \sqrt{D_{HSF(MAX)} \times \frac{I_{L(VALLEY)}{}^2 + (I_{L(VALLEY)} \times I_{L(PEAK)}) + I_{L(PEAK)}{}^2}{3}}$$
$$I_{HSF(MAX)} = \sqrt{0.33 \times \frac{3.75\,A^2 + (3.75\,A \times 6.25\,A) + 6.25\,A^2}{3}} = 2.9\,A \quad (22)$$

The maximum rms current of the low-side MOSFET is:

$$I_{LSF(MAX)} = \sqrt{D_{LSF(MAX)} \times \frac{I_{L(VALLEY)}{}^2 + (I_{L(VALLEY)} \times I_{L(PEAK)}) + I_{L(PEAK)}{}^2)}{3}}$$
$$I_{LSF(MAX)} = \sqrt{0.67 \times \frac{3.75\,A^2 + \left((3.75\,A \times 6.25\,A) + 6.25\,A^2\right)}{3}} = 4.1\,A \quad (23)$$

The $R_{DS(ON)}$ for each MOSFET can be derived from the allowable dissipation. If 10% of the maximum output power is allowed for MOSFET dissipation, the total dissipation will be:

$$P_{D(FETs)} = 0.1 \times V_{OUT} \times I_{OUT(MAX)}$$
$$P_{D(FETs)} = 0.1 \times 1.5\,V \times 6.5\,A = 975\,mW \quad (24)$$

Allocating half of the total dissipation for the high-side MOSFET and half for the low-side MOSFET, and assuming that the resistive loss of the high-side MOSFET is one-third and the switching loss is two-thirds of its total, the required maximum MOSFET resistances will be:

$$R_{DS(ON)HSF} = \frac{P_{D(FETs)}}{3 \times I_{HSF(MAX)}{}^2} = \frac{975\,mW}{3 \times 2.9\,A^2} = 38\,m\Omega \quad (25)$$

$$R_{DS(ON)LSF} = \frac{P_{D(FETs)}}{2 \times I_{LSF(MAX)}{}^2} = \frac{975\,mW}{2 \times 4.1\,A^2} = 29\,m\Omega \quad (26)$$

Note that there is a trade-off between converter efficiency and cost. Larger MOSFETs reduce the conduction losses and allow higher efficiency, but increase the system cost. A Fairchild FDB6982 dual MOSFET (high-side $R_{DS(ON)}$ = 28 mΩ nominal, 35 mΩ worst-case; and low-side $R_{DS(ON)}$ = 16 mΩ nominal, 22 mΩ worst-case) is a good choice in this application.

With this choice, the high-side MOSFET dissipation is:

$$P_{HSF} = R_{DS(ON)HSF} \times I_{HSF(MAX)}{}^2 + \frac{V_{IN} \times I_{L(PEAK)} \times Q_G \times f_{MIN}}{2 \times I_G}$$
$$+V_{IN} \times Q_{RR} \times f_{MIN}$$
$$P_{HSF} = 35\,m\Omega \times 2.9\,A^2 + \frac{5 + 6.25\,A \times 12\,nC \times 192\,kHz}{2 \times 1\,A}$$
$$+5\,V \times 19\,nC \times 192\,kHz = 349\,mW \quad (27)$$

where the second term represents the turn-off loss of the MOSFET and the third term represents the turn-on loss due to the stored charge in the body diode of the low-side MOSFET. In the second term, Q_G is the gate charge to be removed from the gate for turn-off and I_G is the gate turn-off current. From the data sheet, the value of Q_G for the FDS6982 is 12 nC and the peak gate drive current provided by the ADP3171 is about 1 A. In the third term, Q_{RR} is the charge stored in the body diode of the low-side MOSFET at the valley of the inductor current. The data sheet of the FDS6982 shows a value of 19 nC for this parameter.

The low-side MOSFET dissipation is:

$$P_{LSF} = R_{DS(ON)LSF} \times I_{LSF(MAX)}{}^2$$
$$P_{LSF} = 22\,m\Omega \times 4.1\,A^2 = 370\,mW \quad (28)$$

Note that there are no switching losses in the low-side MOSFET.

C_{IN} Selection and Input Current di/dt Reduction

In continuous inductor-current mode, the source current of the high-side MOSFET is a square wave with a duty ratio of V_{OUT}/V_{IN} and an amplitude of one-half of the maximum output current. To prevent large voltage transients, a low ESR input capacitor sized for the maximum rms current must be used. The maximum rms capacitor current is given by:

$$I_{C(RMS)} = I_O \times \sqrt{D_{HSF} - D_{HSF}{}^2}$$
$$I_{C(RMS)} = 5\,A \times \sqrt{0.33 - 0.33^2} = 2.4\,A \quad (29)$$

For a ZA-type capacitor with 1000 µF capacitance and 6.3 V voltage rating, the ESR is 24 mΩ and the maximum allowable ripple current at 100 kHz is 2 A. At 105°C, at least two such capacitors should be connected in parallel to handle the calculated ripple current. At 50°C ambient, however, a higher ripple current can be tolerated, so one capacitor is adequate.

The ripple voltage across the input capacitor is:

$$V_{C(RIPPLE)} = I_O \times \left(\frac{ESR_C}{n_C} + \frac{D_{HSF(MAX)}}{n_C \times C_{IN} \times f_{MIN}}\right)$$
$$V_{C(RIPPLE)} = I_O \times \left(\frac{24\,m\Omega}{1} + \frac{0.33}{1 \times 1\,mF \times 192\,kHz}\right) = 26\,mV \quad (30)$$

Linear Regulators

The linear regulators provide a low-cost, convenient, and versatile solution for generating moderate current supply rails. The maximum output load current is determined by the size and thermal impedance of the external N-channel power MOSFET that is placed in series with the supply and controlled by the ADP3171. The output voltage is sensed at the LRFB × pin and compared to an internal reference voltage in a negative feedback loop that keeps the output voltage in regulation. If the load is reduced or

increased, the MOSFET drive will also be reduced or increased by the ADP3171 to provide a well regulated output voltage. Output voltages higher than the fixed internal reference voltage can be programmed by adding an external resistor divider. The correct resistor values for setting the output voltage of the linear regulators in the ADP3171 can be determined using:

$$V_{OUT\,(LR)} = V_{LRFB\,(X)} \times \frac{R_U + R_L}{R_L} \quad (31)$$

Assuming that R_L = 10 kΩ, $V_{OUT(LR)}$ = 3.3 V and rearranging Equation 31 to solve for R_U yields:

$$R_U = \frac{10\ k\Omega \times \left(V_{OUT(LR)} - V_{LRFB\,2}\right)}{V_{LRFB\,2}}$$
$$R_U = \frac{10\ k\Omega \times \left(3.3\ V - 1.8\ V\right)}{1.8\ V} = 8.33\ k\Omega \quad (32)$$

The closest 1% resistor value is 8.25 kΩ.

Efficiency of the Linear Regulators

The efficiency and corresponding power dissipation of each of the linear regulators are not determined by the ADP3171. Rather, these are a function of input and output voltage and load current. Efficiency is approximated by the formula:

$$\eta = 100\% \times \frac{V_{OUT}}{V_{IN}} \quad (33)$$

The corresponding power dissipation in the MOSFET, together with any resistance added in series from input to output, is given by:

$$P_{LDO} = \left(V_{IN} - V_{OUT}\right) \times I_{OUT} \quad (34)$$

Minimum power dissipation and maximum efficiency are accomplished by choosing the lowest available input voltage that exceeds the desired output voltage. However, if the chosen input source is itself generated by a linear regulator, its power dissipation will be increased in proportion to the additional current it must now provide.

LAYOUT AND COMPONENT PLACEMENT GUIDELINES

The following guidelines are recommended for optimal performance of a switching regulator in a PC system:

General Recommendations

1. For best results, a four-layer PCB is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, a signal ground plane, power planes for both power ground and the input power (e.g., 5 V), and wide interconnection traces in the rest of the power delivery current paths.
2. Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. If critical signal lines (including the voltage and current sense lines of the ADP3171) must cross through power circuitry, it is best if a ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.
4. The GND pin of the ADP3171 should connect first to a ceramic bypass capacitor (on the VCC pin) and then into the analog ground plane. The analog ground plane should be located below the ADP3171 and the surrounding small signal components such as the timing capacitor and compensation network. The analog ground plane should connect to power ground plane at a single point; the best location being the negative terminal of the last output capacitor.
5. The output capacitors should also be connected as closely as possible to the load (or connector) that receives the power (e.g., a microprocessor core). If the load is distributed, the capacitors also should be distributed, and generally in proportion to where the load tends to be more dynamic. It is also advised to keep the planar interconnection path short (i.e., have input and output capacitors close together).
6. Absolutely avoid crossing any signal lines over the switching power path loop, described below.

Power Circuitry

7. The switching power path should be routed on the PCB to encompass the smallest possible area in order to minimize radiated switching noise energy (i.e., EMI). Failure to take proper precaution often results in EMI problems for the entire PC system as well as noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors, the two FETs, and the power Schottky diode, if used, including all interconnecting PCB traces and planes. The use of short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing, and it accommodates the high current demand with minimal voltage loss.
8. A power Schottky diode (1 ~ 2 A dc rating) placed from the lower MOSFET's source (anode) to drain (cathode) will help to minimize switching power dissipation in the upper MOSFET. In the absence of an effective Schottky diode, this dissipation occurs through the following sequence of switching events. The lower MOSFET turns off in advance of the upper MOSFET turning on (necessary to prevent cross conduction). The circulating current in the power converter, no longer finding a path for current through the channel of the lower MOSFET, draws current through the inherent body-drain diode of the MOSFET. The upper MOSFET turns on, and the reverse recovery characteristic of the lower MOSFET's body-drain diode prevents the drain voltage from being pulled high quickly. The upper MOSFET then conducts very large current while it momentarily has a high voltage forced across it, which translates into added power dissipation in the upper MOSFET. The Schottky diode minimizes this problem by carrying a majority of the circulating current when the lower MOSFET is turned off, and by virtue of its essentially nonexistent reverse recovery time.
9. Whenever a power dissipating component (e.g., a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are:

improved current rating through the vias (if it is a current path), and improved thermal performance—especially if the vias extended to the opposite side of the PCB where a plane can more readily transfer the heat to the air.

10. The output power path, though not as critical as the switching power path, should also be routed to encompass a small area. The output power path is formed by the current path through the inductor, the current sensing resistor, the output capacitors, and back to the input capacitors.
11. For best EMI containment, the ground plane should extend fully under all the power components. These are the input capacitors, the power MOSFETs and Schottky diode, the inductor, the current sense resistor, any snubbing elements that might be added to dampen ringing, and the output capacitors.

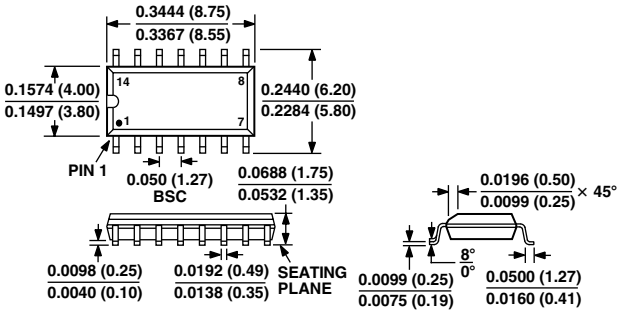
Signal Circuitry

12. The output voltage is sensed and regulated between the GND pin (which connects to the signal ground plane) and the FB– pin. The output current is sensed (as a voltage) and regulated between the CS– pin and the CS+ pin. In order to avoid differential mode noise pickup in those sensed signals, their loop areas should be small. Thus the FB– trace should be routed atop the signal ground plane, and the CS+ and CS– traces should be routed as a closely coupled pair (CS+ should be over the signal ground plane as well).
13. The CS+ and CS– traces should be Kelvin connected to the current sense resistor so that the additional voltage drop due to current flow on the PCB at the current sense resistor connections does not affect the sensed voltage. It is desirable to have the ADP3171 close to the output capacitor bank and not in the output power path, so that any voltage drop between the output capacitors and the GND pin is minimized, and voltage regulation is not compromised.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

14-Lead Narrow SOIC
(R-14)



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