2-Phase IMVP-II & IMVP-III Core Controller for Mobile CPUs

Preliminary Technical Data — ADP3203

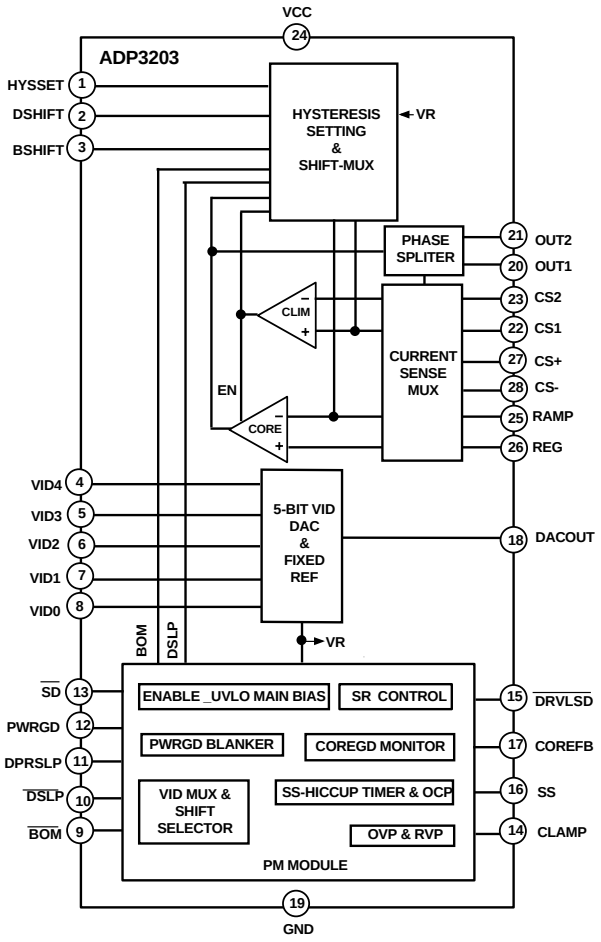
FEATURES

- Pin Selectable 1 or 2-Phase Operation
- Backward Compatible to IMVP-II
- Excellent Static and Dynamic Current Sharing
- Superior Load Transient Response with ADOPT™ Optimal Positioning Technology
- Noise-Blanking for Speed and Stability
- Synchronous Rectifier Control for Extended Battery Life
- Cycle-by-Cycle Current Limiting
- Hiccup or Latched Overload Protection
- Transient-Glitch-Free Power Good
- Soft Start Eliminates Power-On In-Rush Current Surge
- Two-Level Over-Voltage and Reverse-Voltage Protection

APPLICATIONS

- IMVP II-III Core DC/DC Converters
- Fixed Voltage Mobile CPU Core DC/DC Converters
- Notebook/Laptop Power Supplies
- Programmable Output Power Supplies

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3203 is a 1 or 2-phase hysteretic peak current DC-DC buck converter controller dedicated to power a mobile processor's core. The optimized low voltage design is powered from the 3.3 V system supply and draws only 10 μA maximum in shutdown. The nominal output voltage is set by a 5-bit VID code. To accommodate the transition time required by the newest processors for on-the-fly VID changes, the ADP3203 features high-speed operation to allow a minimized inductor size that results in the fastest change of current to the output. To further allow for the minimum number of output capacitors to be used, the ADP3203 features active voltage positioning with ADOPT™ optimal compensation to ensure a superior load transient response. The output signal interfaces with the ADP3415 MOSFET driver that is optimized for high speed and high efficiency for driving both the top and bottom MOSFETs of the buck converter. The ADP3203 is capable of controlling the synchronous rectifier to extend battery lifetime in light load conditions.

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ADP3203–SPECIFICATIONS[1]

(T_A = 25 °C, High (H) = VCC, Low (L) = 0 V, VCC = 3.3 V, $\overline{SD}$ = H, V_{COREFB} = V_{DAC} (≡ V_{DACOUT}), V_{REG} = V_{CS-} = V_{VID} = 1.25 V, R_{OUT} = 100 kΩ, C_{OUT} = 10 pF, C_{SS} = 47 nF, R_{PWRGD} = 680 Ω to 1.2 V, R_{CLAMP} = 5.1 kΩ to VCC, HYSSET, BSHIFT, DSHIFT are open, $\overline{BOM}$ = H, $\overline{DSLP}$ = H, DPRSLP = L, unless otherwise noted) Current sunk by a pin has a positive sign, sourced by a pin has a negative sign. Negative sign is disregarded for min and max values.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SUPPLY-UVLO-SHUTDOWN						
Normal Supply Current	I_{CC}			7	15	mA
UVLO Supply Current	I_{CCUVLO}				425	µA
Shutdown Supply Current	I_{CCSD}	$\overline{SD}$ = L, 3.0 V ≤ VCC ≤ 3.6 V		10		µA
UVLO Threshold		$\overline{SD}$ = H				
	V_{CCH}	V_{CC} ramping up, V_{SS}= 0 V			2.9	V
	V_{CCL}	V_{CC} ramping down, V_{SS} floating	2.65			V
UVLO Hysteresis	V_{CCHYS}		50			mV
Shutdown Threshold (CMOS Input)	V_{SDTH}			V_{CC}/2		V
POWERGOOD-CORE FEEDBACK						
Core Feedback Threshold Voltage	$V_{COREFBH}$	0.9 V < V_{DAC} < 1.675 V				
		V_{COREFB} ramping up	1.12 V_{DAC}		1.14 V_{DAC}	V
		V_{COREFB} ramping down	1.10 V_{DAC}		1.12 V_{DAC}	V
		V_{COREFB} ramping up	0.88 V_{DAC}		0.90 V_{DAC}	V
		V_{COREFB} ramping down	0.86 V_{DAC}		0.88 V_{DAC}	V
Power Good Output Voltage	V_{PWRGD}	V_{COREFB} = V_{DACOUT}	0.95 V_{CC}		V_{CC}	V
(open drain output)		V_{COREFB} = 0.8 V_{DACOUT}	0		0.8	V
Masking Time[2]	$t_{PWRGD,MSK}$[6]	V_{CC} = 3.3 V		100		µs
SOFT-START/HICCUP TIMER						
Charge/Discharge Current	I_{SS}	V_{SS} = 0 V		–16		µA
		V_{SS} = 0.5 V		0.5		µA
Soft-Start Enable/Hiccup Termination Threshold		V_{REG} = 1.25 V, V_{RAMP} = V_{COREFB} = 1.27 V				
	$V_{SSENDWN}$	V_{SS} ramping down		80	200	mV
	V_{SSENUP}[7]	V_{SS} ramping up		150		mV
Soft-Start Termination/Hiccup Enable Threshold	V_{SSTERM}	V_{RAMP} = V_{COREFB} = 1.27 V, V_{SS} ramping up	1.75	2.00	2.25	V
VID DAC						
VID Input Threshold (CMOS Inputs)	$V_{VID0..4}$			V_{CC}/2		V
VID Input Current (Internal Active Pull-up)	$I_{VID0..4}$	VID 0..4 = L		90		µA
Output Voltage	V_{DAC}	See VID Code Table 1	0.600		1.750	V
Accuracy	$\Delta V_{DAC}/V_{DAC}$	0.850 V < V_{DAC} < 1.750 V	–1.0		+1.0	%
		0.600 V < V_{DAC} < 0.825 V	–8.5		+8.5	mV
Settling Time[2]	t_{DACS}[3]	ΔV_{DAC} = 0.5 V, C_{DAC} = 10 nF		3.5		µs

Notes:
[1] All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
[2] Guaranteed by characterization.
[3] Measured from 50% of VID code transition amplitude to the point where V_{DACOUT} settles within ±1% of its steady state value.
[4] 40 mV_{PP} amplitude impulse with 20 mV overdrive. Measured from the input threshold intercept point to 50% of the output voltage swing.
[5] Measured between the 30% and 70% points of the output voltage swing.
[6] Two test conditions: 1)PWRGD is OK but forced to fail by applying an out-of-the-CoreGood-window voltage ($V_{COREFB,BAD}$ = 1.0 V at V_{VID} = 1.25 V setting) to the COREFB pin right after the moment that $\overline{BOM}$ or DPRSLP is asserted/de-asserted. PWRGD should not fail immediately only with the specified blanking delay time. 2) PWRGD is forced to fail ($V_{COREFB,BAD}$ = 1.0 V at V_{VID} = 1.25 V setting) but gets into the CoreGood-window ($V_{COREFB,GOOD}$ = 1.25 V) right after the moment that $\overline{BOM}$ or DPRSLP is asserted/de-asserted. PWRGD should not go high immediately only with the specified blanking delay time.
[7] Guaranteed by design.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CORE COMPARATOR						
Input Offset Voltage (Ramp-Reg)	V_{COREOS}	V_{REG} = 1.25 V		±1.5		mV
Input Bias Current	I_{REG}, I_{RAMP}	V_{REG} = V_{RAMP} = 1.25 V		±1		µA
Output Voltage (OUT1,OUT2)	V_{OUT_H}	V_{CC} = 3.0 V	2.5		3.0	V
	V_{OUT_L}	V_{CC} = 3.6 V	0		0.8	V
Propagation Delay Time[2]	t_{RMPOUT_PD}[4]	T_A = 25°C			30	ns
		T_A = Full Range			40	ns
Rise and Fall Time[2]	t_{OUT_R}[5]			7	10	ns
	t_{OUT_F}[5]			7	10	ns
Noise Blanking Time[2]	t_{BLNK}	OUT L-H Transition		80		ns
		OUT H-L Transition		120		ns
CURRENT LIMIT COMPARATOR						
Input Offset Voltage	V_{CLIMOS}	V_{CS-} = 1.25 V		±4	±6	mV
Input Bias Current	I_{CS+}, I_{CS-}[4]	V_{CS+} = 1.25 V		–5	–3	µA
Propagation Delay Time[2]	t_{CLPD}	T_A = 25° C		30	60	ns
		T_A = Full Range		50	100	ns
CURRENT SENSE MULTIPLEXER						
Trans-Resistance	$R_{CS1-CS+}$,	Switch is ON		150		Ω
	$R_{CS2-CS+}$	Switch is OFF		100		MΩ
Common Mode Voltage Range[7]	V_{CS1} = V_{CS2}		0		2	V
HYSTERESIS SETTING						
Hysteresis Current	I_{RAMP_H}, $-I_{CSP\_H}$	V_{REG} = 1.25 V				
		V_{RAMP} = 1.23 V, $\overline{BOM}$=H				
		I_{HYSSET} = 10 µA	–8	–10	–12	µA
		I_{HYSSET} = 100 µA	–80	–100	–120	µA
		V_{RAMP} = 1.27 V, $\overline{BOM}$ = H				
		I_{HYSSET} = 10 µA	8	10	12	µA
		I_{HYSSET} = 100 µA	80	100	120	µA
		V_{RAMP} = 1.23 V, $\overline{BOM}$ = L				
		I_{HYSSET} = 10 µA	–6.4	–8	–9.6	µA
		I_{HYSSET} = 100 µA	–64	–80	–96	µA
		V_{RAMP} = 1.27 V, $\overline{BOM}$ = L				
		I_{HYSSET} = 10 µA	64	8	96	µA
		I_{HYSSET} = 100 µA	64	80	96	µA
Hysteresis Reference Voltage	V_{HYSSET}		1.53	1.7	1.87	V
CURRENT LIMIT SETTING						
Hysteresis Current	I_{CS-}	V_{RAMP} = 1.23 V				
		V_{REG} = V_{CS-} = V_{COREFB} = 1.25 V				
		V_{CS+} = 1.23 V $\overline{BOM}$ = H				
		I_{HYSSET} = 10 µA	–27	–31.5	–36	µA
		I_{HYSSET} = 100 µA	–268	–301.5	–335	µA
		V_{CS+} = 1.27 V, $\overline{BOM}$ = H				
		I_{HYSSET} = 10 µA	–18	–21.5	–25	µA
		I_{HYSSET} = 100 µA	–178	–201.5	–225	µA
		V_{CS+} = 1.23 V, $\overline{BOM}$ = L				
		I_{HYSSET} = 10 µA	–21	–25.5	–30	µA
		I_{HYSSET} = 100 µA	–212	–241.5	–271	µA
		V_{CS+} = 1.27 V, $\overline{BOM}$ = L				
		I_{HYSSET} = 10 µA	–14	–17.5	–21	µA
		I_{HYSSET} = 100 µA	–140	–161.5	–183	µA

ADP3203–SPECIFICATIONS[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SHIFT SETTING						
Battery-Shift Current	I_{RAMPB},I_{CS+B}	V_{VID} = 1.25 V R_{BSHIFT} = 12.5 k, $\overline{BOM}$ = L $\overline{DSLP}$ = H	–90	–100	–110	µA
Battery-Shift Reference Voltage	V_{BSHIFT}			V_{DAC}		V
DeepSleep-Shift Current	I_{RAMPD},I_{CS+D}	V_{VID} = 1.25 V R_{DSHIFT} = 12.5 k, $\overline{BOM}$ = H $\overline{DSLP}$ = L	–90	–100	–110	µA
DeepSleep-Shift Reference Voltage	V_{DSHIFT}			V_{DAC}		V
SHIFT CONTROL INPUTS						
$\overline{BOM}$ Threshold (CMOS Input)	V_{BOM}			V_{CC}/2		V
$\overline{DSLP}$ Threshold (V_{TT}-Level CMOS Input)	V_{DSLP}			0.9		V
DPRSLP Mode Threshold (CMOS Input)	V_{DPRSLP}			V_{CC}/2		V
LOW-SIDE DRIVE CONTROL						
Output Voltage (CMOS Output)	V_{DRVLSD}	DPRSLP = H	0		0.4	V
		DPRSLP = L	0.7 V_{CC}		V_{CC}	V
Output Current	I_{DRVLSD}	V_{DRVLSD} = 1.5 V DPRSLP = L	0.5			mA
		DPRSLP = H	–0.5			mA
OVER/REVERSE VOLTAGE PROTECTION-CORE FEEDBACK						
Over-Voltage Threshold	$V_{COREFB,OVP}$	V_{COREFB} rising		2.0		V
		V_{COREFB} falling		1.95		V
Reverse-Voltage Threshold	$V_{COREFB,OVP}$	V_{COREFB} falling		–0.3		V
		V_{COREFB} rising		–0.1		V
Output Voltage (Open Drain Output)	V_{CLAMP}		0.7 V_{CC}		V_{CC}	V
Output Current	I_{CLAMP}	V_{CLAMP} = 1.5 V, V_{VID} = 1.25 V V_{COREFB} = V_{DAC}			10	µA
		V_{COREFB} = 2.2 V	1	4		mA

ORDERING GUIDE

Model	DPRSLP Voltage	Temperature Range	Package Option
ADP3203JRU-0.85-RL	0.85 V	0°C to 100°C	TSSOP-28
ADP3203JRU-1.0-RL	1 V	0°C to 100°C	TSSOP-28
ADP3203JRU-1.0-RL7	1 V	0°C to 100°C	TSSOP-28

ABSOLUTE MAXIMUM RATINGS*

Input Supply Voltage (VCC) ..... -0.3 V to +7 V
UVLO Input Voltage ..... -0.3 V to +7 V
All Other Inputs/Outputs ..... VCC + 0.3 V
Operating Ambient Temperature Range ..... 0°C to +100°C
Junction Temperature Range ..... 0°C to +150°C
θ_{JA} ..... 98°C/W
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1	HYSSET	Hysteresis Set. This is an analog I/O pin whose output is a fixed voltage reference and whose input is a current that is programmed by an external resistance to ground. The current is used in the IC to set the hysteretic currents for the Core Comparator and the Current Limit Comparator. Modification of the resistance will affect both the hysteresis of the feedback regulation and the current limit set point and hysteresis.
2	DSHIFT	Deep Sleep Shift. This is an analog I/O pin whose output is the VID reference voltage and whose input is a current that is programmed by an external resistance to ground. The current is used in the IC to set a switched bias current out of the RAMP pin, depending on whether it is activated by the DSLP# signal. When activated, this added bias current creates a downward shift of the regulated core voltage to a predetermined optimum level for regulation corresponding to Deep Sleep mode of CPU operation. The use of the VID code as the reference makes the Deep Sleep offset a fixed percentage of the VID setting, as required by specifications.
3	BSHIFT	Battery Optimized Mode ($\overline{\text{BOM}}$) Shift. This is an analog I/O pin whose output that is the VID reference voltage and whose input current is programmed by an external resistance to ground. The current is used in the IC to set a switched bias current out of the RAMP pin, depending on whether it is activated by the $\overline{\text{BOM}}$ signal. When activated, this added bias current creates a downward shift of the regulated core voltage to a predetermined optimum level for regulation corresponding to Battery Optimized Mode of CPU operation. The use of the VID code as the reference makes the DSHIFT a fixed percentage of the VID setting, as required by specifications.
4–8	VID[4:0]	Voltage Identification Inputs. These are the VID inputs for logic control of the programmed reference voltage that appears at the DACOUT pin, and, via external component configuration, is used for setting the output voltage regulation point. The VID pins have a specified internal pullup current such that, if left open, the pins will default to a logic high state. The VID code does not set the DAC output voltage directly but through a transparent latch which is clocked by the $\overline{\text{BOM}}$ pin's GMUXSEL signal rising and falling edge.
9	$\overline{\text{BOM}}$	Battery Optimized Mode Control (active low). This is a digital input pin that corresponds to the system's GMUXSEL signal that corresponds to Battery Optimized Mode of the CPU operation in its active low state and Performance Optimized Mode (POM) in its deactivated high state. The signal also controls the optimal positioning of the core voltage regulation level by offsetting it downwards in Battery Optimized Mode according to the functionality of the BSHIFT and RAMP pins. It is also used to initiate a masking period for the PWRGD signal whenever a GMUXSEL signal transition occurs.
10	$\overline{\text{DSLP}}$	Deep Sleep Mode Control (active low). This is a digital input pin corresponding to the system's $\overline{\text{STP CPU}}$ signal which, in its active state, corresponds to Deep Sleep mode of the CPU operation, which is a subset operating mode of either BOM or POM operation. The signal controls the optimal positioning of the core voltage regulation level by offsetting it downwards according to the functionality of the DSHIFT and RAMP pins.
11	DPRSLP	Deeper Sleep Mode Control (active high). This is a digital input pin corresponding to the system's DPRSLPVR signal corresponding to Deeper Sleep mode of the CPU operation. The signal when it is activated controls the DAC output voltage by disconnecting the VID signals from the DAC input and setting a specified internal Deeper Sleep code instead. At de-assertion of the DPRSLPVR signal, the DAC output voltage returns to the voltage level determined by the external VID code. The DPRSLPVR signal is also used to initiate a blanking period for the PWRGD signal to disable its response to a pending dynamic core voltage change corresponds to the VID code transition.

Pin	Mnemonic	Function
12	PWRGD	Power Good (active high). This is an open drain output pin which, via the assistance of an external pull-up resistor to the desired voltage, indicates that the core voltage is within the specified tolerance of the VID programmed value or else in a VID transition state as indicated by a recent state transition of either the $\overline{\text{BOM}}$ or DPRSLP pins. PWRGD is deactivated (pulled low) when the IC is disabled or in UVLO mode or starting up, or the COREFB voltage is out of the core powergood window. The open drain output allows external wired ANDing (logical NORing) with other open drain/collector power-good indicators.
13	$\overline{\text{SD}}$	Shutdown (active low). This is a digital input pin coming from a system signal which, in its active state, shuts down the IC operation, placing the IC in its lowest quiescent current state for maximum power savings.
14	CLAMP	Clamp (active high). This is an open drain output pin which, via the assistance of an external pull-up resistor, indicates that the core voltage should be clamped for its protection. To allow the highest level of protection, the CLAMP signal is developed using both a redundant reference and a redundant feedback path with respect to those of the main regulation loop. The signal is timed out using the softstart capacitor, so an external current protection mechanism (e.g., fuse or AC adapter's current limit) should be tripped within ~3 times the programmed soft start time (e.g. 5~10 ms). In a preferred and more conservative configuration, the core voltage is clamped by an external FET. The initial protection function is served when it is activated by detection of either an over-voltage or a reverse-voltage condition on the COREFB pin. A backup protection function due to loss of the latched signal at IC power-off is served by connecting the pull-up resistor to a system "ALWAYS" regulator output (e.g., V5_ALWAYS). If the external FET is used, this implementation will keep the core voltage clamped until the ADP3422 has power re-applied, thus keeping protection for the CPU even after a hard-failure power-down and restart (e.g., a shorted top or bottom FET).
15	$\overline{\text{DRVLSD}}$	Drive-Low Shutdown (active low). This is a digital output pin which, in its active state, indicates that the lower FET of the core VR should be disabled. In the suggested application schematic this pin is directly connected to the pin of the same name on the ADP3415 or other driver IC. Drive-low shutdown is normally activated by the DPRSLP signal, corresponding to a light load condition, but a number of dynamic conditions can override the control of this pin as needed.
16	SS	Soft Start. This is an analog I/O pin whose output is a controlled current source used to charge or discharge an external grounded capacitor and whose input is the detected voltage that is indicative of elapsed time. The pin controls the soft start time of the IC as well as the hiccup cycle time during overload including but not limited to short circuit, over voltage, and reverse voltage. Hiccup operation is a feature that was added to reduce short circuit power dissipation by more than an order of magnitude, while still allowing an automatic restart when the failure mode ceased. The hiccup operation can be overwritten and changed to latched-off operation by clamping the SS pin voltage to a voltage level somewhere above ~ 0.2 V. In this configuration, the controller does not restart after a hiccup cycle is initiated, but stays latched off.
17	COREFB	Core Feedback. This is a high-impedance analog input pin that is used to monitor the output voltage for setting the proper state of the PWRGD and CLAMP pins. It is generally recommended to RC-filter the ripple and noise from the monitored core voltage, as suggested by the application schematic.
18	DACOUT	Digital-to-Analog Converter Output. This output voltage is the VID-controlled reference voltage whose primary function is to determine the output voltage regulation point.
19	GND	Ground.
20	OUT1	Output to Driver 1. This is a digital output pin which is used to command the state of the switched node via the driver and MOSFET switches. It should be connected to the IN pin of the ADP3415 driver that corresponds to the first of two channels.

Pin	Mnemonic	Function
21	OUT2	Output to Driver 2. This is a digital output pin which is used to command the state of the switched node via the driver. It should be connected to the IN pin of the ADP3415 driver that corresponds to the second of two channels.
22	CS1	Current Sense, Channel 1. This is a high-impedance analog input pin which is used for providing negative feedback of the current information for the first of two channels.
23	CS2	Current Sense, Channel 2. This is a high-impedance analog input pin which is used for providing negative feedback of the current information for the second of two channels. The pin is also used to determine whether the chip is acting as a single or dual-phase controller. If the pin is tied to VCC but not a sense resistor then the dual-phase operation is disabled; the chip works as a single phase controller. In this condition the second phase's output signal (OUT2) is not switching but stays static low.
24	VCC	Power supply. This should be connected to the system's 3.3 V power supply output.
25	RAMP	Regulation Ramp Feedback Input. The RAMP pin voltage is compared against the REG pin for cycle-by-cycle switching response. Several switched current sources also appear at this input, the cycle-by-cycle hysteresis-setting switched current programmed by the HYSSET pin, the BOM shift current programmed by the BSHIFT pin, and the Deep Sleep shift current programmed by the DSHIFT pin. The external resistive termination at this pin sets the magnitude of the hysteresis applied to the regulation loop.
26	REG	Regulation Voltage Summing Input. This is a high-impedance analog input pin into which the voltage reference of the feedback loop allows the summing of both the DACOUT voltage and the core voltage for programming the output resistance of the core voltage regulator. This is also the pin at which an optimized transient response can be tailored using Analog Devices' patented ADOPT design technique.
27	CS+	Current Limit Positive Sense. This is a high-impedance analog input pin that is multiplexed between either of the two current-sense inputs during the high state of the OUT pin of the respective channel. During the common off-time of both channels the pin's voltage reflects the average of the two channels. The multiplexed current sense signal is passed to the core comparator through an external resistive termination connected from this pin to the RAMP pin. The external (RAMP) resistor sets the magnitude of the hysteresis applied to the regulation loop.
28	CS-	Current Limit Negative Sense. This is a high-impedance analog input pin which is normally Kelvin connected via a current-limit programming resistor to the negative node of the current sense resistor(s). A hysteretically-controlled current - three times the current programmed at the HYSSET pin - also flows out of this pin and develops a current-limit-setting voltage across that resistor which then must be matched by the inductor current flowing in the current sensing resistor in order to trigger the current limit function. When triggered, the current flowing out of this pin is reduced to two-thirds of its previous value, producing hysteresis in the current limiting function.

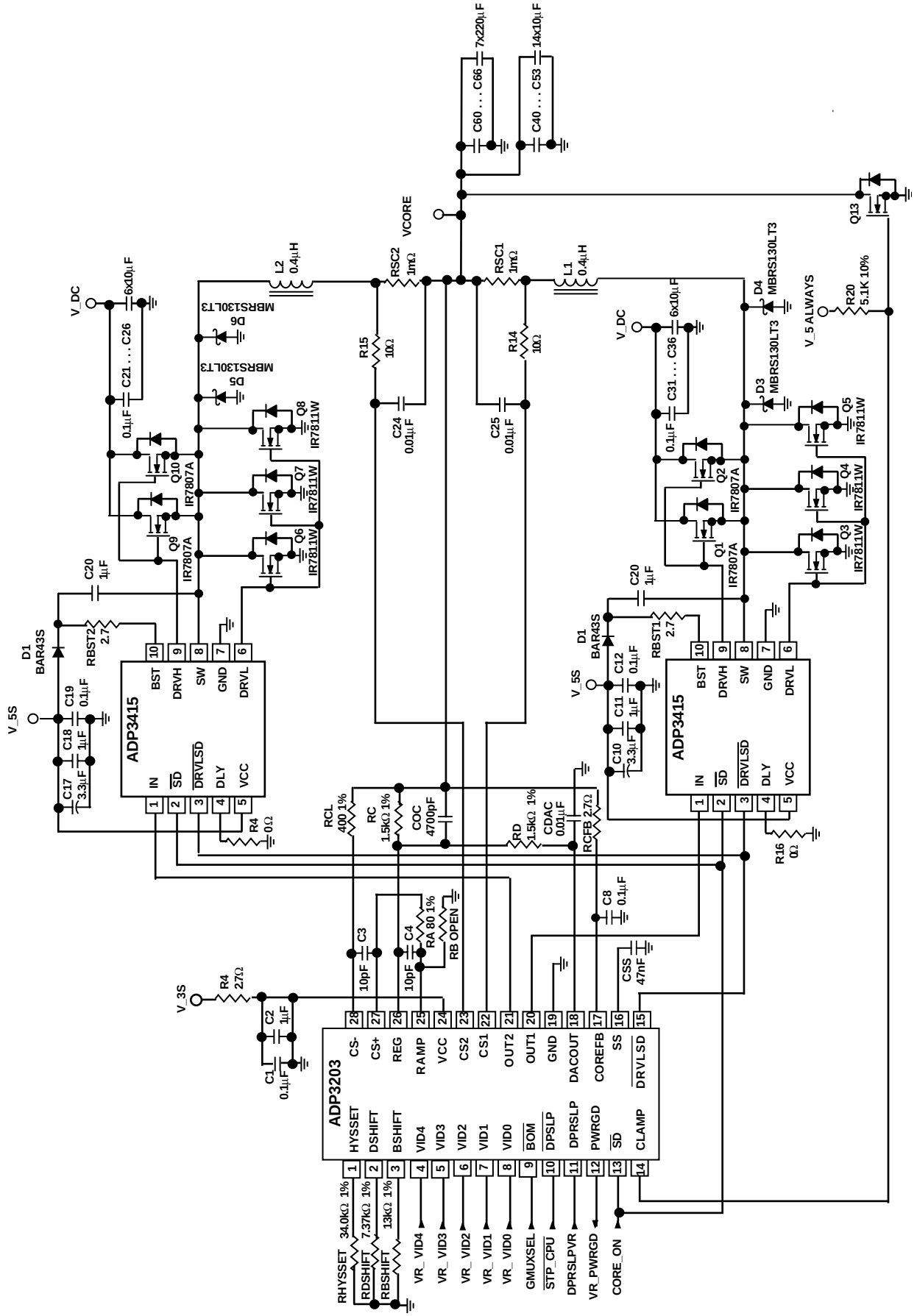

Figure 1. Typical Application

THEORY OF OPERATION

Overview

Featuring a new proprietary single-or-dual-channel buck converter hysteretic control architecture developed by Analog Devices, Inc., the ADP3203 is the optimal core voltage control solution for both IMVP-II & -III generation microprocessors. The complex multi-tiered regulation requirements of either IMVP specification are easily implemented with the highly integrated functionality of this controller.

Power Conversion Control Architecture

Driving of the individual channels is accomplished using external drivers, such as the ADP3415. One PWM interface pin per channel, OUT1 and OUT2, is provided. A separate pin, $\overline{\text{DRVLSD}}$, commands the driver to enable or disable synchronous operation during the off time of each channel. The same $\overline{\text{DRVLSD}}$ pin is connected to both drivers.

The ADP3203 utilizes hysteretic control. The resistor from the HYSSET pin to ground sets up a current that is switched bi-directionally into a resistor interconnected between RAMP and CS+ pins. The switching of this current sets the hysteresis.

In its dual-channel configuration, the hysteretic control requires multiplexing information in the two channels. The inductor current of the channel that is driven high is controlled against the upper hysteresis limit. During the common off-time of the two channels, the inductor currents are averaged together and compared against the lower hysteresis limit. This proprietary off-time averaging technique serves to eliminate a systematic offset that otherwise appears in a fully multiplexed hysteretic control system.

Compensation

As with all ADI products for core voltage control, the controller is compatible with ADOPT™ compensation, which provides the optimum output voltage containment within a specified voltage window or along a specified load-line using the fewest possible number of output capacitors. The inductor ripple current is kept at a fixed programmable value while the output voltage is regulated with fully programmable voltage positioning parameters, which can be tuned to optimize the design for any particular CPU regulation specifications. By controlling the ripple current rather than ripple voltage, the frequency variations associated with changes in output impedance for standard ripple regulators will not appear.

Feedback/Current Sensing

Accurate current sensing is needed to accomplish output voltage positioning accurately, which, in turn, is required to allow the minimum number of output capacitors to be used to contain transients. A current sense resistor is used between each inductor and the output capacitors. To allow the control to operate without amplifiers, the negative feedback signal is multiplexed from the inductor, or upstream, side of the current sense resistors, and a positive feedback signal, if needed for load-line tuning is taken from the output, or downstream, side.

Output Voltage Programming by VID, Offsets, & Load-Line

In the IMVP-II & -III specifications, the output voltage is a function of both the core current – according to a specified load line – and the system operating mode – i.e., performance or battery optimized, normal or deepsleep clocking state, or deepersleep. The VID code programs the "nominal" core voltage. The core voltage decreases as a function of load current along the load line (which is synonymous with an output resistance of the power converter). The core voltage is also offset by a DC value – usually specified as a percentage – depending on the operating mode. The voltage offset is also called a "shift".

Two pins, BSHIFT and DSHIFT, are used to program the magnitude of the voltage shifts. The voltage shifts are accomplished by injecting current at the node of the negative input pin of the feedback comparator. Resistive termination at the pins determines the magnitude of the voltage shifts.

Two other pins, $\overline{\text{BOM}}$ and $\overline{\text{DSLP}}$, are used to activate the respective two shifts only in their active low states. In the ADP3203, the shifts are mutually exclusive, with the DeepSleep shift (controlled by $\overline{\text{DSLP}}$ and DSHIFT pins) being the dominant one. Another pin, DPRSLP, eliminates both shifts only in its active high state. Its assertion corresponds to the DeeperSleep operating mode.

Current Limiting

The current programmed at the HYSSET pin and a resistor from the CS- pin to the common node of the current sense resistors sets the current limit. If the current limit threshold is triggered, a hysteresis is applied to the threshold so that hysteretic control is maintained during a current limited operating mode.

Softstart and Hiccup

A capacitor from the SS pin to determines both the soft-start time and the frequency at which hiccup will occur under a continuous short circuit or overload.

System Signal Interface

Several pins of the ADP3203 are meant to connect directly to system signals. The VID pins connect to the system VID control signals. The DPRSLP pin connects to the system's DPRSLPVR signal. The $\overline{\text{DSLP}}$ pin connects to the system's $\overline{\text{DPSLP}}$ or $\overline{\text{STPCPU}}$ signal. The $\overline{\text{BOM}}$ signal connects to the system's GMUXSEL signal. In an IMVP-II system, the GMUXSEL signal preceeds any VID code change with a few nanoseconds, while in an IMVP-III system, it follows it with a maximum 12 µs delay. To comply with both specifications, the ADP3203 has a VID register in front of the DAC inputs that is written by a short pulse generated at the rising or falling edge of the GMUSEL signal. In an IMVP-II configuration, if the external VID multiplex settling time is longer than the internal VID register's write pulse-width, then the insertion of an external RC delay network in the GMUXSEL signal path (in front of the $\overline{\text{BOM}}$ pin) is recommended. The Intel spec calls for maximum 200 ns VID code set-up time. This specification can be met with a simple RC network which consists of only a 220 kΩ resistor, and no external capacitor just the $\overline{\text{BOM}}$ pin's capacitance.

Undervoltage Lockout

The ADP3203's supply pin, $V_{CC,}$ has undervoltage lockout (UVLO) functionality to ensure that if V_{CC} is too low to maintain proper operation, the IC will remain off and in a low current state.

Over-Voltage Protection (OVP) & Reverse-Voltage Protection (RVP)

The ADP3203 features a comprehensive redundantly monitored OVP and RVP implementation to protect the CPU core against an excessive or reverse voltage, e.g., as might be induced by a component or connection failure in the control or power stage. Two pins are associated with the OVP/RVP circuitry – a pin for output voltage feedback, COREFB, which is used also for power good monitoring but not for voltage regulation, and an output pin, CLAMP.

The CLAMP pin defaults to a low state at startup of the ADP3203 and remains low until an OV or RV condition is detected. If either condition is detected, the CLAMP pin is switched and latched to the VCC pin. The high state of the CLAMP pin is reset only after several milliseconds as the softstart pin discharges.

For maximum and fastest protection, the CLAMP pin should be used to drive the gate of a power MOSFET whose drain-source is connected across the CPU core voltage. Detection of OV or RV will clamp the core voltage to essentially zero, thus quickly removing the fault condition and preventing further energy from being applied to the CPU core.

For a less comprehensively protective but also less costly solution, the CLAMP pin may be used to latch the disconnection of input power. The latch should be powered whenever any input power source is present. Typically, such a latching circuit is already present in a system design, so it becomes only a matter of allowing the CLAMP pin to also trigger the latch. In this configuration, the latched off state of the system would be indicative of a system failure. The OV/RV protective means is via not allowing the continued application of energy to the CPU core. The design objective should be to ensure that the CPU core could safely absorb the remaining energy in the power converter, however, since this energy is not clamped as in the preferred configuration.

LAYOUT CONSIDERATIONS

Advantages in PCB Layout

Analog Devices Inc., provides ADP3203/3415 as a dedicated 2-phase power management solution for IMVP-3 Intel P4 mobile core supply.

This 2-phase solution separates the controller (ADP3203) and MOSFET driver (ADP3415). Today, most motherboards only leave small pieces of PCB area for power management circuit. Therefore, the separation of the controller and the MOSFET drivers gives much greater freedom in layout than any single chip solution can do.

Meanwhile, the separation also provides the freedom to place the analog controller in a relatively quiet area in the motherboard. This can minimize the susceptibility of the controller to injected noise. Any single chip solution with a high speed loop design will suffer larger susceptibility to jitter that appears as modulation of the output voltage.

The ADP3203 maximizes the integration of IMVP-3 features. Therefore, no additional externally implemented functions are required to comply with IMVP-3 specifications. This saves PCB area for component placement on the motherboard.

PCB Layout Consideration for ADP3203/3415

The following guidelines are recommended for optimal performance of the ADP3203 and ADP3415 in a power converter. The circuitry is considered in three parts: the power switching circuitry, the output filter, and the control circuitry.

Placement Overview

1. For ideal component placement, the output filter capacitors will divide the power switching circuitry from the control section. As an approximate guideline, considered on a single-sided PCB, the best layout would have components aligned in the following order: ADP3415, MOSFETs and input capacitor, output inductor, current sense resistor, output capacitors, control components and ADP3203. Note that the ADP3203 and ADP3415 are completely separated for an ideal layout, which is impossible with a single-chip solution. This keeps the noisy switched power section isolated from the precision control section and gives more freedom in the layout of the power switching circuitry.
2. Whenever a power-dissipating component (e.g., a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad if possible and immediately surrounding it, is recommended. Two important reasons for this are: improvement of the current rating through the vias (if it is a current path), and improved thermal performance- especially if there is opportunity to spread the heat with a plane on the opposite side of the PCB.

Power Switching Circuitry

ADP3415, MOSFETs, and Input Capacitors

3. Locate the ADP3415 near the MOSFETs so the loop inductance in the path of the top gate drive returned to the SW pin is small, and similarly for the bottom gate drive whose return path is the ground plane. The GND pin should have at least one very close via into the ground plane.
4. Locate the input bypass MLC capacitors close to the MOSFETs so that the physical area of the loop enclosed in the electrical path through the bypass capacitor and around through the top and bottom MOSFETs (drain-source) is small and wide. This is the switching power path loop.
5. Make provisions for thermal management of all the MOSFETs. Heavy copper and wide traces to ground and power planes will help to pull the heat out. Heatsinking by a metal tap soldered in the power plane

near the MOSFETs will help. Even just small airflow can help tremendously. Paralleled MOSFETs to achieve a given resistance will help spread the heat.

6. An external "antiparallel" schottky diode (across the bottom MOSFET) may help efficiency a small amount (< ~1 %) depending on its forward voltage drop compared to the MOSFET's body diode at a given current; a MOSFET with a built in antiparallel schottky is more effective. For an external schottky, it should be placed next to the bottom MOSFET or it may not be effective at all.
7. The VCC bypass capacitor should be close to the VCC pin and connected on either a very short trace to the GND pin or to the GND plane.

Output Filter

Output Inductor and Capacitors, Current Sense Resistor

8. Locate the current sense resistors very near to the output voltage plane.
9. The load-side heads of two sense resistors should join as closely as possible for accurate current signal measurement of each phase.
10. PCB trace resistances from the current sense resistors to the regulation point should be minimized, known (calculated or measured), and compensated for as part of the design if it is significant. (Remote sensing is not sufficient for relieving this requirement!) A square section of 1-ounce copper trace has a resistance of ~500 mΩ and this adds to the specified DC output resistance of the power converter. The output capacitors should similarly be close to the regulation point and well tied into power planes as impedance here will add to the "AC output resistance" (i.e., the ESR) that is implicitly specified as well.
11. Whenever high currents must be routed between PCB layers, vias should be used liberally to create parallel current paths so that the resistance and inductance is minimized and the via current rating is not exceeded.

Control Circuitry

ADP3203, Control Components

12. If the ADP3203 cannot be placed as previously recommended, at the least care should be taken to keep the device and surrounding components away from radiation sources (e.g., from power inductors) and capacitive coupling from noisy power nodes.
13. Noise immunity can be improved by the use of a devoted signal ground plane for the power controller and its surrounding components. Space for a ground plane might readily be available on a signal plane of the PCB since it is often unused in the vicinity of the power controller.
14. If critical signal lines (i.e., signals from the current sense resistor leading back to the ADP3203) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals.
15. Absolutely avoid crossing any signal lines over the switching power path loop, described previously.
16. Accurate voltage positioning depends on accurate current sensing, so the control signals which monitor the voltage differentially across the current sense resistor should be kelvin connected. Please refer to ADI Evaluation Board of the ADP3203 and its documentation for control signal connection with sense resistors.
17. The RC filter used for the current sense signal should be located near the control components as this serves the dual purpose of filtering out the effect of the current sense resistors' parasitic inductance and noise picked up along the routing of the signal. The former purpose is achieved by having the time constant of the RC filters approximately matched to that of the sense resistors and is important for maintaining the accuracy of the current signal.

TABLE 1. VID CODE

VID4	VID3	VID2	VID1	VID0	VOUT
0	0	0	0	0	1.750
0	0	0	0	1	1.700
0	0	0	1	0	1.650
0	0	0	1	1	1.600
0	0	1	0	0	1.550
0	0	1	0	1	1.500
0	0	1	1	0	1.450
0	0	1	1	1	1.400
0	1	0	0	0	1.350
0	1	0	0	1	1.300
0	1	0	1	0	1.250
0	1	0	1	1	1.200
0	1	1	0	0	1.150
0	1	1	0	1	1.100
0	1	1	1	0	1.050
0	1	1	1	1	1.00
1	0	0	0	0	0.975
1	0	0	0	1	0.950
1	0	0	1	0	0.925
1	0	0	1	1	0.900
1	0	1	0	0	0.875
1	0	1	0	1	0.850
1	0	1	1	0	0.825
1	0	1	1	1	0.800
1	1	0	0	0	0.775
1	1	0	0	1	0.750
1	1	0	1	0	0.725
1	1	0	1	1	0.700
1	1	1	0	0	0.675
1	1	1	0	1	0.650
1	1	1	1	0	0.625
1	1	1	1	1	0.600

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Thin Shrink Small Outline Package (TSSOP)
(RU-28)