Super Sync Separator

The EL4511 sync separator IC is designed for operation in the next generation of DTV, HDTV, and projector applications, as well as broadcast equipment and other applications where video signals need to be processed.

The EL4511 accepts sync on green, separate sync, and H/V sync inputs, automatically selecting the relevant format. It is also capable of detecting and decoding tri-level syncs used with the latest HD systems. Unlike standard sync separators, the EL4511 can automatically detect the line rate and locks to it, without the use of an external R_{SET} resistor.

The EL4511 is available in a 24-pin QSOP package and operates over the full 0°C to 70°C temperature range.

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL4511CU	24-Pin QSOP	-	MDP0040
EL4511CU-T7	24-Pin QSOP	7”	MDP0040
EL4511CU-T13	24-Pin QSOP	13”	MDP0040

Features

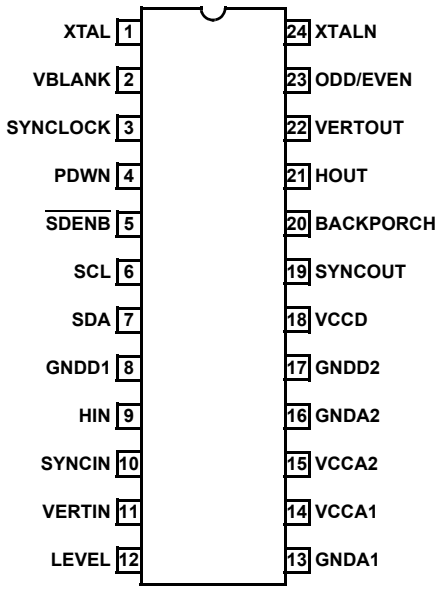
- Composite, component, HDTV, and PC signal-compatible
- Tri-level & bi-level sync-compatible
- Auto sync detection
- 150kHz max line rate
- Low power
- Small package outline
- 3.3V and 5V operation

Applications

- HDTV/DTV analog inputs
- Video projectors
- Computer monitors
- Set top boxes
- Security video
- Broadcast video equipment

Pinout

EL4511
(24-PIN QSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage . . . . . (V_S to GND) +6V
Pin Voltage. . . . . GND - 0.3V, V_S +0.3V
V_{CCA1}, V_{CCA2} & V_{CCD} . . . . . .Must Be Same Voltage

Storage Temperature Range . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . 125°C
Ambient Operating Temperature . . . . . 0°C to +70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

$V_S = V_{CCA1} = V_{CCA2} = V_{CCD}$ = +5V, T_A = 25°C, NTSC input signal on SYNCIN, no output loads, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
ISD	Digital Supply Current	(Note 1)		15	20	mA
		Standby PDWN = V_{CCD} (Note 2)		4	20	µA
ISA2	Rate Acquisition Oscillator Supply Current	(Note 1)		3	20	mA
		Standby PDWN = V_{CCD}		2.5	20	µA
ISA1	Analog Processing Supply Current	(Note 1)		3	20	mA
		Standby PDWN = V_{CCD} (Note 2)		3	20	µA
COMPOSITE SYNC INPUT AT SYNCIN						
V_{SYNC}	Sync Signal Amplitude	AC coupled to SYNCIN pin (Notes 1 & 3)	140		600	mV
V_{SLICE}	Slicing Level of Sync Signal	After sync lock is attained, see description		50		%
HORIZONTAL AND VERTICAL INPUT AT H_{IN}, VERTIN						
H_{SLICE}, V_{SLICE}	Slice Level of H_{IN} and VERTIN			1.4		V
T_{HINL}	H Sync Width		3		12.8	% of H time
F_{HINH}	H Sync Frequency		10.75		150	kHz
T_{VINL}	V Sync Width		2		7	H lines
F_{VINH}	V Sync Frequency		23		100	Hz
LOGIC OUTPUT SIGNALS, H_{OUT}, V_{OUT}, V_{BLANK}, BACKPORCH, ODD/EVEN, SYNCLOCK						
O/P_{LOW}	Logic Low State	1.6mA, V_{CCD} = 5V			GNDD+0.4	V
		1.6mA, V_{CCD} = 3.3V			GNDD+0.5	
O/P_{HI}	Logic High State	1.6mA, V_{CCD} = 5V	V_{CCD}-0.4			V
		1.6mA, V_{CCD} = 3.3V	V_{CCD}-0.5			
Td_{HOUT}	H_{OUT} Timing Relative to Input	See timing diagrams 1, 2, 3 & 4				
$Td_{SYNCOUT}$	SYNCOUT Timing Relative to Input	See timing diagrams 1, 2, 3 & 4				
$Td_{BACKPORCH}$	BACKPORCH Timing Relative to Input	See timing diagrams 1, 2, 3 & 4				
LEVEL OUTPUT DRIVER, LEVEL						
V_{LEVEL}	2 X Amplitude of V_{SYNC}	Refer to description of operation	1.9x	2.15x	2.4x	
Z_{LEVEL}	O/P Resistance of Driver Stage			450		Ω
REFERENCE OSCILLATOR						
F_{IN}	Reference Input Frequency	Refer to description of operation			50	kHz
F_{XTAL}	Crystal Frequency	Watch crystal (optional)		32.768		kHz

Electrical Specifications $V_S = V_{CCA1} = V_{CCA2} = V_{CCD} = +5V$, $T_A = 25°C$, NTSC input signal on SYNCIN, no output loads, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL INTERFACE SIGNALS PDWN, $\overline{SDENB}$, SCL AND SDA						
V_{HIGH}	Input Logic High Threshold				V_{CCD}-1V	
V_{LOW}	Input Logic Low Threshold		V_{GNDD}+1V			
O/PV_{HI}	SDA O/P Logic High State	@ 1mA	V_{CCD}-0.4			V
O/PV_{LOW}	SDA O/P Logic Low State	@ 1mA			GNDD+0.4	V
F_{SCL}	Serial Control Clock Frequency			5		MHz
T_{CLS}	Setup Time			30		ns
T_{CLH}	Hold Time			30		ns
T_{LC}	Load to Clock Time			30		ns
T_{DC}	Hold to Clock Time			30		ns
T_{CD}	Clock to Data Out Time			30		ns

NOTES:

1. NTSC signal; see curves for other rates
2. XTAL pin must be low, otherwise 70µA
3. I/P range reduces if V_S of 3.3V - 4.5V (see timing diagram 1)

Pin Descriptions

PIN NUMBER	PIN NAME	PIN TYPE	PIN DESCRIPTION
1	XTAL	Input	Crystal input (see Table 5 for details)
2	VBLANK	Logic Output	Vertical blank output
3	SYNCLOCK	Logic Output	Indicates that the EL4511 has locked to the line rate and has found three consecutive “good H lines”
4	PWDN	Logic Input	Power-down = hi
5	$\overline{SDENB}$	Logic Input	Serial interface enable = low
6	SCL	Logic Input	Serial clock
7	SDA	Logic BIDIR	Serial data (input for chip setup, output for diagnostic information)
8	GNDD1	Power	Digital ground 1
9	HIN	Input	Horizontal sync
10	SYNCIN	Input	Video input, which may incorporate sync signal; connect to Y or G
11	VERTIN	Input	Vertical sync input
12	LEVEL	Output	Indicates 2x amplitude of sync tip vs. back porch; referred to ground
13	GNDA1	Power	Analog ground 1
14	VCCA1	Power	Analog power supply 1
15	VCCA2	Power	Analog power supply 2
16	GNDA2	Power	Analog ground 2
17	GNDD2	Power	Digital ground 2
18	VCCD1	Power	Digital power supply 1
19	SYNCOUT	Logic Output	Composite sync output
20	BACKPORCH	Logic Output	Back porch output
21	HOUT	Logic Output	Horizontal sync output
22	VERTOUT	Logic Output	Vertical sync output
23	ODD/EVEN	Logic Output	Odd-Even field indicator output
24	XTALN	Output	Crystal output (see Table 5 for details)

TABLE 1. SERIAL INTERFACE REGISTER BIT ALLOCATIONS

REGISTER NUMBER	REGISTER BIT	SIGNAL NAME	TYPE	RESET VALUE	DESCRIPTION AND COMMENTS
1		**General Control Reg 1**	**R/W**	**00h**	
	7	General Reset		0	Software reset. Does not affect serial interface.
	6	AlwaysEnOutputs		0	Overrides internal qualification of outputs.
	5:3	ModeCtrl		0	Sync acquisition. Selects input signal. See Table 2.
2		**General Control Reg 2**	**R/W**	**10h**	
	5	Select Fixed Slicing (no S/H)		0	Necessary for SECAM. May be useful for VCRs.
	4	FILTER_ENABLED		1	Set Hi to include digital filter on horizontal input.
	1	OE_MODE		0	Set Hi for Odd/Even changes on rising edge of vertical.
3		**V_{BLANK} Control Reg 1**	**R/W**	**90h**	
	7	EnVBlank		1	Enables vertical blank interval detection algorithm.
	6:0	VSTPlusBP		10h	Number of lines after vertical sync time.
4		**V_{BLANK} & Polarity Ctrl**	**R/W**	**4Fh**	
	7:4	VFrontPorch		4h	Number of lines before vertical sync time.
	3	DefaultHPolarity		1	HIN polarity on reset if EnHpolarityDet = Lo.
	2	DefaultVPolarity		1	VERTIN polarity on reset and if EnVpolarityDet = Lo.
	1	EnHPolarityDet		1	Allows EL4511 to detect and set polarity on HIN.
	0	EnVPolarityDet		1	Allows EL4511 to detect and set polarity on VERTIN.
6		**Oscillator Control 2**	**R/W**	**22h**	
	7:6	CMuxCtrl <1:0>		0	Multiplexes clock onto V_{BLANK} or Odd/Even. See Table 3.
7		**V_{BLANK} O/P Reg 1**	**R**		Only valid if V_{BLANK} circuit is enabled
	7:0	LinesPerFrame <7:0>		-	Least significant byte of lines per frame count.
8		**V_{BLANK} O/P Reg 2 & Misc**	**R**	**80h**	
	7:4	LinesPerFrame <11:8>		-	Most significant 4 bits of lines per frame count.
	3	En50Slice		-	Indicates sample and hold front end is being used.
	2	LPFValid		-	Indicates lines per frame has been updated.
	1	progressive		-	Not valid for certain types of composite sync.
	0	tri-level detect		-	Only valid if tri-level sync detected.
9		**Analog Control Reg 1**	**R/W**		
	6	ENXTAL		0	Set Hi to enable crystal oscillator.
	5	ENLEVELBLANKING		0	Set Hi to enable V_{LEVEL} when not locked.
	4	$\overline{\text{ENLEVEL}}$		0	Set Hi to disable V_{LEVEL} output.
	3	$\overline{\text{ENSYCLAMP}}$		0	Set Hi to disable “soft” sync tip clamping in SYNCIN.
	2	$\overline{\text{ENALOS}}$		0	Set Hi to disable analog loss of signal feature.
	1	$\overline{\text{ENRVIDEO}}$		0	Set Hi to disable internal biasing on SYNCIN (passive resistor or soft clamp.)
	0	PWRSAVE		0	Set Hi to put the analog circuit into powersave mode.
13		**Absolute Timing Ref 1**	**R**		
	7:0	CountsPerField <7:0>		-	Crystal clock periods per field: L.S. Byte. (see description)
14		**Absolute Timing Ref 2 & Misc**	**R**		

TABLE 1. SERIAL INTERFACE REGISTER BIT ALLOCATIONS (Continued)

REGISTER NUMBER	REGISTER BIT	SIGNAL NAME	TYPE	RESET VALUE	DESCRIPTION AND COMMENTS
	7:6	CountsPerField <9:8>		-	Crystal clock periods per field: Bits 9:8. (see description)
	5	SyncLock			As sync lock pin.
	4	CPFValid		-	Counts per field valid. Set L if read occurs during an update.
	3	SetBiLevel		-	Lo: Tri-level mode; Hi: Bi-level mode.
	2	VinSyncDet		-	Indicates vertical sync on VERTIN successfully acquired.
	1	VinPolarity		-	VERTIN polarity setting: Observe.
	0	HPolarity		-	HIN polarity setting: Observe.
16		**Oscillator Settings Observe 2**	**R**		
	4	RateLocked		-	Indicates line rate successfully acquired.
	3	ALOS		-	Analog loss of signal, measured via S/H. H indicates analog signal amplitude is below threshold.

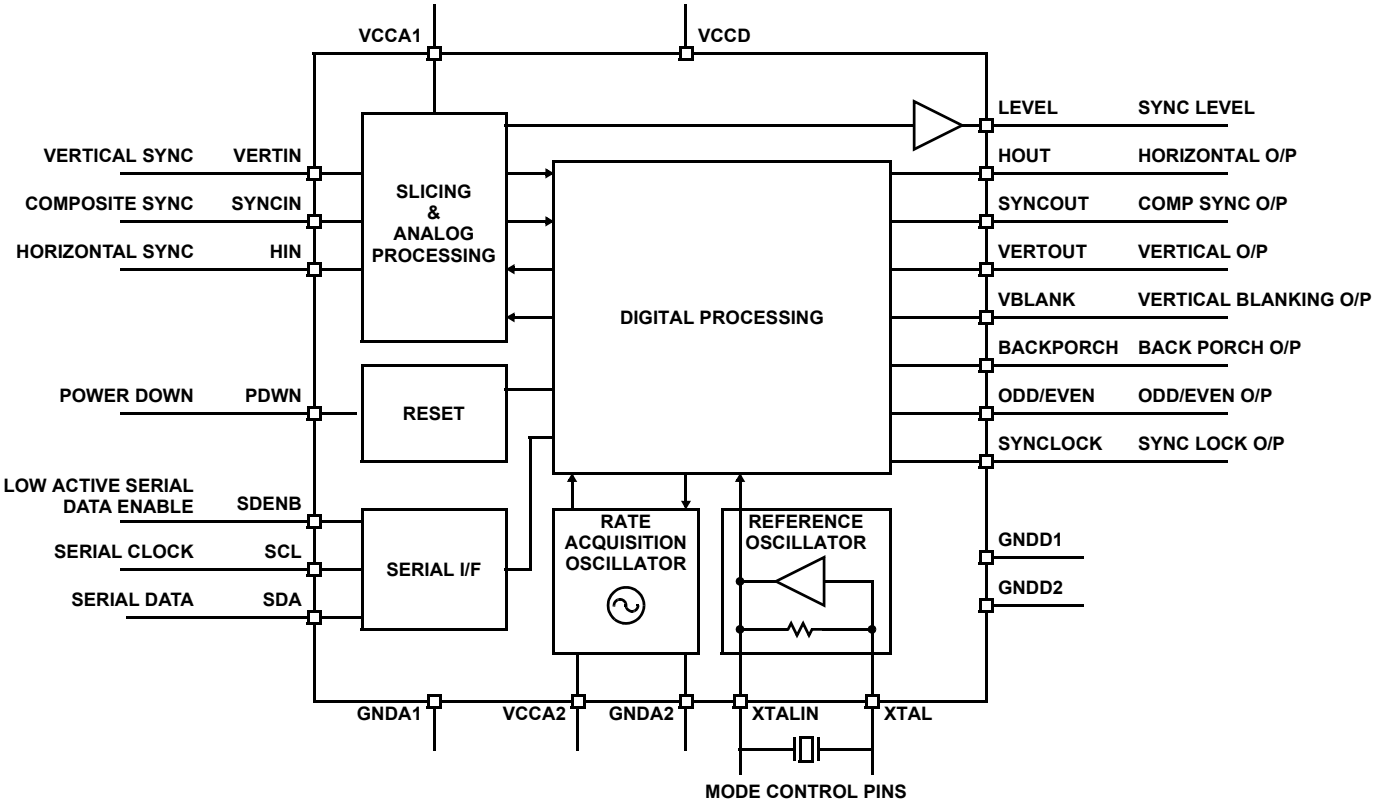
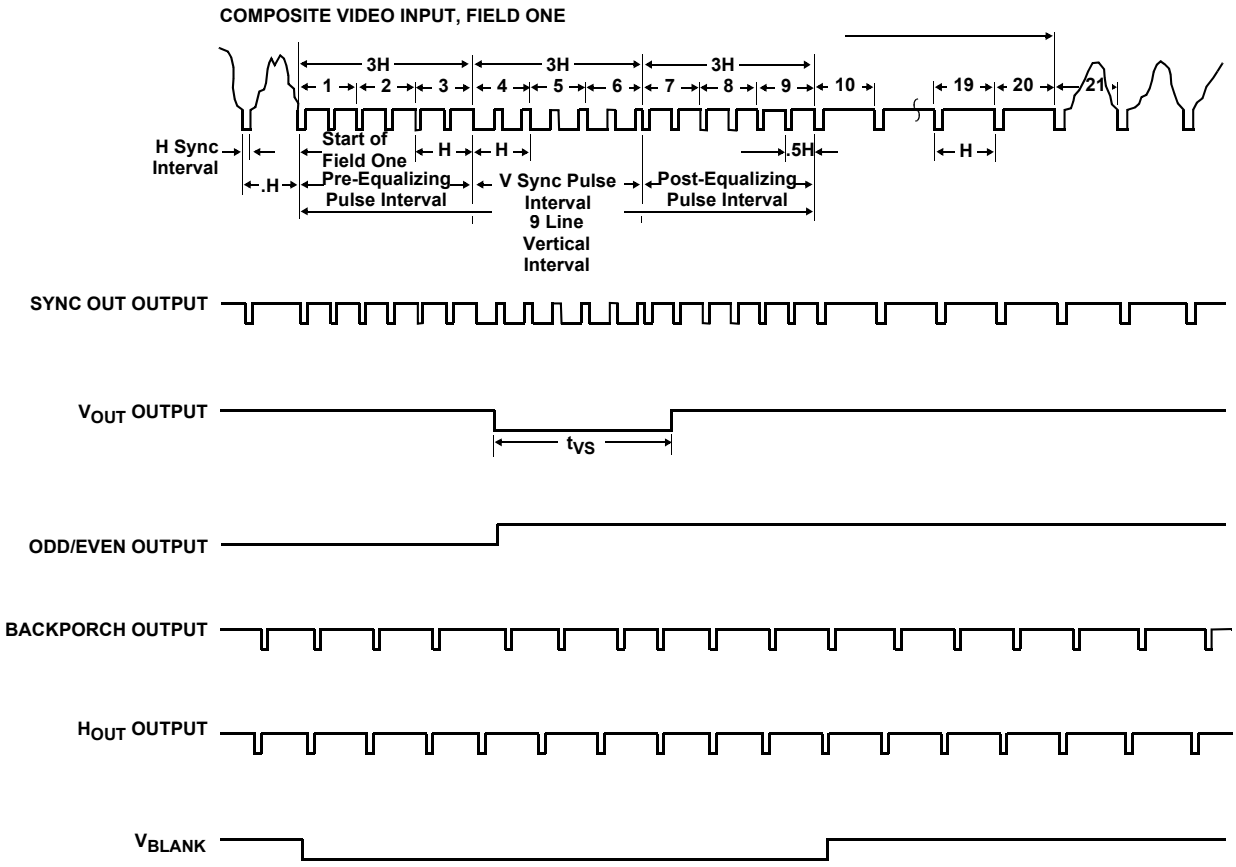


FIGURE 1. BLOCK DIAGRAM



Notes:

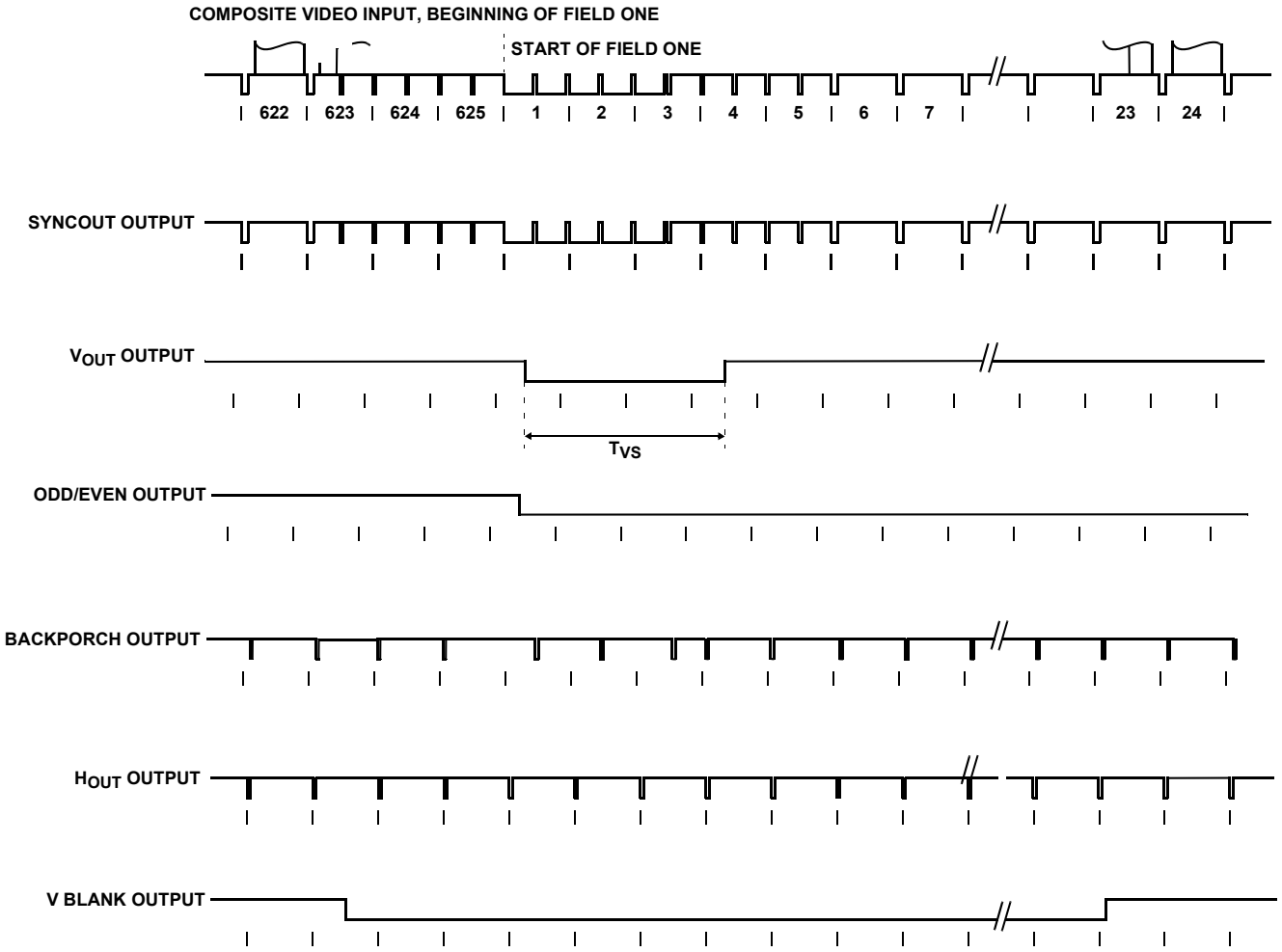
b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

FIGURE 2. EXAMPLE OF VERTICAL INTERVAL (525)



Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

FIGURE 3. EXAMPLE OF VERTICAL INTERVAL (625)

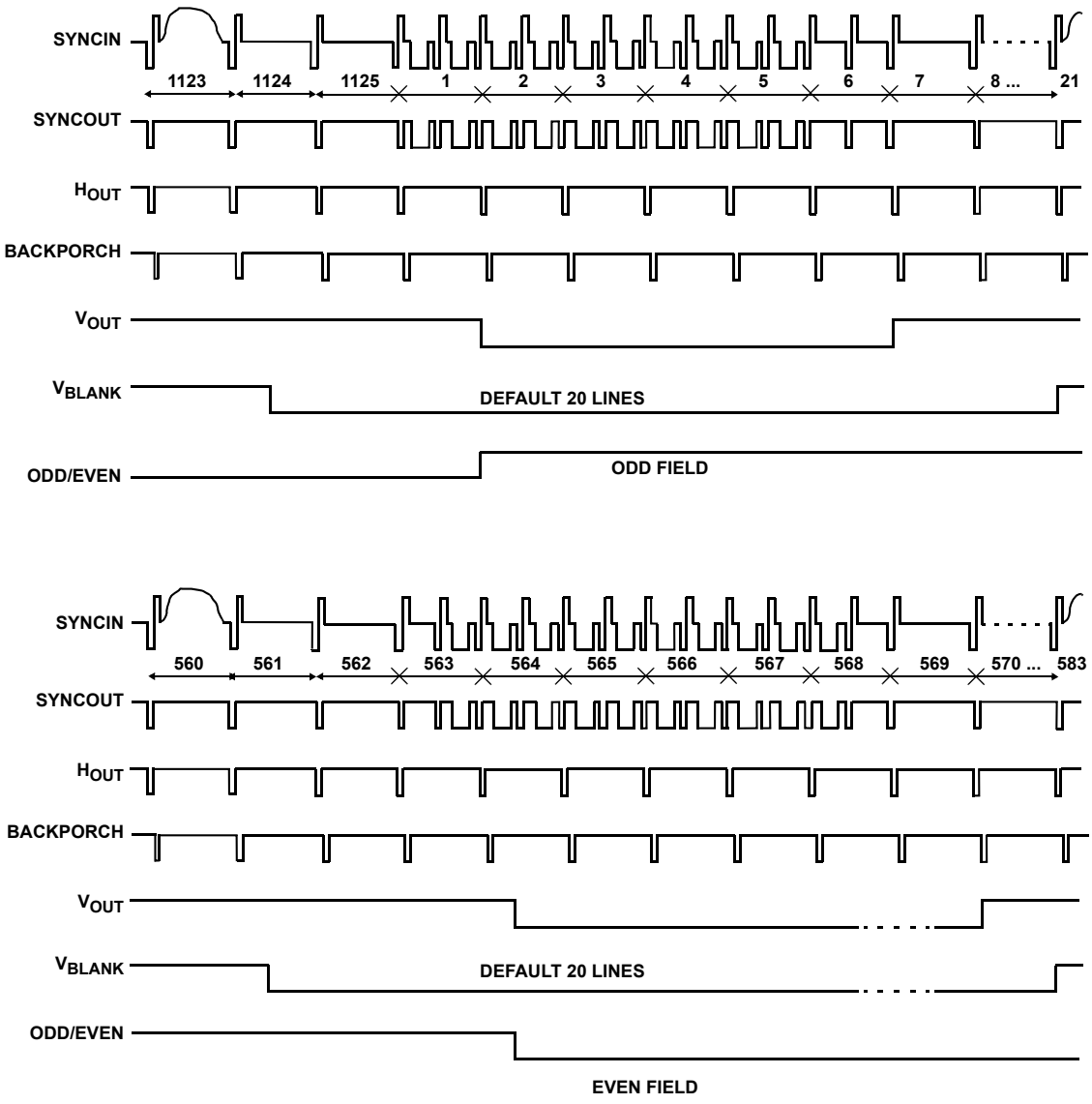


FIGURE 4. EXAMPLE OF HDTV 1080I/30 LINE COMPOSITE VIDEO: INTERLACED, ODD & EVEN FIELD

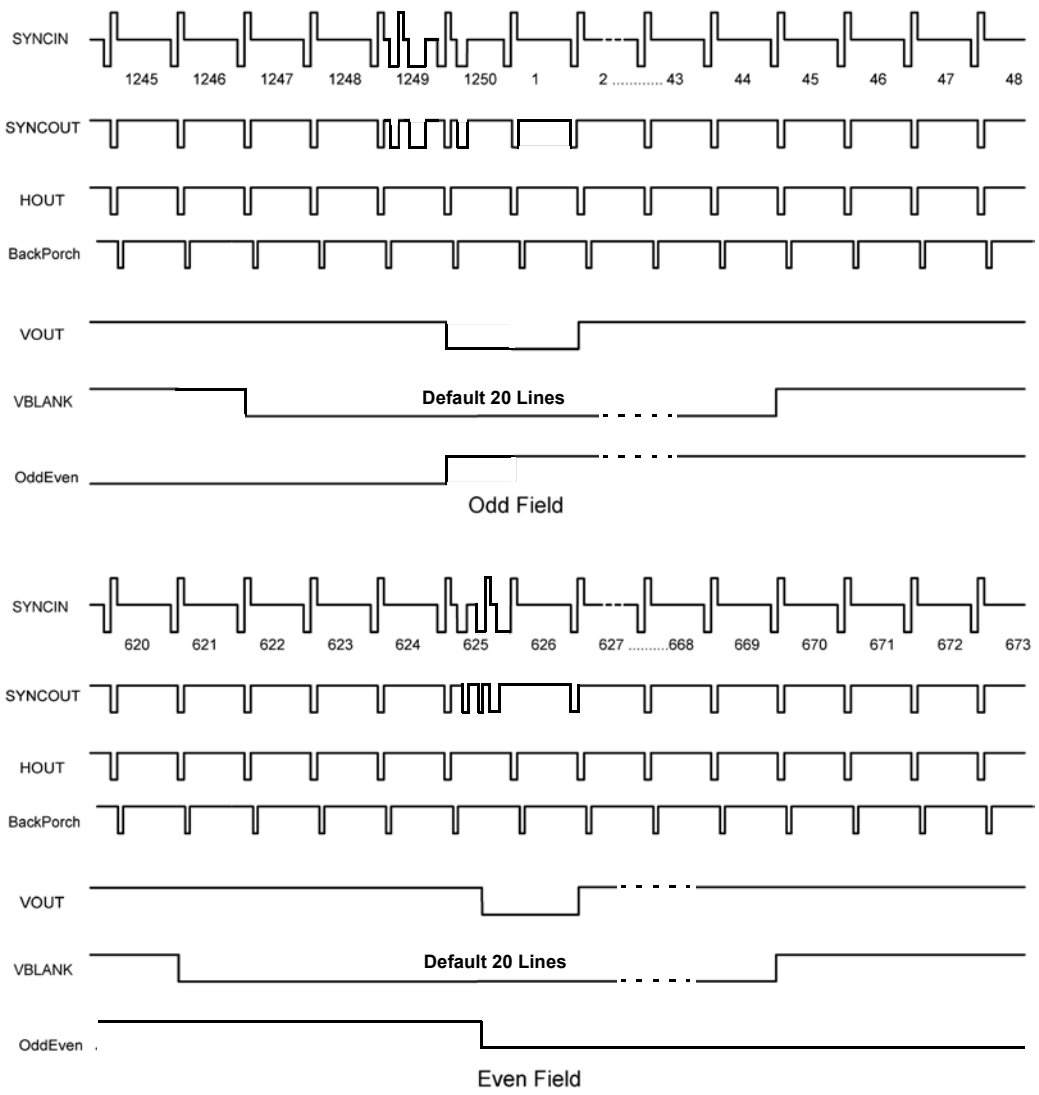
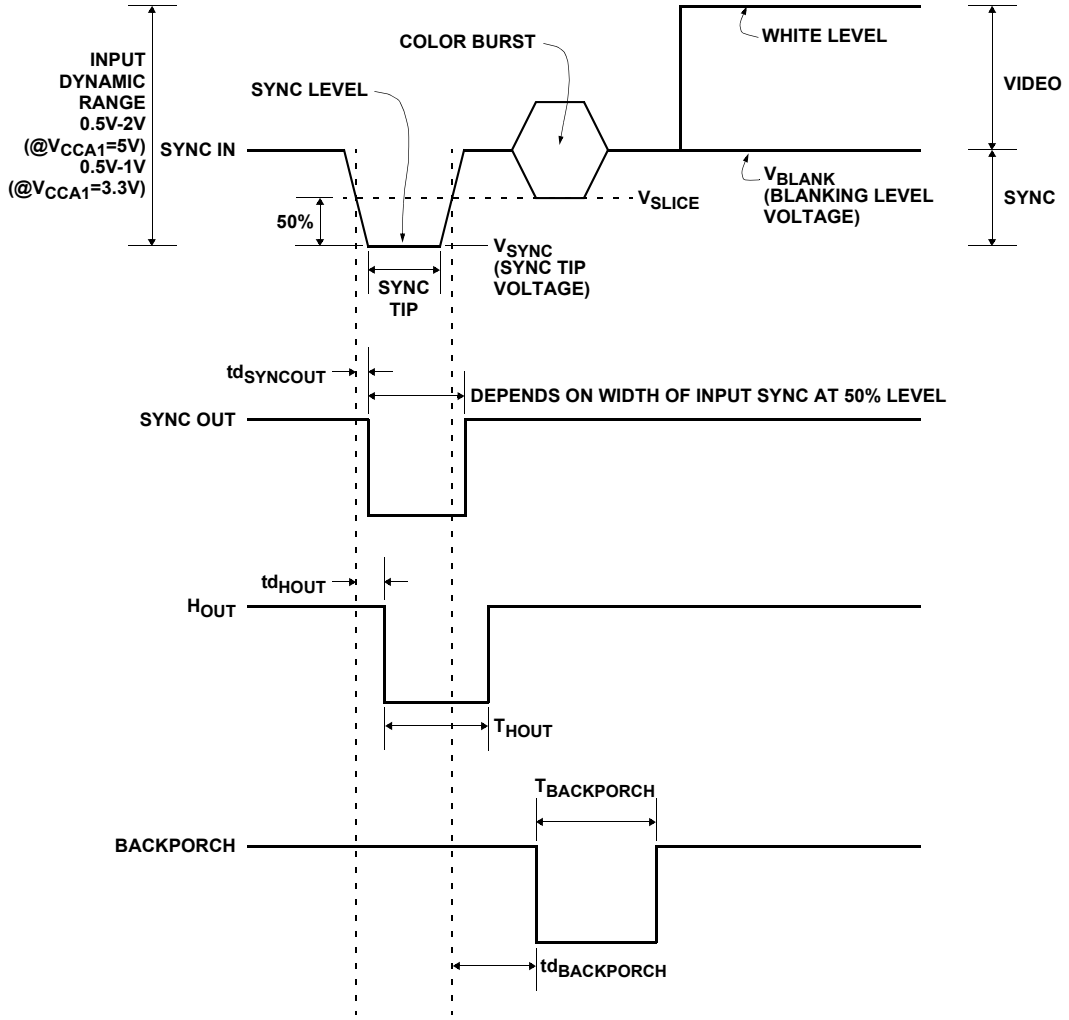


FIGURE 5. HDTV 1080I/25 LINE COMPOSITE VIDEO: INTERLACED ODD & EVEN FIELD (1250 LINES)

Timing Diagram 1 - Example of Horizontal Interval 525/625 Line Composite

CONDITIONS: $V_{CCA1} = V_{CCA2} = V_{CCD} = +5V$, $T_A = 25°C$, NO FILTER (REGISTER 2 BIT 4=0)



No Filter

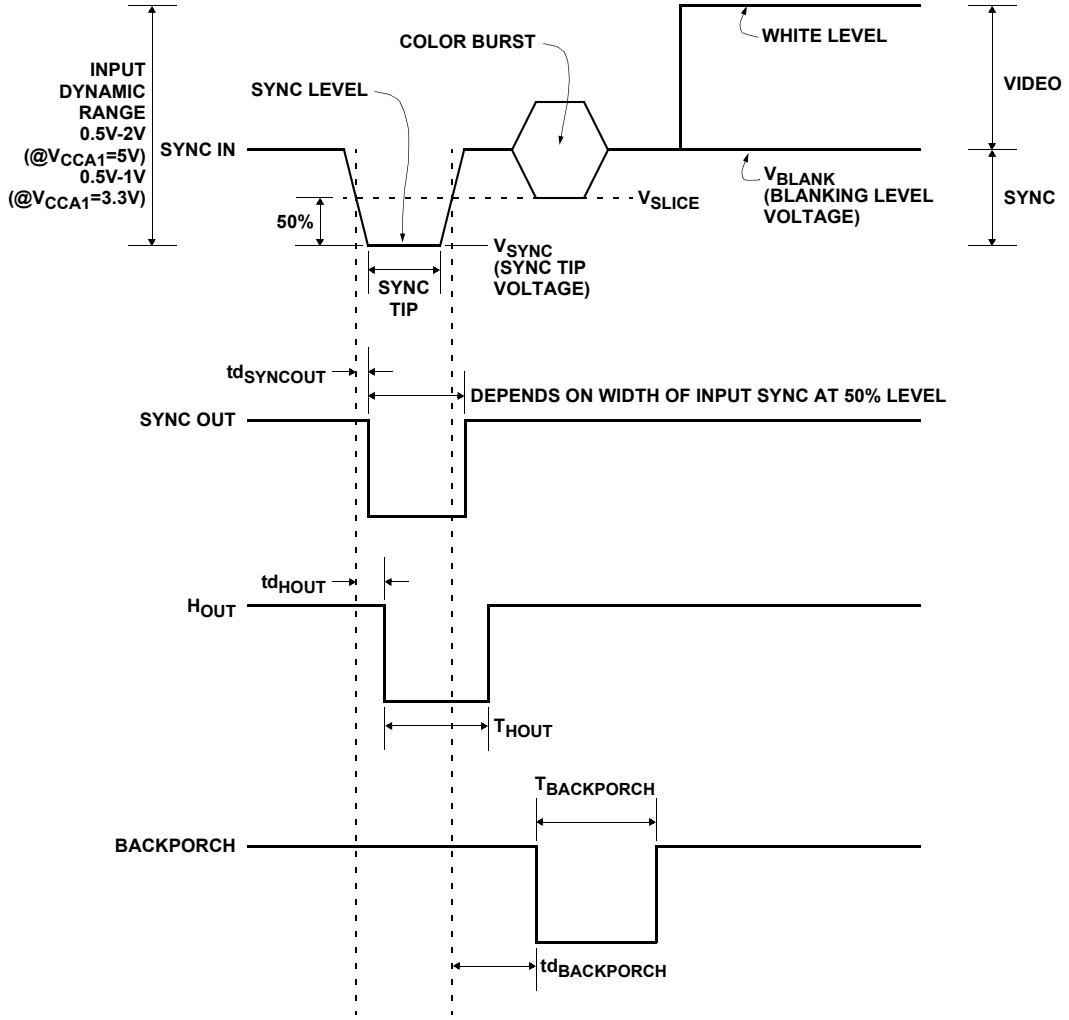
PARAMETER	DESCRIPTION	CONDITIONS	TYP (Note 1)	UNIT
$td_{SYNCOUT}$	SYNCOUT Timing Relative to Input	See timing diagram 1	65	ns
td_{HOUT}	HOUT Timing Relative to Input	See timing diagram 1	470	ns
$td_{BACKPORCH}$	BACKPORCH Timing Relative to Input	See timing diagram 1	525	ns
T_{HOUT}	Horizontal Output Width	See timing diagram 1	1545	ns
$T_{BACKPORCH}$	BACKPORCH (Clamp) Width	See timing diagram 1	3345	ns

NOTE:

1. Delay variation is less than 2.5ns over temperature range

Timing Diagram 2 - Example of Horizontal Interval 525/625 Line Composite

CONDITIONS: $V_{CCA1} = VC_{CA2} = V_{CCD} = +5V$, $T_A = 25°C$, FILTER IN (REGISTER 2 BIT 4=1)



Filter In

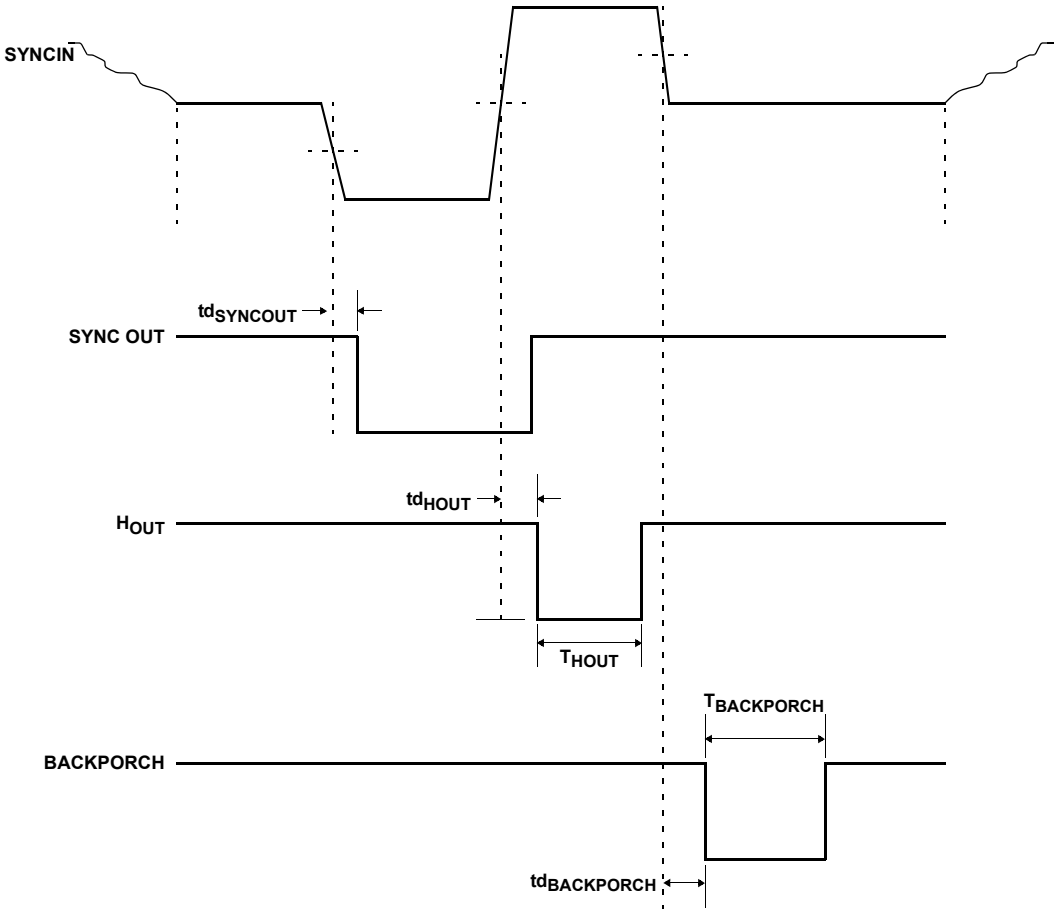
PARAMETER	DESCRIPTION	CONDITIONS	TYP (Note 1)	UNIT
$td_{SYNCOUT}$	SYNCOUT Timing Relative to Input	See timing diagram 2	220	ns
td_{HOUT}	HOUT Timing Relative to Input	See timing diagram 2	470	ns
$td_{BACKPORCH}$	BACKPORCH Timing Relative to Input	See timing diagram 2	525	ns
T_{HOUT}	Horizontal Output Width	See timing diagram 2	1545	ns
$T_{BACKPORCH}$	BACKPORCH (Clamp) Width	See timing diagram 2	3345	ns

NOTE:

1. Delay variation is less than 2.5ns over temperature range

Timing Diagram 3 - Example of Horizontal Interval (HDTV) (720p)

CONDITIONS: $V_{CCA1} = V_{CCA2} = V_{CCD} = +3.3V/+5V$, $T_A = 25°C$, NO FILTER (REGISTER 2 BIT 4=0)



H Timing for HDTV, No Filter (using 720p input signal)

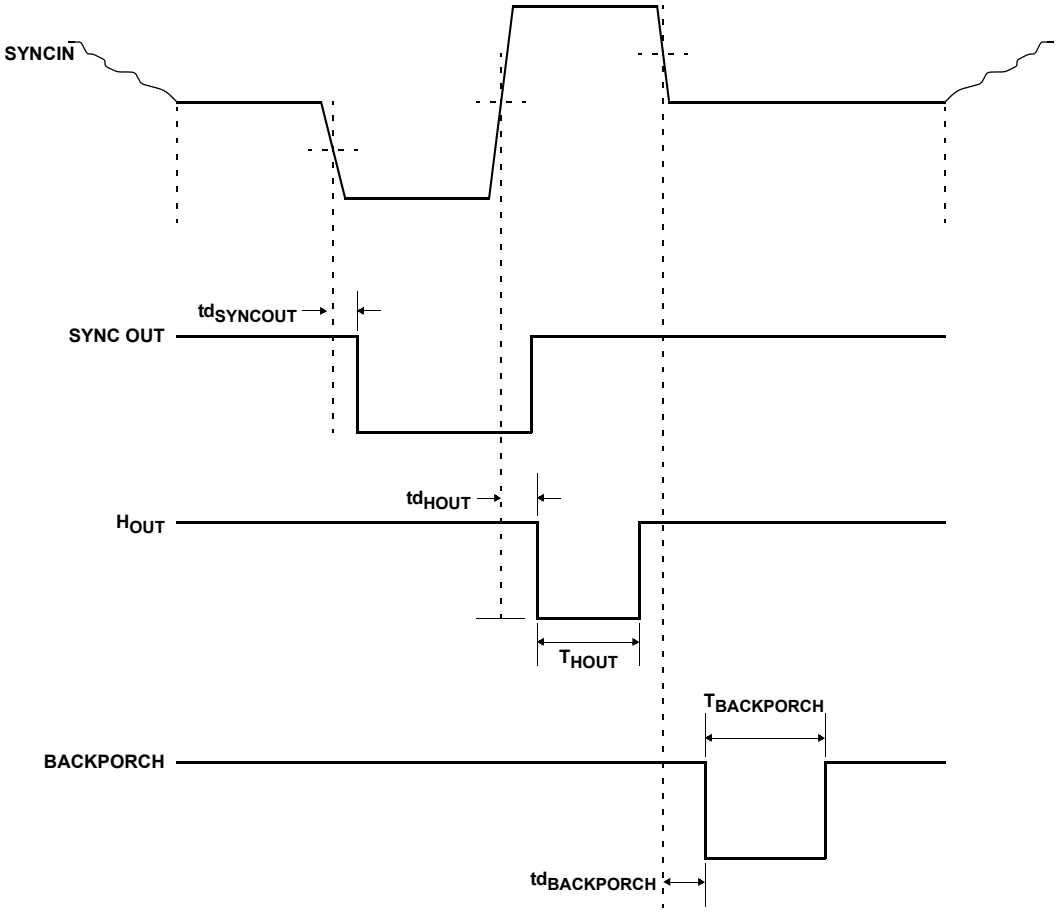
PARAMETER	DESCRIPTION	CONDITIONS	TYP @ 3.3V (Note 1)	TYP @ 5V (Note 1)	UNIT
$td_{SYNCOUT}$	SYNCOUT Timing Relative to Input	See timing diagram 3	56	50	ns
td_{HOUT}	HOUT Timing Relative to Input	See timing diagram 3	48	36	ns
$td_{BACKPORCH}$	BACKPORCH Timing Relative to Input	See timing diagram 3	150	140	ns
T_{HOUT}	Horizontal Output Width	See timing diagram 3	275	275	ns
$T_{BACKPORCH}$	BACKPORCH (Clamp) Width	See timing diagram 3	300	300	ns

NOTE:

1. Delay variation is less than 2.5ns over temperature range

Timing Diagram 4 - Example of Horizontal Interval (HDTV)

CONDITIONS: $V_{CCA1} = V_{CCA2} = V_{CCD} = +3.3V/+5V$, $T_A = 25°C$, FILTER (REGISTER 2 BIT 4=1)



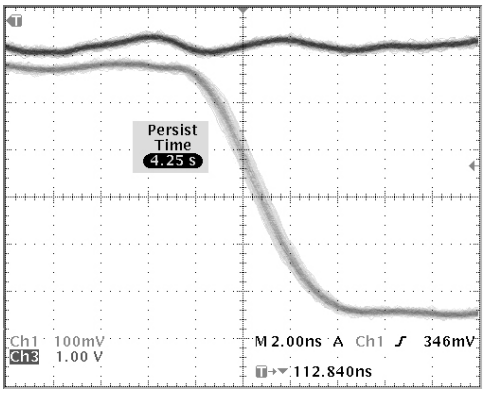
H Timing for HDTV, With Filter (using 720p input)

PARAMETER	DESCRIPTION	CONDITIONS	TYP @ 3.3V (Note 1)	TYP @ 5V (Note 1)	UNIT
$td_{SYNCOUT}$	SYNCOUT Timing Relative to Input	See timing diagram 4	120	110	ns
td_{HOUT}	HOUT Timing Relative to Input	See timing diagram 4	112	100	ns
$td_{BACKPORCH}$	BACKPORCH Timing Relative to Input	See timing diagram 4	155	140	ns
T_{HOUT}	Horizontal Output Width	See timing diagram 4	300	300	ns
$T_{BACKPORCH}$	BACKPORCH (Clamp) Width	See timing diagram 4	300	300	ns

NOTE:

1. Delay variation is less than 2.5ns over temperature range

Timing Diagram 5 - 720p Standard with Filter in Circuit



This waveform shows the output jitter present on the H_{OUT} signal. The oscilloscope is triggered from the positive reference edge of the composite sync output.

Description of Operation

The EL4511 incorporates the following functional blocks:

- Analog I/Ps, processing, and slicing
- Signal source and polarity detector
- Signal & H rate acquisition block
- Advanced sync separator which will detect both conventional and tri-level sync signals
- Video lock and level indicators
- Reference counter
- Computer and control interface

Analog I/Ps, Processing, and Slicing

The EL4511 has three I/P pins which may be connected to a source of external sync signals.

For YPrPb or RGB applications, Y or G should be connected to SYNCIN. For applications with separate horizontal and vertical sync inputs, these should be connected to HIN and VERTIN, respectively. (HIN may also be used for composite sync without video.)

Composite video input signals should be connected to SYNCIN. This should be AC coupled from a low impedance source. The input resistance is in the order of 100kΩ. After H lock is obtained, this signal will be “soft clamped” (5kΩ) to approximately 20% of the V_{CCA1} voltage.

In the default mode, the clamping action ensures that the correct slicing levels will be used throughout the field.

This operation can be modified through Register 9. The soft clamp can be disabled by setting bit 3 to Hi. Setting bit 1 to high will disconnect the input bias network.

Once the acquisition process is complete (see below for description), the slice level will be adaptive. The sync signal is measured from sync tip to blanking level; (Tri-level is measured between negative and positive sync tips). The slice level is then set to 50% of these levels.

It is possible to force the slicing level to remain at the fixed level of 78mV above the sync tip; Register 2, bit 5 is set High to do this. This can help when dealing with signal that have bursts of noise, or formats that have signals that will modify the sync amplitude measurement process.

VGA type of signals will be connected to the HIN and VERTIN pins (use HIN for combined H & V). These are DC coupled signals; they will be sliced at a fixed level of approximately 1.4V. These inputs may be any combination of positive and negative polarities; the EL4511 will invert as required to keep the outputs in the correct polarity. This polarity correction process may be modified with Register 4 bits 3:0.

Signal and Horizontal Rate Acquisition Block

On power-up, if both HIN and SYNCIN are enabled; the

EL4511 will slice the SYNCIN input at 78mV above the negative sync tip level and monitor the sliced signal for up to 320µs. If a periodic signal within the specified frequency limits is found to be present, this is assumed to be the horizontal frequency. If no signal is found, the EL4511 will switch to slice and monitor the HIN input at a TTL level. The EL4511 will continue to monitor these two signals in turn until an appropriate signal is detected.

If only one of HIN and SYNCIN is enabled, the EL4511 will continuously monitor the selected signal until an appropriate signal is detected; this will give a shorter lock time where only one type of signal is used. At this point, the rate acquisition oscillator lock process (to the H rate signal) will begin.

TABLE 2. MODE CONTROL TRUTH TABLE (see also Table 5 for hardware over-ride)

Mode Ctrl	EnTri Level	EnBi Level	EnHin Vin	TriLevel Priority	Hin Priority	HinVin Only
Reg 1 b5 b4 b3						
0 0 0	1	1	1	0	0	0
0 0 1	1	1	1	0	1	0
0 1 0	1	1	1	1	0	0
0 1 1	1	0	0	1	0	0
1 0 0	0	1	1	0	0	0
1 0 1	0	1	0	0	0	0
1 1 0	0	1	1	0	1	0
1 1 1	0	1	1	0	1	1

EnTriLevel, EnBiLevel and EnHinVin; these enable tri-level sync detection, two-level sync detection and separate H/V (VGA) sync detection, respectively.
Other signals used to prioritize tri-level syncs (TriLevPriority), separate H/V (Hin Priority), or to only allow signals from HIN/VERTIN (HinVinOnly).

Horizontal Rate Acquisition Oscillator

This oscillator is frequency locked to 512 times the horizontal rate. This clock signal generates the timing and gating signals that are employed internally by the EL4511. This operation is entirely automatic and requires no input from the external circuitry or microprocessor.

It is possible to gain access to this oscillator O/P by changing the assignment of pin 2 (V_{BLANK}) or pin 23 (ODD/EVEN).

Register 6, bits 7:6 make this selection; see Table 3 for allocations.

The oscillator frequency is adjusted at the beginning of the line. At the time of frequency adjustment the clock O/P may have a phase discontinuity.

TABLE 3. ACQUISITION CLOCK MULTIPLEXER

CmuxCtrl	ACTION
Reg6 b7 b6	
0 0	Normal Operation
0 1	Clock multiplexed onto Odd/Even (pin 23)
1 0	Clock multiplexed onto V_{BLANK} (pin 2)
1 1	Reserved

Advanced Sync Separator

Once the line rate has been determined, the signal can be analyzed by the advanced sync separator. This has been designed to be compatible with a wide range of video standards, operating with horizontal line rates up to 150kHz. PAL/NTSC/SECAM; HDTV, including bi-level and tri-level sync Standards and computer display syncs. The EL4511 can be programmed to disable the detection of either bi-level or tri-level sync signals or to prioritize the detection of one sync signal type over the other.

If the vertical sync input pin, VERTIN, is enabled, the EL4511 will automatically detect whether a valid signal is present on that pin, and incorporate that signal into the algorithm. Otherwise, the input signal on which the horizontal sync was detected will be treated as a composite sync. The sync separator also includes a qualification scheme which rejects high frequency noise and other video artifacts, such as color burst. The horizontal line rate is automatically acquired from the signal (see above.) A digital filter is included in the signal path to remove noise and glitches; this may be removed if the extra delay it incurs needs to be removed. Setting register 2, bit 4 to Low will remove the filter.

After the signal has been identified and the qualification process is complete, the SYNCLOCK pin will go high and the output waveforms will be enabled. These may be enabled all the time by setting register 1, bit 6 to a high state. This can help noisy and varying signals as the revalidation does not have to take place before the signals are available at the outputs, See Figures 2 through 5 for examples of various types of input signal.

Part of the signal recognition algorithm uses the number of horizontal lines between vertical pulses. A counter is clocked by the Hclock, this counter is also used to generate vertical timing pulses. This count information is available via the serial I/F; this is a 12 bit number.

The lines per frame count is available at register 8, bits 7:4 for the MSBs; the LSBs are available at register 7, bits 7:0. Register 8, bit 2 indicates that the lines/frame counter has been updated when it is high.

This counter also generates the V_{BLANK} waveform. Using a look up table, the default blanking is based on number of lines in the field. This operation may be disabled by setting register 3, bit 7 to a low. As this is dependent on application and product usage, this may be modified. Register 3, bits 6:0 will set the number of horizontal lines after VERTOUT leading edge. Register 4, bits 7:4 sets the number of lines before the VERTOUT leading edge.

Video Lock and Level Indicators

Loss of video signal can be detected by monitoring the SYNCLOCK pin 3. This pin goes high once the sync separator has detected a valid sync signal and goes low if this signal is lost for more than 20 successive lines. This

signal is also available at register 14 pin 5. Other lock acquisition signals available from the system are listed in Table 4.

The sync tip amplitude is buffered with a nominal gain of 2.15 to produce a positive, ground-referenced signal on the LEVEL pin. This output can be used for AGC applications.

TABLE 4. ACQUISITION CONTROL SIGNALS

REGISTER	BIT	SIGNAL NAME	DESCRIPTION
8	3	En50Slice	1=Sample and Hold front end is in use
8	1	Progressive	1=Progressive scan detected
8	0	Tri-Level Detected	1= Tri-Level syncs detected
9	5	$\overline{\text{ENLEVEL}}$ $\overline{\text{BLANKING}}$	1= V_{LEVEL} is available when system is not locked
9	4	$\overline{\text{ENLEVEL}}$	1=Disable V_{LEVEL} Output
9	2	$\overline{\text{ENALOS}}$	1=Analog loss of signal not used in lock indication.
14	5	SYNCLOCK	Same information as SYNCLOCK pin 3
16	4	RateLocked	Line rate is locked
16	3	ALOS	Sync Amplitude is below minimum

Mode Decode

In order to allow more flexibility when operating without a serial interface, the XTAL and XTALN pins are decoded by default to enable four control modes. These modes could be used to over-ride sync type used. See Table 5 for details.

The all-signal type allowed mode is the same as the default mode when the crystal oscillator is enabled (set bit 6 of Reg9 to 1) except the countsPerField function is disabled in Reg13 and Reg14.

The bi-level mode is for bi-level sync only, such as NTSC and PAL. The tri-level mode is for tri-level sync only, such as HDTV signals. The VGA only mode is for computer digital types of signals signal only.

The internal pull-up resistors on XTAL & XTALN are very high, these pins should use 10kΩ pull-up/down to operate when not using a crystal.

By default, the EL4511 will wake up with Register 9, bit 6 set to Low. This will allow the use of logic levels on pins 1 & 24 to drive register1, bits 5:3 and register 2 bit 0 into the combinations shown in Table 5.

To define the mode through the serial interface, the register 9, bit 6 must be set to High, the logic levels on pins 1 & 24 are no longer valid; (most likely now being an AC signal for the reference clock).

TABLE 5. MODE CONTROL USING PINS 1 & 24

ENXTAL	PIN 1 XTAL	PIN 24 XTALN	MODE CONTROL	DESCRIPTION
Register9 b 6			Register1 b5 b4 b3	
0	0	0	0 0 0	All signals enabled
0	0	1	0 1 1	Tri-Level Only
0	1	0	1 0 1	Bi-Level Only
0	1	1	1 1 1	VGA only
1	X	X	Set by Serial I/F	Crystal Oscillator is operational

Using the Reference Oscillator and Counter

A counter is provided for measuring the vertical time interval; this counts the clocks at the XTAL pin 1 between vertical pulses.

This information is not necessary for the operation of the chip; only for information to the system micro-control. The count value is read from register 14 at bits 7:6 for the MSBs, the LSBs are available in register 13, bits 7:0. Register 14, bit 4 should be a high to indicate that the read operation did not collide with the up-date timing.

If the crystal oscillator is enabled through the serial interface (Register 9, bit 6, ENXTAL), the XTAL and XTALN pins will become the crystal input and crystal output pins for the 32.7kHz crystal. It is also possible to drive the XTAL pin with a logic level clock up to a maximum of 50kHz; this signal is only used to measure the vertical rate.

Example:

Using a 32.768kHz crystal, the count period is 30.52µs. With a 20ms vertical rate, there will be approximately 656 cycles (290 Hex) in the "counts per field" registers 13 and 14. With a 16.666'ms vertical rate, the count of 546 (222 Hex) will be seen.

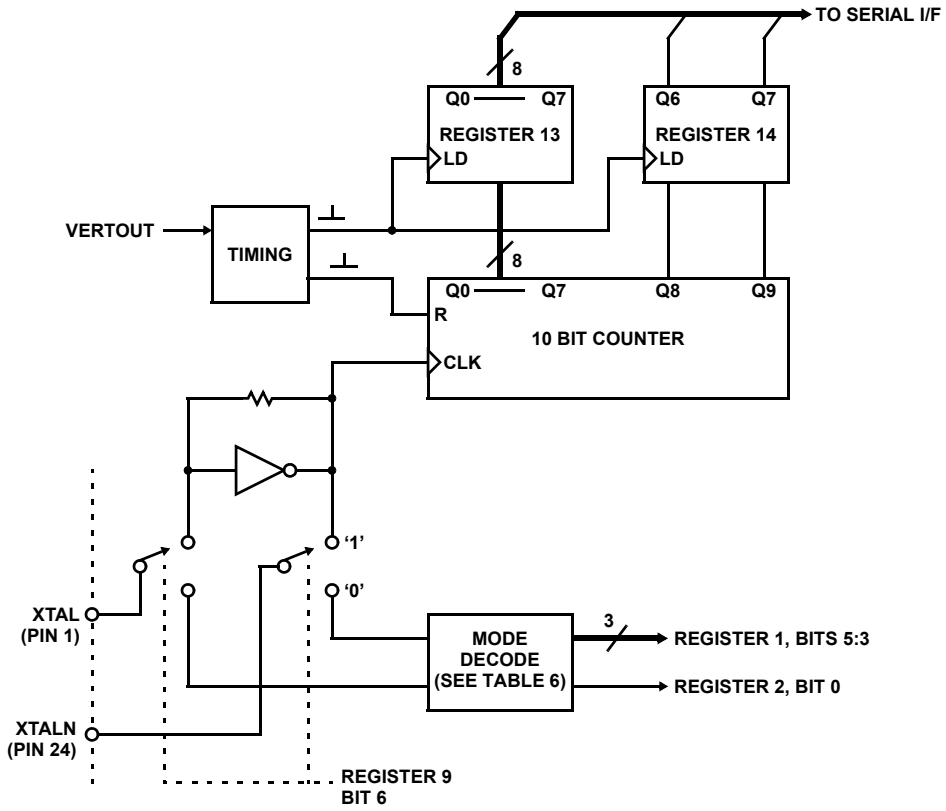


FIGURE 6. BLOCK DIAGRAM OF REFERENCE OSCILLATOR

Computer & Control Interface

In addition to the mode control pins, the chips default operating mode may be changed by way of a serial interface. This is of the three-wire type, Data, clock and /enable. After the /ENABLE line (pin 5) is taken low, the 16 bits of data on the SDA pin 7 will be clocked into the chip by the clock signal SCL pin 6. See Figure 7.

The first bit of the data determines whether it will be a read or write operation. When set to a "0", a write operation will take place. The following 7 bits, select the register to be written to. Finally, the last 8 bits are the data to be written or read. For a read operation, the first bit is a "1".

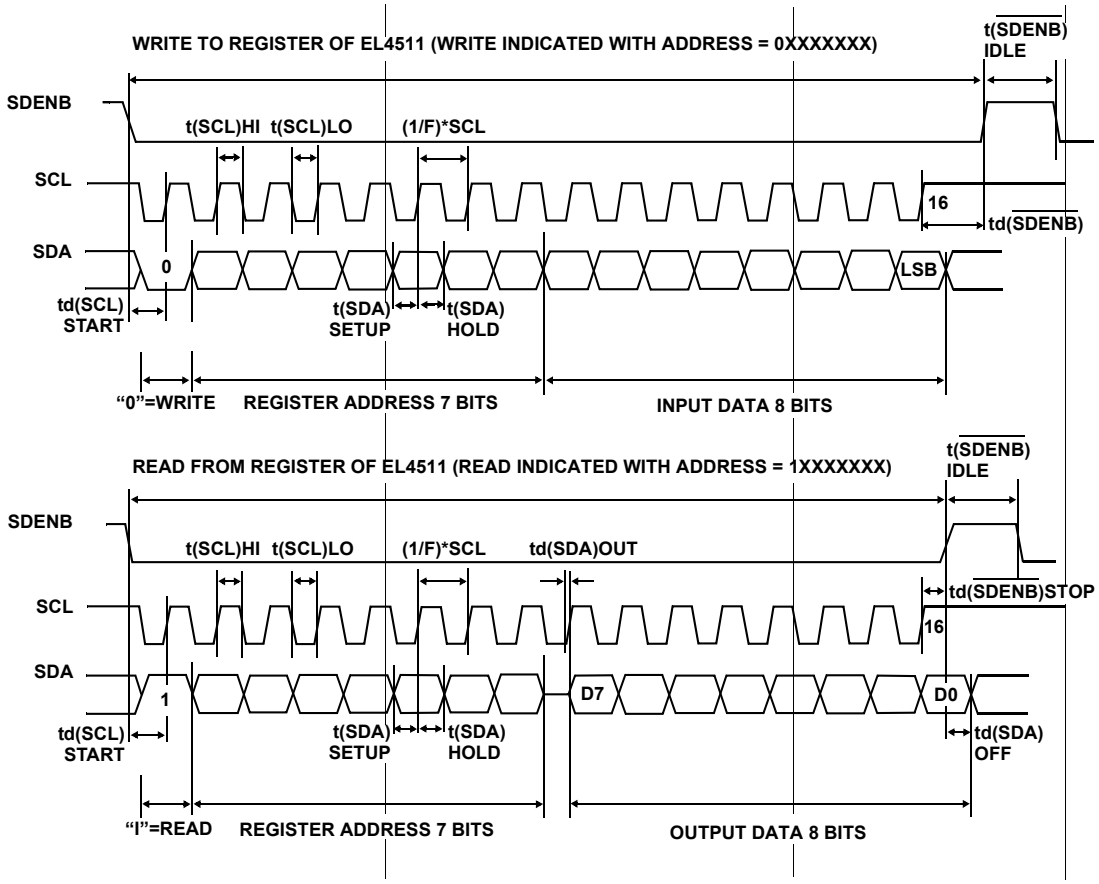


FIGURE 7. SERIAL INTERFACE TIMING DIAGRAM

Applications Examples

The following examples show how a system may be configured to operate the EL4511.

Application 1 (minimum circuitry application)

In this example, the requirement is for vertical and horizontal timing to be generated from either an NTSC/PAL composite video waveform, or a computer generated image with separate TTL level syncs.

The EL4511 has the advantage that the sync separation is carried out over a wide frequency range without the need to adjust "R_{SET}" as required by earlier generations of sync separators.

As there is no Microcontroller connected in this example, there is no need for a XTAL at pins 1 & 24. These pins are tied low, this enables the EL4511 to check for either type of input signal (See Table 5 for details.)

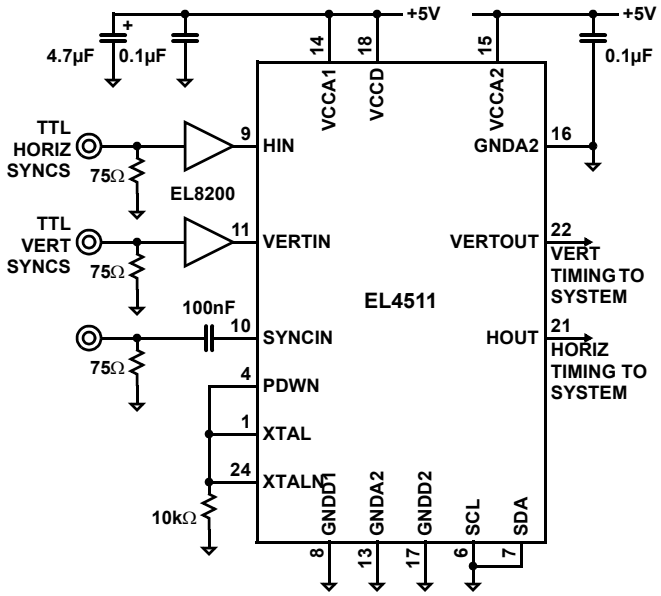


FIGURE 8. APPLICATIONS DRAWING 1

Application 2 (application using mode setting logic signals)

In this example, the requirement is to provide the synchronizing information in a small display device. In this example the incoming sync signals may come from one of three sources. Computer, HDTV Set-top Box or an NTSC/PAL tuner.

The EL4511 has the advantage that the sync separation is carried out over a wide frequency range without the need to adjust "R_{SET}" as required by earlier generations of sync separators.

As there is no Microcontroller connected in this example, there is no need for a XTAL at pins 1 & 24. These pins can be used to force the EL4511 to select the correct operation (and speed up acquisition).

Note that a Low Pas Filter is in the NTSC/PAL signal path to reduce noise, glitches and subcarrier. (In signals with bad Croma/Luma gain balance, the subcarrier can extend into the sync slicing level) (See Table 5 for details.)

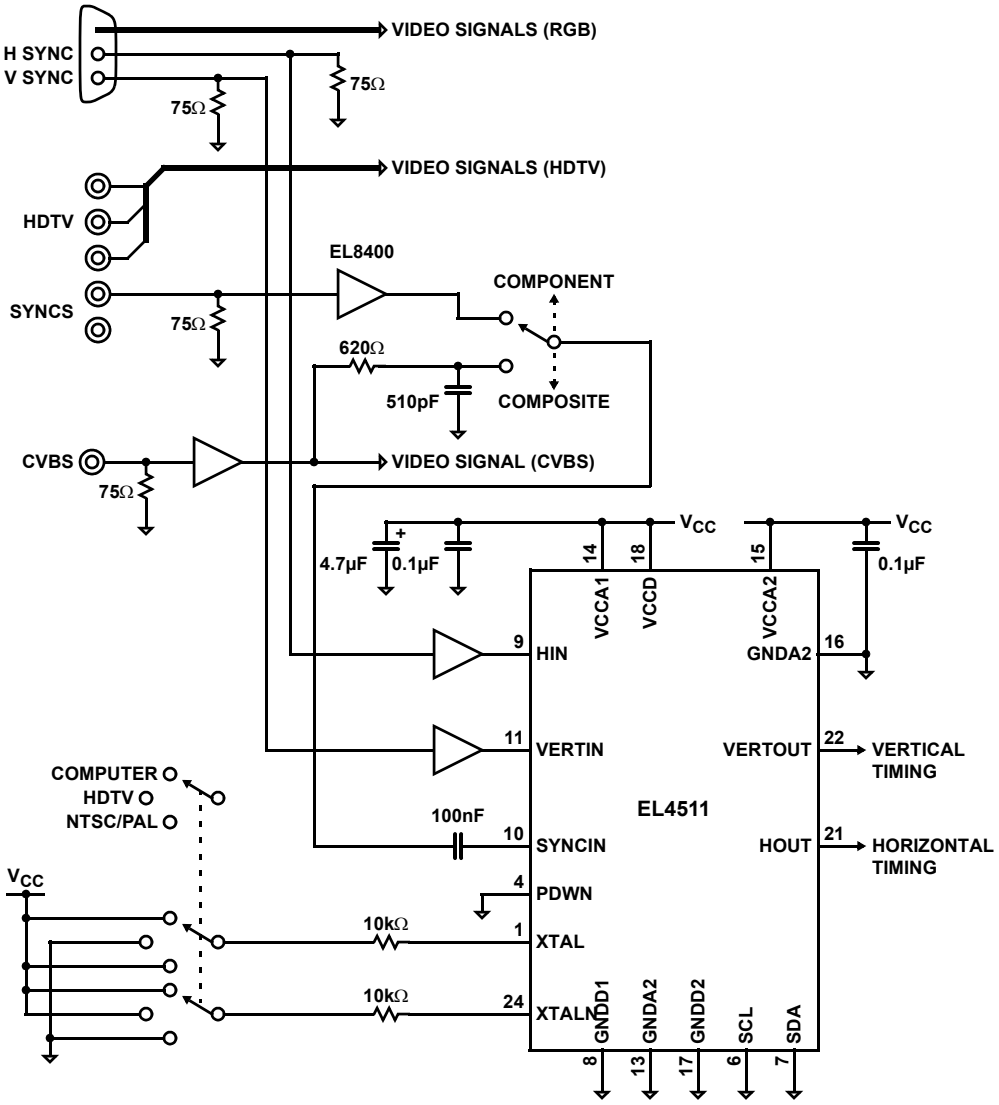


FIGURE 9. APPLICATIONS DRAWING 2

Application 3 (application using a microcontroller interface)

In this example, the requirement is to provide the synchronizing information in a video digitizing interface. This example is very similar to the example in application 2. In this example the incoming sync signals may come from one of three sources. Computer, HDTV source or an NTSC/PAL device.

As there is a Microcontroller connected in this example, a 32.768kHz XTAL is connected to pins 1 & 24; this will allow the system microcontroller to gather timing information for the vertical rate. To enable the crystal oscillator, register 9, bit 6 must be set to a high.

Note that a Low Pass Filter is in the NTSC/PAL signal path to reduce noise, glitches and subcarrier. (In signals with bad Croma/Luma gain balance, the subcarrier can extend into the sync slicing level).

As some of the signals in this application were non standard formats, the fixed slice mode is used by setting register 2, bit 5 to a high. Register 1, bit 6 is also set to a high. This forced the EL4511 to provide outputs even when the input signals are not recognized by the internal algorithms.

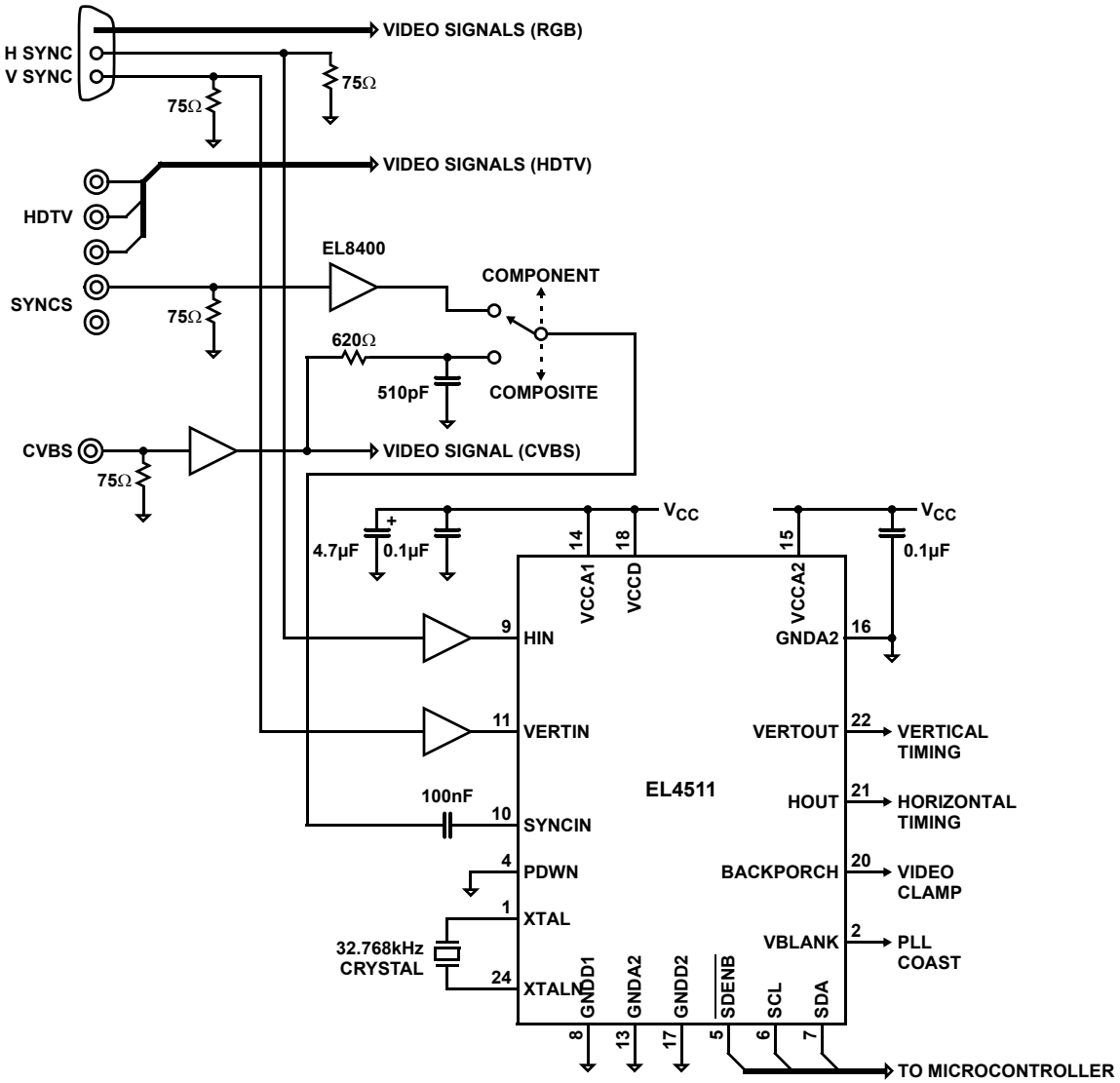


FIGURE 10. APPLICATIONS DRAWING 3

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