Ordering number : EN2666A

CMOS LSI

SANYO No. 2666A

LC5733, 5733H

SINGLE-CHIP 4-BIT MICROCOMPUTER WITH LCD DRIVERS FOR LOW-VOLTAGE, LOW-POWER USE

General Description

The LC5733/5733H are single-chip 4-bit microcomputers with LCD drivers. The features of the LC5733/5733H include low-voltage operation, low power dissipation, etc. The HALT function, which can be used to stop/start the CPU operations, facilitates the low power dissipation of the system. The LC5733/5733H are ideally suited for use in melody function-provided timepiece/timer applications.

♦ Hardware Features

- ROM ..... 2048 x 8 bits
- RAM ..... 128 x 4 bits
- Instruction execution time
  - 120μs ..... 1.3V to 1.65V (LC5733 Ag version)
  - 120μs ..... 2.6V to 3.6V (LC5733 Li version)
  - 60μs ..... 2.0V to 3.6V (LC5733 EXTV version)
  - 17.6μs .... 4.5V to 6.0V (LC5733H EXTV version)
- Current dissipation ..... 1.0μA typ at 1.55V (LC5733 Ag version): HALT mode
  0.8μA typ at 2.9V (LC5733 Li version): HALT mode
- Input/output pins ..... Number of input pins: 8
  Number of input/output pins: 8 (8 x 8 key matrix configuration available)
  Number of control output pins: 3 (Alarm output pins: 2, output pin: 1)
- LCD drivers

LCD display system	Number of drivable segments
Static	27 segments (max)
1/2bias-1/2duty	54 segments (max)
1/2bias-1/3duty	81 segments (max)

- Possible to use LCD drive output pins as output-only ports (mask option-selectable)
- On-chip melody function ..... 3 octaves
- On-chip segment PLA
  The LCD driver output can be used to support any LCD panel layout without software processing.
- On-chip step-up/step-down circuit
- Shipping style: FLP-64 (or chip)

♦ Software Features

- Powerful instruction set: 93 instructions
- Table read instruction (possible to set table in all ROM areas)
- 1-level subroutine nesting
- On-chip time-base 15-bits divider (delivers overflow signal every 32ms or 64ms/100ms/500ms when a 32.768kHz crystal OSC is used)
- HALT function

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Application Development Support System

- Evaluation chip (LC5797) is available for application development and the dedicated equipment is available as the application development tools.
- SDS-410 system
  Using the SDS-410, program development (editing, assembling) for microcomputer application circuit may be done. (IBM-PC* or its equivalent also available)
- EVA-510 + TB-5734 + DCB-1** + Application evaluation board + LC5797 (**Rev. 2.0 or greater)
  By connecting to the SDS-410, application development program correction and debugging may be done.
- TB-5734 + DCB-1** + Application evaluation board + LC5797
  By using the EPROM (2732) with application development program data written in, mounting evaluation may be done.

* The IBM-PC is an IBM-made product.

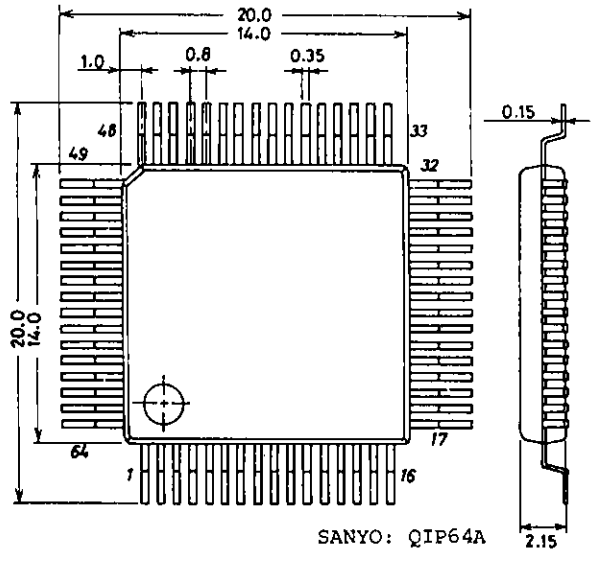
Note) The application evaluation board is constructed by the user.
LEDs or LCDs may be used for display.
The EVA-510 is a modified version of the EVA-410 whose monitor ROM is replaced by the SCR-5734.

Since the evaluation chip and the LC5733, 5733H differ in RAM capacity, be sure to check the RAM capacity when preparing or debugging programs.
LC5733: 128 x 4 bits
LC5797: 256 x 4 bits

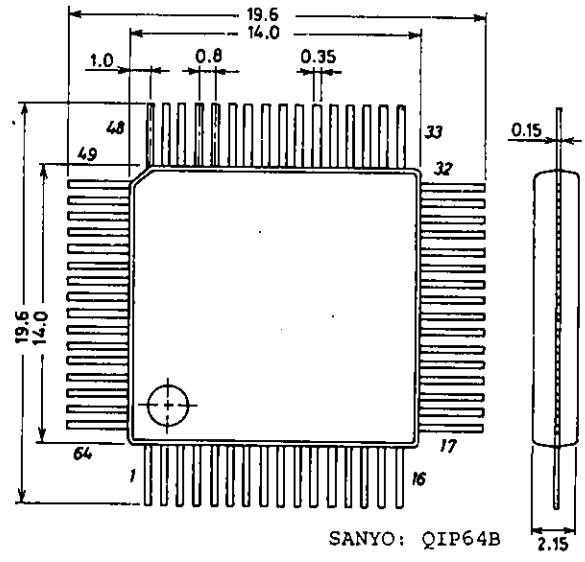
Sample Applications

- LCD game
- Multifunctional timepiece
- Timer
- Desk-top calculator

Package Dimensions 3057-Q64AIC
(unit: mm)



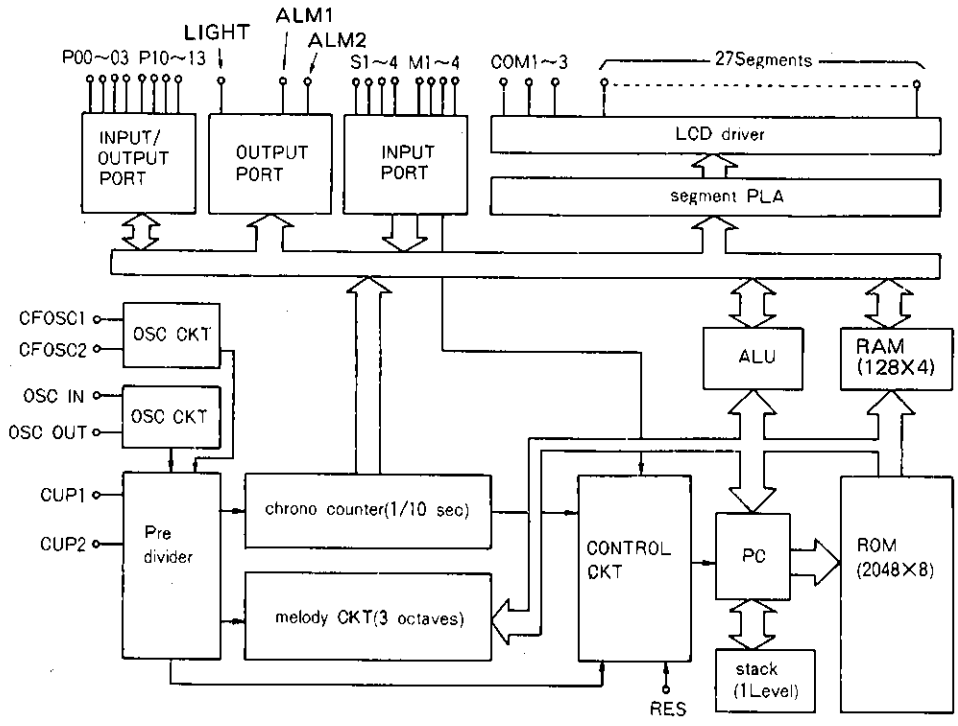
Package Dimensions 3026B-Q64BIC
(unit: mm)



When mounting the QIP package on the board, do not dip it in solder.

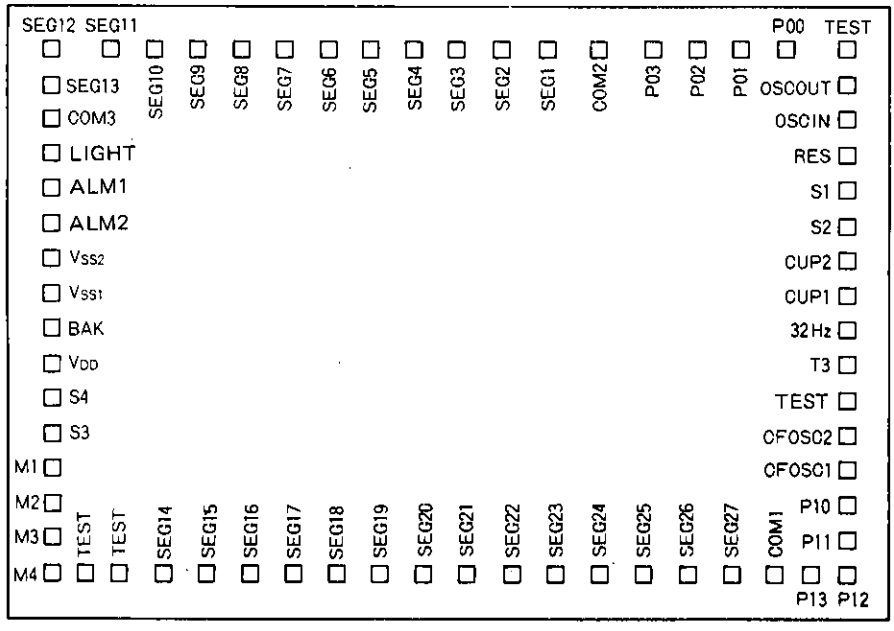
Note) When developing programs, take care of the DP_H value. The usable DPH values are 0 to 7. We will be will free from any blame even if you use DP_H=8 to F_H to develop programs.

Equivalent Circuit and Block Diagram



Pad Assignment of LSI Chip

Chip size:: 5.48mm x 3.70mm
Chip thickness: 480um
Pad size: 120um x 120um



Note) SEG14 to 27 can be used for output ports. (mask option-selectable)

Pad Name and Coordinates

QIP 64 Pin Assignment					QIP 64 Pin Assignment				
	Pad No.	Pin Name	X (μm)	Y (μm)		Pad No.	Pin Name	X (μm)	Y (μm)
26	1	V_{DD}	−300	2590	57	34	CUP1	45	−2590
27	2	S4	−485	2590	58	35	CUP2	255	−2590
28	3	S3	−710	2590	59	36	S2	460	−2590
29	4	M1	−1020	2590	60	37	S1	685	−2590
30	5	M2	−1245	2590	61	38	RES	915	−2590
31	6	M3	−1470	2590	62	39	OSCIN	1215	−2590
32	7	M4	−1700	2590	63	40	OSCOUT	1440	−2590
	8	TEST	−1700	2355	64	41	TEST	1700	−2590
	9	TEST	−1700	2130	1	42	P00	1700	−2265
33	10	SEG14	−1700	1860	2	43	P01	1700	−1975
34	11	SEG15	−1700	1640	3	44	P02	1700	−1680
35	12	SEG16	−1700	1420	4	45	P03	1700	−1390
36	13	SEG17	−1700	1200	5	46	COM2	1700	−960
37	14	SEG18	−1700	980	6	47	SEG1	1700	−605
38	15	SEG19	−1700	760	7	48	SEG2	1700	−385
39	16	SEG20	−1700	540	8	49	SEG3	1700	−165
40	17	SEG21	−1700	320	9	50	SEG4	1700	55
41	18	SEG22	−1700	100	10	51	SEG5	1700	275
42	19	SEG23	−1700	−120	11	52	SEG6	1700	495
43	20	SEG24	−1700	−340	12	53	SEG7	1700	715
44	21	SEG25	−1700	−560	13	54	SEG8	1700	935
45	22	SEG26	−1700	−780	14	55	SEG9	1700	1160
46	23	SEG27	−1700	−1000	15	56	SEG10	1700	1380
47	24	COM1	−1700	−1180	16	57	SEG11	1700	1600
48	25	P13	−1700	−1405	17	58	SEG12	1700	2590
49	26	P12	−1700	−2590	18	59	SEG13	1455	2590
50	27	P11	−1470	−2590	19	60	COM3	1225	2590
51	28	P10	−1260	−2590	20	61	LIGHT	1020	2590
52	29	CFOSC1	−1040	−2590	21	62	ALM1	810	2590
53	30	CFOSC2	−840	−2590	22	63	ALM2	615	2590
54	31	TEST	−630	−2590	23	64	V_{SS2}	330	2590
55	32	T3	−405	−2590	24	65	V_{SS1}	110	2590
56	33	32Hz	−180	−2590	25	66	BAK	−105	2590

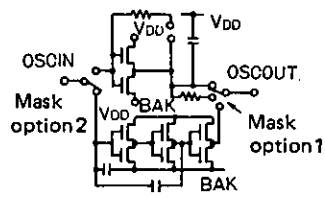
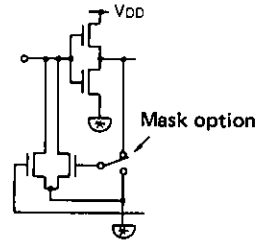
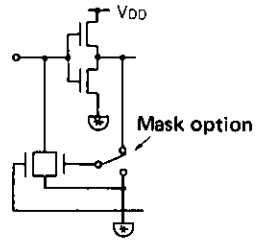
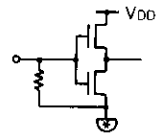
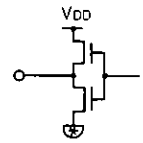
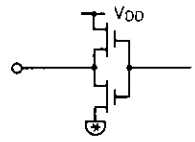
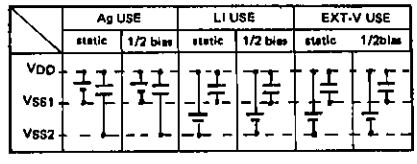
- The values (X, Y) indicate the coordinates of each pad center with the center of the chip as the origin.

Notes for developing an LC5730 series microcomputer-used system

The low current dissipation is a distinctive feature of the LC5730 series microcomputers. However, it is not easy to determine the total current to be dissipated in an LC5730 series microcomputer-used system by actual measurement when you develop a software, because much current flows in the peripherals of the evaluation tools.

For a system which requires low current dissipation, check the current dissipation using an evaluation sample before mass-producing the system.

Pin Description

Pad No.	Pin Name	Input/ Output	Circuit Configuration	Function
39	OSCIN	Input		1) Crystal OSC mode A crystal is connected across OSCIN and OSCOUT for oscillation. 2) RC OSC mode R (external resistance) is connected across OSCIN and OSCOUT and C (external capacitance) is connected across OSCIN and V_{DD} for oscillation.
40	OSCOUT	Output		
37 36 3 2	S1 S2 S3 S4	Input		Input-only port LSI system is reset by applying V_{DD} to S1 to S4 simultaneously.
4 5 6 7	M1 M2 M3 M4	Input		Input-only port.
38	RES	Input		Input pin for resetting LSI system.
66	BAK			(–) power supply pin for logic unit inside the LSI. For Li version, a capacitor must be connected across BAK and V_{DD} to prevent the logic unit from malfunctioning.
61	LIGHT	Output		Output-only pin Suited for delivering signal to drive transistor for light.
62 63	ALM1 ALM2	Output		Output-only pins Used to deliver *4kHz, 2kHz, 1kHz modulation signal with the execution of an instruction. Also used to deliver non-modulation signal. Used to deliver melody signal of 3 octaves with the execution of an instruction.
1	V_{DD}			(+) power supply pin.
64 65	V_{SS2} V_{SS1}			(–) power supply pins Ag version, Li version, EXT-V version: Mask option-selectable. 

Continued on next page.

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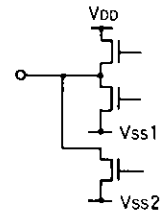
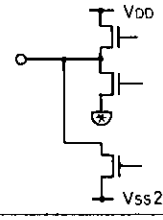
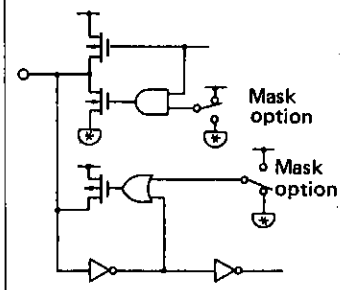
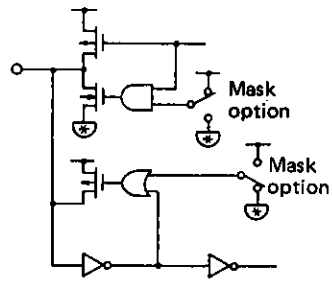
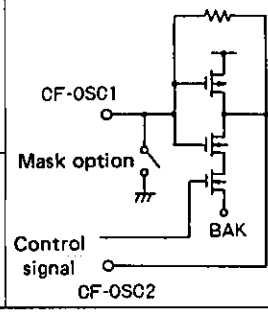
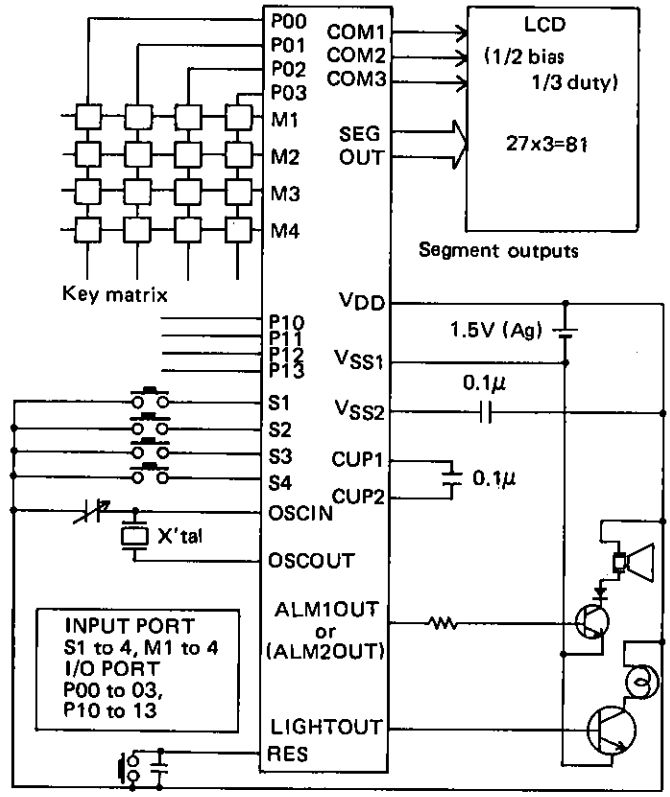
<table>
<tr><th>Pad No.</th><th>Pin Name</th><th>Input/ Output</th><th>Circuit Configuration</th><th>Function</th></tr>
<tr><td>34
35</td><td>CUP1
CUP2</td><td></td><td></td><td>Pins for connecting voltage step-up (step-down) capacitor.</td></tr>
<tr><td>24
46
60</td><td>COM1
COM2
COM3</td><td>Output</td><td> 
</td><td>Output pins for LCD panel common plate.
The following pin is used in each case.
<table>
<tr><th></th><th>Static</th><th>1/2duty</th><th>1/3duty</th></tr>
<tr><td>COM1</td><td>○</td><td>○</td><td>○</td></tr>
<tr><td>COM2</td><td>—</td><td>○</td><td>○</td></tr>
<tr><td>COM3</td><td>—</td><td>—</td><td>○</td></tr>
<tr><td>Alternating frequency</td><td>32Hz</td><td>32Hz</td><td>43Hz</td></tr>
</table>
(Alternating frequency is for 32.768kHz crystal OSC application.)</td></tr>
<tr><td>10
to
23
47
to
59</td><td>Segment Driver</td><td>Output</td><td> 
</td><td>Output pins for LCD panel segments.
Mask option permits SEG14 to SEG27 (Pad No. 10 to 23) to be used as output ports.</td></tr>
<tr><td>33
32
41
8
9
31</td><td>32Hz
T3
TEST</td><td>Test</td><td></td><td>Test pins (not used by user)</td></tr>
<tr><td>42
43
44
45</td><td>P-00
P-01
P-02
P-03</td><td>Input/ Output</td><td> 
</td><td>• 4-bit input/output port.
• Mask option can be used to select C-MOS output or P-ch open drain output.</td></tr>
<tr><td>28
27
26
25</td><td>P-10
P-11
P-12
P-13</td><td>Input/ Output</td><td> 
</td><td>• 4-bit input/output port.
• Mask option can be used to select C-MOS output or P-ch open drain output.</td></tr>
<tr><td>29</td><td>CF-OSC1</td><td>Input</td><td rowspan="2"> 
</td><td>Input pin used to provide OSC and also used for internal clock generation.
When no ceramic resonator is used, this input pin is set at "L" level by mask option.</td></tr>
<tr><td>30</td><td>CF-OSC2</td><td>Output</td><td>Output pin used to provide OSC.</td></tr>
</table>

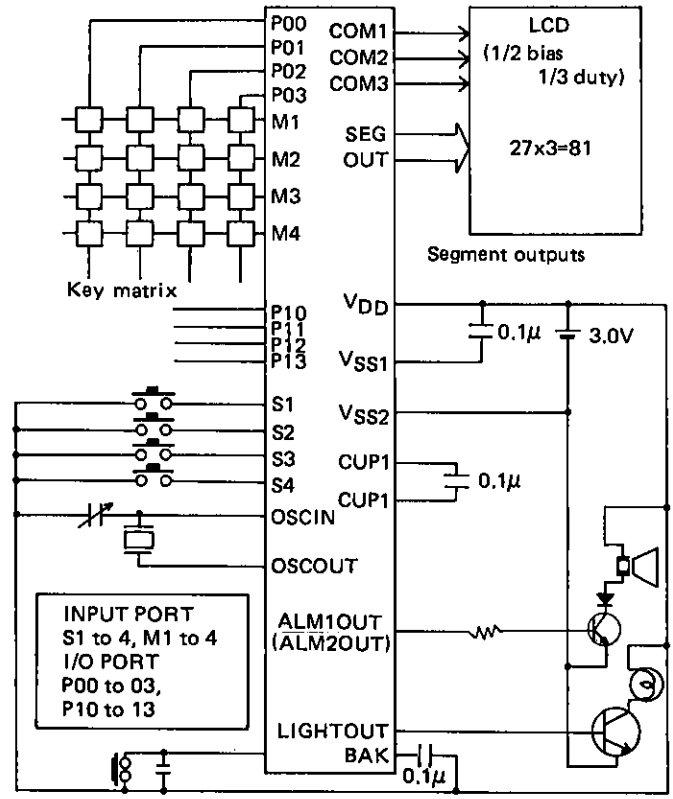
Note) For Ag battery power supply, ⏚ is connected to V_{SS1}, for Li battery /EXT-V power supply, ⏚ is connected to V_{SS2}.
*4kHz, 2kHz, 1kHz: For 32.768kHz crystal OSC application, Proportional to OSC frequency.

Sample Application Circuits

(1) Typical application circuit for Ag version (1/2bias, 1/3duty)

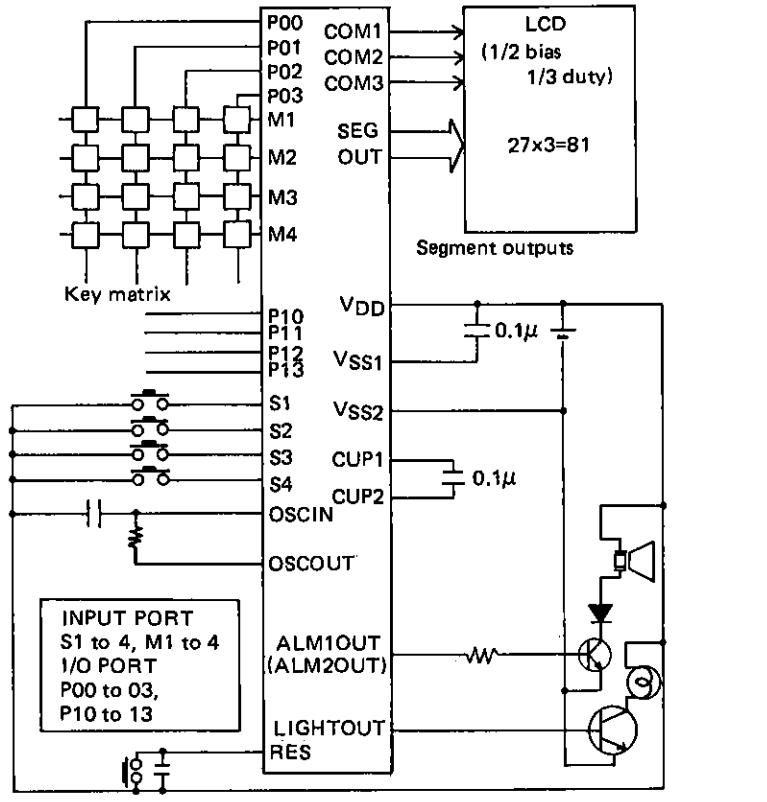


(2) Typical application circuit for Li version (1/2bias, 1/3duty)



Unit (capacitance: F)

(3) Typical application circuit for EXT-V version (1/2bias, 1/3duty)



Unit (capacitance: F)

● **Ag Version**

Absolute Maximum Ratings/Ta=25±2°C, V_{DD}=0V

			Limits	Unit
Maximum Supply Voltage	V_{SS1}		−4.0 to +0.3	V
	V_{SS2}		−4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	S1-4, M1-4, P00-03, P10-13,32Hz, TEST, OSC1N, RES	V_{SS1}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	32Hz, CUP2, OSCOUT, ALM1, ALM2, LIGHT P00-0.3, P10-13	V_{SS1}−0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1, COM2, COM3, CUP1	V_{SS2}−0.3 to 0.3	V
Operating Temperature	Topr		−30 to +70	°C
Storage Temperature	Tstg		−40 to +125	°C

Allowable Operating Conditions/Ta=−30 to +70°C, V_{DD}=0V

			Limits			unit
			min	typ	max	
Supply Voltage	V_{SS1}		−1.65		−1.30	V
	V_{SS2}		−3.3		−2.4	V
Input "H"-Level Voltage	V_{IH}	S1-4, M1-4, RES, P00-03, P10-13	−0.2		0	V
Input "L"-Level Voltage	V_{IL}	S1-4, M1-4, RES, P00-03 P10-13, 8Hz-IN	V_{SS1}		V_{SS1} +0.2	V
Operating Frequency	fopg1	Crystal OSC (Fig. 7)	32	32.768	33	kHz
	fopg2	RC OSC (Fig. 12)		32.768		kHz

Electrical Characteristics/Ta=−30 to +70°C, V_{DD}=0V

			Limits			Unit
			min	typ	max	
Input Resistance	R_{IN1A}	V_{SS1}=−1.55V, V_{IL}=V_{SS1}+0.2V, "L"-level hold Tr., *1, Fig. 1	200	800	2000	kΩ
	R_{IN1B}	V_{SS1}=−1.55V "L"-level pull-in Tr., *1, Fig. 1	50	100	200	kΩ
	R_{IN2A}	V_{SS1}=−1.55V, V_{IH}=−0.2V, "H"-level hold tr., *4, Fig. 6	100	400	2000	kΩ
	R_{IN3}	V_{SS1}=−1.55V, TEST, RES	10		300	kΩ
Output "H"-Level Voltage	V_{OH1}	V_{SS1}=−1.55V, I_{OH}=−0.4μA, *2	−0.2			V
Output "L"-Level Voltage	V_{OL1}	V_{SS1}=−1.55V, I_{OL}=0.4μA, *2			V_{SS2} +0.2	V
Output "H"-Level Voltage	V_{OH2}	V_{SS1}=−1.55V, I_{OH}=−4μA, COM1, COM2, COM3	−0.2			V
Output "M"-Level Voltage	V_{OM}	V_{SS1}=−1.55V, I_{OH}=−4μA, I_{OL}=4μA, COM1, COM2, COM3	V_{SS1} −0.2		V_{SS1} +0.2	V
Output "L"-Level Voltage	V_{OL2}	V_{SS1}=−1.55V, I_{OL}=4μA, COM1, COM2, COM3			V_{SS2} +0.2	V

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			Limits			Unit
			min	typ	max	
Output "H"-Level Voltage	V_{OH3}	V_{SS1}=−1.35V, I_{OH} =−250μA, LIGHT	−0.65			V
Output "L"-Level Voltage	V_{OL3}	V_{SS1}=−1.35V, I_{OL}=150μA, LIGHT			V_{SS1} +0.65	V
Output "H"-Level Voltage	V_{OH4}	V_{SS1}=−1.55V, I_{OH}=−20μA, *3	−0.2			V
Output "L"-Level Voltage	V_{OL4}	V_{SS1}=−1.55V, I_{OL}=20μA, *3			V_{SS1} +0.2	V
Output "H"-Level Voltage	V_{OH5}	V_{SS1}=−1.35V, I_{OH}=−1mA, ALM1, ALM2	−0.65			V
Output "L"-Level Voltage	V_{OL5}	V_{SS1}=−1.35V, I_{OL}=1mA, ALM1, ALM2			V_{SS1} +0.65	V
Output Current (H)	I_{OH}	V_{DD}−V_{SS1}=1.55V, V_{OH}=V_{SS1}×0.5 *4			−100	μA
Output Current (L)	I_{OL}	V_{DD}−V_{SS1}=1.55V, V_{OL}=V_{SS1}×0.5 *4	5			μA
Output Voltage	V_{SS2}	V_{SS1}=−1.35V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 2	−3.3		−2.5	V
Supply Current 1	I_{DD1}	V_{SS1}=−1.55V, C1=C2=0.1μF, Cg=20pF, CI ≦ 25kΩ Ta≦ 50°C Xtal OSC, HALT mode, Fig. 2		1.0	3.0	μA
Supply Current 2	I_{DD2}	V_{SS}=−1.55V, C1=C2=0.1μF, Rext=470kΩ, Cext=30pF RC OSC, HALT mode, Fig. 8 Ta≦ 50°C		5.0	15.0	uA
OSC Start Voltage	Vstt	Cg=20pF, Xtal OSC (CI ≦ 25kΩ), Fig. 3, Ta=25°C	−1.35			V
OSC Hold Voltage	V_{HOLD}	Cg=20pF, Xtal OSC (CI ≦ 25kΩ), Fig. 3, Ta=25°C	−1.65		−1.30	V
OSC Start Time	tstt	Cg=20pF, Xtal OSC, V_{SS1}=−1.35V (CI≦25kΩ), Fig. 3, Ta=25°C			10	s
OSC Compensation	20pF	RC OSC (OSCIN side)	16	20	24	pF

● **Li Version**

Absolute Maximum Ratings/Ta=25±2°C, V_{DD}=0V

			Limits	Unit
Maximum Supply Voltage	V_{SS1}		−4.0 to +0.3	V
	V_{SS2}		−4.0 to +0.3	
Maximum Input Voltage	V_{IN1}	OSCIN, 32Hz	V_{SS1}−0.3 to 0.3	V
	V_{IN2}	S1-4, M1-4, TEST, RES, P00-03,P10-13	V_{SS2}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	32Hz, CUP2, OSCOUT	V_{SS1}−0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1, COM2, COM3, CUP1, LIGHT, ALM1, ALM2, P00-03, P10-13	V_{SS2}−0.3 to 0.3	
Operating Temperature	Topr		−30 to +70	°C
Storage Temperature	Tstg		−40 to +125	°C

Allowable Operating Conditions/Ta=−30 to +70°C, V_{DD}=0V

			Limits			Unit
			min	typ	max	
Supply Voltage	V_{SS1}		−3.6		−1.3	V
	V_{SS2}		−3.6		−2.6	V
Input "H"-Level Voltage	V_{IH}	S1-4, M1-4, RES, P00-03, P10-13	−0.4		0	V
Input "L"-Level Voltage	V_{IL}	S1-4, M1-4, RES, P00-03 P10-13	V_{SS2}		V_{SS2} +0.4	V
Operating Frequency	fopg1	Crystal OSC (Fig. 7)	32	32.768	33	kHz

Electrical Characteristics/Ta=−30 to +70°C, V_{DD}=0V

			Limits			Unit
			min	typ	max	
Input Resistance	R_{IN1A}	V_{SS2}=−2.9V, V_{IL}=V_{SS2}+0.4V, "L"-level hold tr., *1, Fig. 4	150	300	1000	kΩ
	R_{IN1B}	V_{SS2}=−2.9V, "L"-level pull-in Tr., *1, Fig. 4	60	100	150	kΩ
	RIN2A	V_{SS2}=−2.9V, V_{IH}=−0.4V, "H"-level hold tr., *4, Fig. 6	200	600	2000	kΩ
	R_{IN3}	V_{SS2}=−2.9V, TEST, RES	10		300	kΩ
Output "H"-Level Voltage	V_{OH1}	V_{SS2}=−2.9V, I_{OH}=−0.4μA, *2	−0.2			V
Output "L"-Level Voltage	V_{OL1}	V_{SS2}=−2.9V, I_{OL}=0.4μA, *2			V_{SS2} +0.2	V
Output "H"-Level Voltage	V_{OH2}	V_{SS2}=−2.9V, I_{OH}=−4μA, COM1, COM2, COM3	−0.2			V
Output "M"-Level Voltage	V_{OM}	V_{SS2}=−2.9V, I_{OH}=−4μA, I_{OL}=4μA, COM1, COM2, COM3	V_{SS2}/2 −0.2		V_{SS2}/2 +0.2	V
Output "L"-Level Voltage	V_{OL2}	V_{SS2}=−2.9V, I_{OL}=4μA, COM1, COM2, COM3			V_{SS2} +0.2	V
Output "H"-Level Voltage	V_{OH3}	V_{SS2}=−2.4V, I_{OH}=−250μA, ALM1, ALM2	−0.65			V
Output "L"-Level Voltage	V_{OL3}	V_{SS2}=−2.4V, I_{OL}=250μA, ALM1, ALM2			V_{SS2} +0.65	V
Output "H"-Level Voltage	V_{OH4}	V_{SS2}=−2.4V, I_{OH}=−150μA LIGHT	−1.5			V
Output "L"-Level Voltage	V_{OL4}	V_{SS2}=−2.4V, I_{OL}=150μA LIGHT			V_{SS2} +1.5	V
Output Current (H) 1	I_{OH1}	V_{SS2}=−2.9V, V_{OH}=−0.4V, *3			−50	μA
Output Current (L) 1	I_{OL1}	V_{SS2}=−2.9V, V_{OL}=V_{SS2}+0.4V, *3	50			μA
Output Current (H) 2	I_{OH2}	V_{SS2}=−2.9V, V_{OH}=−0.4V, *4			−450	μA
Output Current (L) 2	I_{OL2}	V_{SS2}=−2.9V, V_{OL}=V_{SS2}+0.4V *4	450			μA
Output Voltage (halver)	V_{SS1}	V_{SS2}=−2.8V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 5			−1.35	V
Supply Current	I_{DD}	V_{SS2}=−2.9V, Xtal OSC (CI≦25kΩ) HALT mode, C1=C2=0.1μF, Ta≦50°C Cg=20pF, Fig. 5		0.8	2.5	μA
OSC Start Voltage 1	V_{Stt1}	Cg=20pF	−1.35			V
OSC hold Voltage 1	V_{HOLD1}	Xtal OSC (CI≦25kΩ), Fig. 3 Ta=25°C			−1.3	V
OSC Start Time	tstt	V_{SS1}=V_{SS2}=−1.35V, Cg=20pF Xtal OSC (CI≦25kΩ), Fig. 3, Ta=25°C			10	s

- **EXT-V Version (Xtal OSC, CF OSC, RC OSC)**

Absolute Maximum Ratings/Ta=25±2°C, V_{DD}=0V

			Limits	Unit
Maximum Supply Voltage	V_{SS1}		−7.0 to +0.3	V
	V_{SS2}		−7.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	OSCIN, 32Hz, CF-OSC1	V_{SS2}−0.3 to 0.3	V
	V_{IN2}	S1-4, M1-4, TEST, RES, P00-03, P10-13	V_{SS2}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	32Hz, CUP2, OSCOUT, CF-OSC2	V_{SS2}−0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1, COM2, COM3, CUP1, LIGHT, ALM1, ALM2, P00-03, P10-13	V_{SS2}−0.3 to 0.3	V
Operating Temperature	Topr		−30 to +70	°C
Storage Temperature	Tstg		−40 to + 125	°C

Allowable Operating Conditions/Ta=−30 to +70°C, V_{DD}=0V

			Limits			Unit
			min	typ	max	
Supply Voltage	V_{SS1}		−6.0		−1.30	V
	V_{SS2}		−6.0		−2.0	V
Input "H"-Level Voltage	V_{IH1}	S1-4, M1-4, P00-03, P10-13	0.3X V_{SS2}		0	V
Input "L"-Level Voltage	V_{IL1}	S1-4, M1-4, P00-03, P10-13	V_{SS2}		0.7X V_{SS2}	V
Input "H"-Level Voltage	V_{IH2}	RES	0.25X V_{SS2}		0	V
Input "L"-Level Voltage	V_{IL2}	RES	V_{SS2}		0.75X V_{SS2}	V
Operating Frequency	f_{opg1}	Crystal OSC 1 (Fig. 7)	32	32.768	33	kHz
	f_{opg2}	Crystal OSC2 (Fig. 7)	60	65.536	70	kHz
	f_{CF}	CF OSC (Fig. 13), (Cycle time 16μs at CF=500kHz)	380	455	500	kHz
	f_{CR}	RC OSC (Fig. 12)		32.768		kHz

Electrical Characteristics/Ta=−30 to +70°C, V_{DD}=0V

			Limits			Unit
			min	typ	max	
Input Resistance	R_{IN1A}	V_{SS2}=−2.9V, V_{IL}=V_{SS2}+0.4V, "L"-level hold tr., *1, Fig. 4	150	300	1000	kΩ
	R_{IN1B}	V_{SS2}=−2.9V, "L"-level pull-in Tr., *1, Fig. 4	60	100	150	kΩ
	R_{IN2A}	V_{SS2}=−2.9V, V_{IH}=−0.4V, "H"-level hold tr., *4, Fig. 6	200	600	2000	kΩ
	R_{IN3}	V_{SS2}=−2.9V, TEST, RES	10		300	kΩ
Output "H"-Level Voltage	V_{OH1}	V_{SS2}=−2.9V, I_{OH}=−0.4μA, *2	−0.2			V
Output "L"-Level Voltage	V_{OL1}	V_{SS2}=−2.9V, I_{OL}=0.4μA, *2			V_{SS2} +0.2	V
Output "H"-Level Voltage	V_{OH2}	V_{SS2}=−2.9V, I_{OH}=−4μA, COM1, COM2, COM3	−0.2			V
Output "M"-Level Voltage	V_{OM}	V_{SS2}=−2.9V, I_{OH}=−4μA, I_{OL}=4μA, COM1, COM2, COM3	V_{SS2}/2 −0.2		V_{SS2}/2 +0.2	V
Output "L"-Level Voltage	V_{OL2}	V_{SS2}=−2.9V, I_{OL}=4μA COM1, COM2, COM3			V_{SS2} +0.2	V
Output "H"-Level Voltage	V_{OH3}	V_{SS2}=−2.4V, I_{OH}=−2.0mA, ALM1, ALM2	−1.0			V
Output "L"-Level Voltage	V_{OL3}	V_{SS2}=−2.4V, I_{OL}=2.0mA, ALM1, ALM2			V_{SS2} +1.0	V
Output "H"-Level Voltage	V_{OH4}	V_{SS2}=−2.4V, I_{OH}=−250μA, LIGHT	−0.65			V
Output "L"-Level Voltage	V_{OL4}	V_{SS2}=−2.4V, I_{OL}=250μA, LIGHT			V_{SS2} +0.65	V
Output Current (H) 1	I_{OH1}	V_{SS2}=−3.0V, V_{OH}=−0.45V, *3			−45	μA
Output Current (L) 1	I_{OL1}	V_{SS2}=−3.0V, V_{OL}=V_{SS2}+0.45V, *3	45			μA
Output Current (H) 2	I_{OH2}	V_{SS2}=−3.0V, V_{OH}=−0.45V, *4			−450	μA
Output Current (L) 2	I_{OL2}	V_{SS2}=−3.0V, V_{OL}=V_{SS2}+0.45V, *4	450			μA
Output Voltage (halver)	V_{SS1}	V_{SS2}=−2.9V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 5		−1.45	−1.35	V

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			Limits			Unit
			min	typ	max	
Supply Current 1	I_{DD1}	V_{SS2}=−3.0V, 32.768kHz Xtal OSC (CI≦25kΩ), Ta≦50°C, HALT mode, C1=C2=0.1μF, Cg=20pF, Fig. 5		3.0	15	μA
Supply Current 2	I_{DD2}	V_{SS2}=−3.0V, 65.536kHz Xtal OSC (CI≦25kΩ), Ta≦50°C, HALT mode, C1=C2=0.1μF, (Cd=20pF), Cg=10pF Fig. 5		8.0	30	μA
Supply Current 3	I_{DD3}	V_{SS2}=−3.0V, 455kHz CF OSC, HALT mode, C1=C2=0.1μF, C_{CFI}=C_{CFO}=150pF, Rf=1MΩ, Ta≦50°C, Fig. 10		80	300	μA
Supply Current 4	I_{DD4}	V_{SS2}=−3.0V, R_{EXT}=470kΩ, Cext=30pF, C1=C2=0.1uF, Ta≦50°C, Fig. 9		40	150	μA
OSC Start Voltage 1	Vstt1	Cg=20pF	−2.3			V
OSC Hold Voltage 1	V_{HOLD1}	32.768kHz Xtal OSC (CI≦25kΩ), Fig. 3, Ta=25°C			−2.0	V
OSC Start Time 1	tstt1	V_{SS2}=−2.3V, Cg=20pF 32.768kHz Xtal OSC (CI≦25kΩ), Fig. 3, Ta=25°C			10	s
OSC Start Voltage 2	Vstt2	Cg=10pF (Cd=20pF), 65.536kHz Xtal OSC (CI≦25kΩ),	−2.6			V
OSC Hold Voltage 2	V_{HOLD2}	Fig. 3, Ta=25°C			−2.4	V
OSC Start Time 2	tstt2	V_{SS2}=−2.6V, Cg=10pF (Cd=20pF), Ta=25°C, 65.536kHz Xtal OSC (CI≦25kΩ), Fig. 3			10	s
OSC Start Voltage 3	Vstt3	C_{CFI}=C_{CFO}=150pF, 455kHz CF OSC,	−2.0			V
OSC Hold Voltage 3	V_{HOLD3}	Rf=1MΩ, Fig. 11, Ta=25°C			−2.0	V
OSC Start Time 3	tstt3	C_{CFI}=C_{CFO}=150pF, 455kHz CF OSC, Rf=1MΩ, Fig. 11, V_{SS2}=−2.0V, Ta=25°C			30	ms

LC5733H Version

- **EXT-V Version (Xtal OSC, CF OSC, RC OSC)**

Absolute Maximum Ratings/Ta=25±2°C, V_{DD}=0V

			Limits	Unit
Maximum Supply Voltage	V_{SS1}		−7.0 to +0.3	V
	V_{SS2}		−7.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	OSCIN, 32Hz, CF-OSC1	V_{SS2}−0.3 to 0.3	V
	V_{IN2}	S1-4, M1-4, TEST, RES, P00-0.3, P10-13	V_{SS2}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	32Hz, CUP2, OSCOUT, CF-OSC2	V_{SS2}−0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1, COM2, COM3, CUP1, LIGHT, ALM1, ALM2, P00-03, P10-13	V_{SS2}−0.3 to 0.3	V
Operating Temperature	Topr		−30 to +70	°C
Storage Temperature	Tstg		−40 to + 125	°C

Allowable Operating Conditions/Ta=−30 to +70°C, V_{DD}=0V

			Limits			Unit
			min	typ	max	
Supply Voltage	V_{SS1}		−6.0		−2.20	V
	V_{SS2}		−6.0		−4.5	V
Input "H"-Level Voltage	V_{IH1}	S1-4, M1-4, P00-03, P10-13	0.3X V_{SS2}		0	V
Input "L"-Level Voltage	V_{IL1}	S1-4, M1-4, P00-03, P10-13	V_{SS2}		0.7X V_{SS2}	V
Input "H"-Level Voltage	V_{IH2}	RES	0.25X V_{SS2}		0	V
Input "L"-Level Voltage	V_{IL2}	RES	V_{SS2}		0.75X V_{SS2}	V
Operating Frequency	f_{opg1}	Crystal OSC 1 (Fig. 7)	32	32.768	33	kHz
	f_{opg2}	Crystal OSC2 (Fig. 7)	60	65.536	70	kHz
	f_{CF}	CF OSC (Fig. 13), (Cycle time 16μs at CF=500kHz)	380	455	500	kHz
	f_{CR}	RC OSC (Fig. 12)		32.768		kHz

Electrical Characteristics/Ta=−30 to +70°C, V_{DD}=0V

			Limits			Unit
			min	typ	max	
Input Resistance	R_{IN1A}	V_{SS2}=−5.0V, V_{IL}=V_{SS2}+0.4V, "L"-level hold tr., *1, Fig. 4	70	200	600	kΩ
	R_{IN1B}	V_{SS2}=−5.0V, "L"-level pull-in Tr., *1, Fig. 4	60	100	150	kΩ
	R_{IN2A}	V_{SS2}=−5.0V, V_{IH}=−0.4V, "H"-level hold tr., *4, Fig. 6	100	400	1000	kΩ
	R_{IN3}	V_{SS2}=−5.0V, TEST, RES	10		300	kΩ
Output "H"-Level Voltage	V_{OH1}	V_{SS2}=−5.0V, I_{OH}=−0.4μA, *2	−0.2			V
Output "L"-Level Voltage	V_{OL1}	V_{SS2}=−5.0V, I_{OL}=0.4μA, *2			V_{SS2} +0.2	V
Output "H"-Level Voltage	V_{OH2}	V_{SS2}=−5.0V, I_{OH}=−4μA, COM1, COM2, COM3	−0.2			V
Output "M"-Level Voltage	V_{OM}	V_{SS2}=−5.0V, I_{OH}=−4μA, I_{OL}=4μA, COM1, COM2, COM3	V_{SS2}/2 −0.2		V_{SS2}/2 +0.2	V
Output "L"-Level Voltage	V_{OL2}	V_{SS2}=−5.0V, I_{OL}=4μA COM1, COM2, COM3			V_{SS2} +0.2	V
Output "H"-Level Voltage	V_{OH3}	V_{SS2}=−5.0V, I_{OH}=−2.0mA, ALM1, ALM2	−1.0			V
Output "L"-Level Voltage	V_{OL3}	V_{SS2}=−5.0V, I_{OL}=2.0mA, ALM1, ALM2			V_{SS2} +1.0	V
Output "H"-Level Voltage	V_{OH4}	V_{SS2}=−5.0V, I_{OH}=−250μA, LIGHT	−0.65			V
Output "L"-Level Voltage	V_{OL4}	V_{SS2}=−5.0V, I_{OL}=250μA, LIGHT			V_{SS2} +0.65	V
Output Current (H) 1	I_{OH1}	V_{SS2}=−5.0V, V_{OH}=−0.75V, *3			−75	μA
Output Current (L) 1	I_{OL1}	V_{SS2}=−5.0V, V_{OL}=V_{SS2}+0.75V, *3	75			μA
Output Current (H) 2	I_{OH2}	V_{SS2}=−5.0V, V_{OH}=−0.75V, *4			−750	μA
Output Current (L) 2	I_{OL2}	V_{SS2}=−5.0V, V_{OL}=V_{SS2}+0.75V, *4	750			μA
Output Voltage (halver)	V_{SS1}	V_{SS2}=−5.0V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 5			−2.4	V

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			Limits			Unit
			min	typ	max	
Supply Current 1	I_{DD1}	V_{SS2}=−5.0V, 32.768kHz Xtal OSC (CI≦25kΩ), Ta≦50°C, HALT mode, C1=C2=0.1μF, Cg=20pF, Fig. 5		8.0	50	μA
Supply Current 2	I_{DD2}	V_{SS2}=−5.0V, 65.536kHz Xtal OSC (CI≦25kΩ), Ta≦50°C, HALT mode, C1=C2=0.1μF, Cg=10pF (Cd=20pF), Fig. 5		20	100	μA
Supply Current 3	I_{DD3}	V_{SS2}=−5.0V, 455kHz CF OSC, HALT mode, C1=C2=0.1μF, C_{CFI}=C_{CFO}=150pF, Rf=1MΩ, Ta≦50°C, Fig. 10		300	400	μA
Supply Current 4	I_{DD4}	V_{SS2}=−5.0V, R_{EXT}=470kΩ, Cext=30pF, C1=C2=0.1uF, Ta≦50°C, Fig. 9		200	400	μA
OSC Start Voltage 1	Vstt1	Cg=20pF	−2.3			V
OSC Hold Voltage 1	V_{HOLD1}	32.768kHz Xtal OSC (CI≦25kΩ), Fig. 3, Ta=25°C			−2.0	V
OSC Start Time 1	tstt1	V_{SS2}=−2.3V, Cg=20pF 32.768kHz Xtal OSC (CI≦25kΩ), Fig. 3, Ta=25°C			10	s
OSC Start Voltage 2	Vstt2	Cg=10pF(Cd=20pF), 65.536kHz Xtal OSC (CI≦25kΩ),	−2.6			V
OSC Hold Voltage 2	V_{HOLD2}	Fig. 3, Ta=25°C			−2.4	V
OSC Start Time 2	tstt2	Ta=25°C V_{SS2}=−2.6V, Cg=10pF (Cd=20pF) 65.536kHz Xtal OSC (CI≦25kΩ), Fig. 3			10	s
OSC Start Voltage 3	Vstt3	C_{CFI}=C_{CFO}=150pF, 455kHz CF OSC	−2.0			V
OSC Hold Voltage 3	V_{HOLD3}	Rf=1MΩ, Fig. 11, Ta=25°C			−2.0	V
OSC Start Time 3	tstt3	C_{CFI}=C_{CFO}=150pF, 455kHz CF OSC, Rf=1MΩ, Fig. 11, V_{SS2}=−2.0V, Ta=25°C			30	ms

*1 S1, S2, S3, S4, M1, M2, M3, M4
*2 LCD driver output pins of SEGOUT1 to 13 and SEGOUT14 to 27.
*3 Output pins (used as output port) of SEGOUT14 to 27.
*4 P-00, P-01, P-02, P-03, P-10, P-11, P-12, P-13.

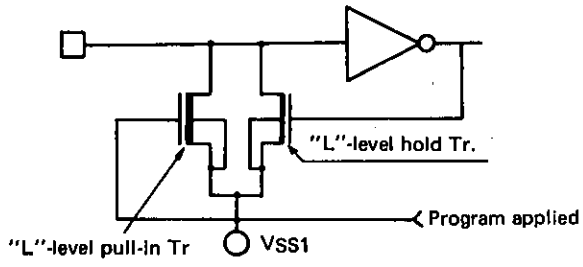

Fig. 1 Input configuration of S1-4, M1-4

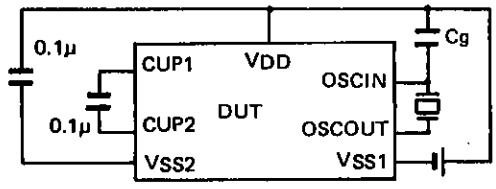

Fig. 2 Current dissipation, output voltage test circuit

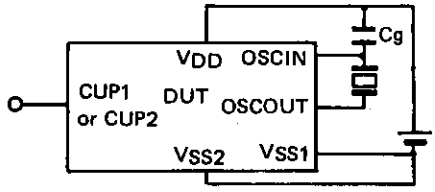

Fig. 3 Oscillation start voltage, oscillation start time, frequency stability, oscillation hold voltage test circuit.

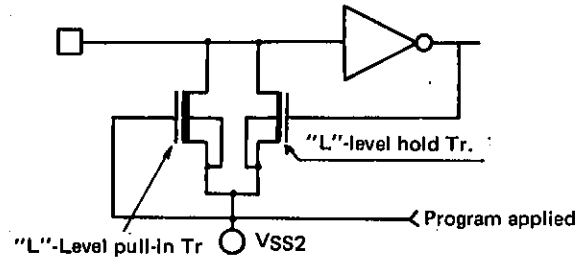

Fig. 4 Input configuration of S1-4, M1-4

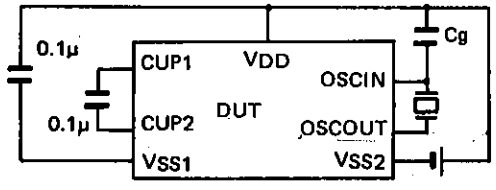

Fig. 5 Current dissipation, output voltage test circuit.

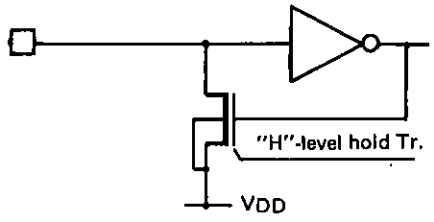

Fig. 6 Input configuration of P00-03, P10-13

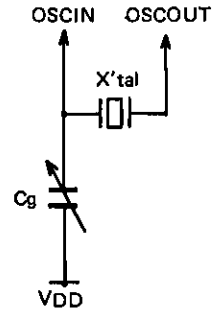

Fig. 7 Crystal oscillator

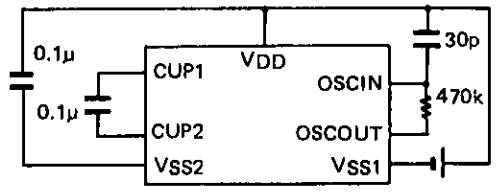

Fig. 8 Current dissipation, output voltage test circuit.

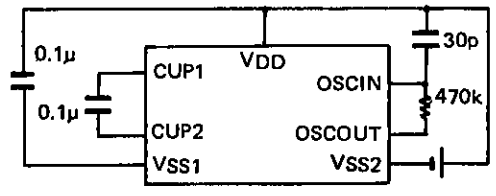

Fig. 9 Current dissipation, output voltage test circuit.

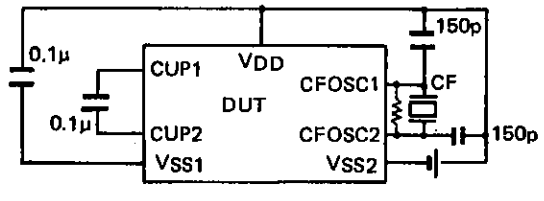

Fig. 10 Current dissipation, output voltage test circuit.

Unit (resistance: Ω, capacitance: F)

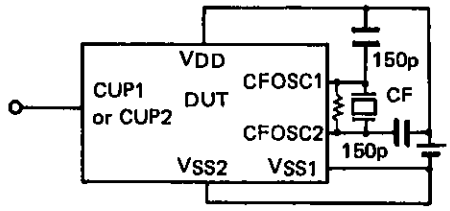

Fig. 11 Oscillation start voltage, oscillation start time, frequency stability, oscillation hold voltage test circuit.

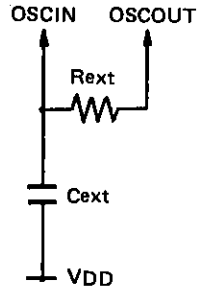

Fig. 12 RC oscillation

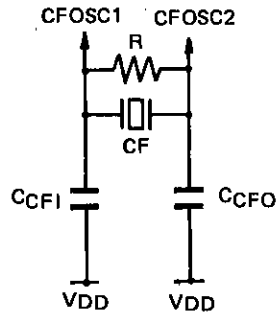

Fig. 13 CF oscillation

Unit (capacitance: F)

LC5733 Instruction Map

Instruction set: 93 instructions

1-cycle instruction ····· 1-byte instruction

2-cycle instruction ····· 2-byte instruction

LOWER / UPPER	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	HALT	TAAT	TWRT	TMEL	CSP	CST	RC5	SC5	JMP X							
1	JMP*	PAGE	MTR	RTS	MPCL	MPCM	MPCH	IN	ASR0	ASR1	ASL0	ASL1	SDPL	SDPH	EDPL	EDPH
2	MVI X															
3	LDI X															
4	BAZ X								BAB0 X							
5	BANZ X								BAB1 X							
6	BCNH X								BAB2 X							
7	BCH X								BAB3 X							
8	ADC	SBC	ADD	SUB	ADN	AND	EOR	OR	ADC*	SBC*	ADD*	SUB*	ADN*	AND*	EOR*	OR*
9	ADCI	SBCI	ADDI	SUBI	ADNI	ANDI	EORI	ORI	INC	DEC	IDPL	DDPL	IDPH	DDPH	ISP	DSP
A	JSR X								IPM	LDA	LSP	LHLT	L500	STA	SSP	IPS
B	MDPL X															
C	MDPH X															
D	SIC X															
E	MSP X															
F	RCF	SCF	RLGT	SLGT	SPDR X				RBAK	SBAK	SAS X	CSEC	OUT	LDPL	LDPH	NOP

Instruction Set of LC5733

Summary of LC5733 Instructions

Symbol Meaning

AC	: Accumulator	M(DP)	: Memory addressed by DP	( ), [ ]	: Contents
ACn	: Accumulator bit	[P( )]	: Contents of port ( )	←	: Transfer direction, result
DP	: Data pointer	PC	: Program counter	∧	: AND
EDP	: Save data pointer	STACK	: Stack register	∨	: OR
SP	: Strobe pointer	[M(DP)]	: Contents of memory	∀	: Exclusive OR
CF	: Carry flag		addressed by DP		
TREG	: Temporary register	STSn	: Status register		
SCFn	: Start condition flag n	CSTF	: Chrono start flag		
HEFn	: Halt enable flag n	PDF	: Pull-down flag		
L(SP)	: LCD latch specified by SP	PAGE	: Page latch		
M	: Memory	PGX	: Current Page		

Instruction	Mnemonic		Instruction code D7 D6 D5 D4 D3 D2 D1 D0	Bytes	Cycles	Function	Description	Status flag to be affected
Accumulator manipulation instructions, memory manipulation instructions	RCF	Reset CF	1 1 1 1 0 0 0 0	1	1	CF ← 0	The CF is reset.	CF
	SCF	Set CF	1 1 1 1 0 0 0 1	1	1	CF ← 1	The CF is set.	CF
	ASR0	Shift Right AC & MSB=0	0 0 0 1 1 0 0 0	1	1	ACn ← ACn+1 AC_3 ← 0	The AC contents are shifted right and 0 is loaded to the MSB.	
	ASR1	Shift Right AC & MSB=1	0 0 0 1 1 0 0 1	1	1	ACn ← ACn+1 AC_3 ← 1	The AC contents are shifted right and 1 is loaded to the MSB.	
	ASL0	Shift Left AC & LSB=0	0 0 0 1 1 0 1 0	1	1	ACn ← ACn−1 AC_0 ← 0	The AC contents are shifted left and 0 is loaded to the LSB.	
	ASL1	Shift Left AC & LSB=1	0 0 0 1 1 0 1 1	1	1	ACn ← ACn−1 AC_0 ← 1	The AC contents are shifted left and 1 is loaded to the LSB.	
	INC	Increment M(DP)	1 0 0 1 1 0 0 0	1	1	M(DP),AC ← M(DP)+1	The memory M(DP) contents are incremented (+1) and are loaded to the M(DP) and AC.	
	DEC	Decrement M(DP)	1 0 0 1 1 0 0 1	1	1	M(DP),AC ← M(DP)-1	The memory M(DP) contents are decremented (−1) and are loaded to the M(DP) and AC.	
	TAAT	Read table data from program ROM	0 0 0 0 0 0 0 1	1	2	AC, TREG ← ROM (PGX, AC, M(DP))	The contents of the ROM on current page addressed by the PC whose low-order 8 bits are replaced with the contents of the AC and M(DP) are loaded to the AC and TREG.	
	MTR	Store TREG to M(DP)	0 0 0 1 0 0 1 0	1	1	M(DP) ← TREG	The TREG contents are stored to the M(DP).	
Operation instructions	ADC	Add M(DP) to AC with CF	1 0 0 0 0 0 0 0	1	1	AC ← (AC)+[M(DP)] +(CF)	The AC, memory [M(DP)], CF contents are binary-added and the result is loaded to the AC.	CF
	ADC*	Add M(DP) to AC with CF	1 0 0 0 1 0 0 0	1	1	AC, M(DP) ← (AC)+[M(DP)] +(CF)	The AC, memory [M(DP)], CF contents are binary-added and the result is loaded to the AC and M(DP).	CF
	SBC	Subtract M(DP) from AC with CF	1 0 0 0 0 0 0 1	1	1	AC ← (AC)+$\overline{[M(DP)]}$ +(CF)	The memory M(DP), CF contents are binary-subtracted from the AC contents and the result is loaded to the AC.	CF
	SBC*	Subtract M(DP) from AC with CF	1 0 0 0 1 0 0 1	1	1	AC, M(DP) ← (AC)+$\overline{[M(DP)]}$ +(CF)	The memory M(DP), CF contents are binary-subtracted from the AC contents and the result is loaded to the AC and M(DP).	CF
	ADD	Add M(DP) to AC	1 0 0 0 0 0 1 0	1	1	AC ← (AC)+[M(DP)]	The AC, memory [M(DP)] contents are binary-added and the result is loaded to the AC.	CF
	ADD*	Add M(DP) to AC	1 0 0 0 1 0 1 0	1	1	AC, M(DP) ← (AC)+[M(DP)]	The AC, memory [M(DP)] contents are binary-added and the result is loaded to the AC and M(DP).	CF
	SUB	Subtract M(DP) from AC	1 0 0 0 0 0 1 1	1	1	AC ← AC+$\overline{[M(DP)]}$ +1	The memory M(DP) contents are binary-subtracted from the AC contents and the result is loaded to the AC.	CF
	SUB*	Subtract M(DP) from AC	1 0 0 0 1 0 1 1	1	1	AC, M(DP) ← (AC)+$\overline{[M(DP)]}$ +1	The memory M(DP) contents are binary-subtracted from the AC contents and the result is loaded to the AC and M(DP).	CF
	ADN	Add M(DP) to AC	1 0 0 0 0 1 0 0	1	1	AC ← (AC)+[M(DP)]	The AC, memory [M(DP)] contents are binary-added and the result is loaded to the AC.	
	ADN*	Add M(DP) to AC	1 0 0 0 1 1 0 0	1	1	AC, M(DP) ← (AC)+[M(DP)]	The AC, memory [M(DP)] contents are binary-added and the result is loaded to the AC and M(DP).	
	AND	AND M(DP) to AC	1 0 0 0 0 1 0 1	1	1	AC ← (AC)∧[M(DP)]	The AC contents and memory [M(DP)] contents are ANDed and the result is loaded to the AC.	
	AND*	AND M(DP) to AC	1 0 0 0 1 1 0 1	1	1	AC, M(DP) ← (AC)∧[M(DP)]	The AC contents and memory [M(DP)] contents are ANDed and the result is loaded to the AC and M(DP).	
	EOR	Exclusive OR M(DP) to AC	1 0 0 0 0 1 1 0	1	1	AC ← (AC)∀[M(DP)]	The AC contents and memory [M(DP)] contents are exclusive-ORed and the result is loaded to the AC.	
	EOR*	Exclusive OR M(DP) to AC	1 0 0 0 1 1 1 0	1	1	AC, M(DP) ← (AC)∀[M(DP)]	The AC contents and memory [M(DP)] contentes are exclusive-ORed and the result is loaded to the AC and M(DP).	

Instruction	Mnemonic		Instruction code D7 D6 D5 D4 D3 D2 D1 D0	Bytes	Cycles	Function	Description	Status flag to be affected
Operation instructions	OR	OR M(DR) to AC	1 0 0 0 0 1 1 1	1	1	AC ← (AC)∨[M(DP)]	The AC contents and memory [M(DP)] contents are ORed and the result is loaded to the AC.	
	OR*	OR M(DR) to AC	1 0 0 0 1 1 1 1	1	1	AC, M(DP) ← (AC)∨[M(DP)]	The AC contents and memory [M(DP)] contents are ORed and the result is loaded to the AC and M(DP).	
	ADCI X	Add Immediate data to ACC with CF	1 0 0 1 0 0 0 0 – – – – X3 X2 X1 X0	2	2	AC ← (AC)+X+(CF)	The AC, CF contents and Immediate data X are binary-added and the result is loaded to the AC.	CF
	SBCI X	Subtract Immediate data from AC with CF	1 0 0 1 0 0 0 1 – – – – X3 X2 X1 X0	2	2	AC ← (AC)+$\overline{X}$+(CF)	Immediate data X is binary-subtracted from the AC contents and the result is loaded to the AC.	CF
	ADDI X	Add Immediate data to AC	1 0 0 1 0 0 1 0 – – – – X3 X2 X1 X0	2	2	AC ← (AC)+X	The AC contents and Immediate data X are binary-added and the result is loaded to the AC.	CF
	SUBI X	Subtract Immediate data from AC	1 0 0 1 0 0 1 1 – – – – X3 X2 X1 X0	2	2	AC ← (AC)+$\overline{X}$+1	Immediate data X is binary-subtracted from the AC contents and the result is loaded to the AC.	CF
	ADNI X	Add Immediate data to AC	1 0 0 1 0 1 0 0 – – – – X3 X2 X1 X0	2	2	AC ← (AC)+X	The AC contents and Immediate data X are binary-added and the result is loaded to the AC.	
	ANDI X	ANDImmediate data to AC	1 0 0 1 0 1 0 1 – – – – X3 X2 X1 X0	2	2	AC ← (AC)∧X	The AC contents and Immediate data X are ANDed and the result is loaded to the AC.	
	EORI X	Exclusive OR Immediate data to AC	1 0 0 1 0 1 1 0 – – – – X3 X2 X1 X0	2	2	AC ← (AC)∀X	The AC contents and Immediate data X are exclusive-ORed and the result is loaded to the AC.	
	ORI X	OR Immediate data to AC	1 0 0 1 0 1 1 1 – – – – X3 X2 X1 X0	2	2	AC ← (AC)∨X	The AC contents and Immediate data X are ORed and the result is loaded to the AC.	
Data pointer manipulation instructions	SDPL	Store AC to DP_L	0 0 0 1 1 1 0 0	1	1	DP_L ← (AC)	The AC contents are loaded to the DP_L.	
	SDPH	Store AC to DP_H	0 0 0 1 1 1 0 1	1	1	DP_H ← (AC)	The AC contents are loaded to the DP_H.	
	EDPL	Exchange DP_L with EDP_L	0 0 0 1 1 1 1 0	1	1	$(DP_L)\rightleftarrows(EDP_L)$	The DP_L contents and EDP_L contents are exchanged.	
	EDPH	Exhange DP_H with EDP_H	0 0 0 1 1 1 1 1	1	1	$(DP_H)\rightleftarrows(EDP_H)$	The DP_H contents and EDP_H contents are exchanged.	
	IDPL	Increment DP_L	1 0 0 1 1 0 1 0	1	1	DP_L ← (DP_L)+1	The DP_L contents are incremented +1.	
	DDPL	Decrement DP_L	1 0 0 1 1 0 1 1	1	1	DP_L ← (DP_L)−1	The DP_L contents are decremented −1.	
	IDPH	Increment DP_H	1 0 0 1 1 1 0 0	1	1	DP_H ← (DP_H)+1	The DP_H contents are incremented +1.	
	DDPH	Decrement DPH	1 0 0 1 1 1 0 1	1	1	DP_H ← (DP_H)−1	The DP_H contents are decremented −1.	
	LDPL	Load AC from DP_L	1 1 1 1 1 1 0 1	1	1	AC ← (DP_L)	The DP_L contents are loaded to the AC.	
	LDPH	Load AC from DP_H	1 1 1 1 1 1 1 0	1	1	AC ← (DP_H)	The DP_H contentes are loaded to the AC.	
	MDPL X	Move Immediate data to DP_L	1 0 1 1 X3 X2 X1 X0	1	1	DP_L ← X	Immediate data X is loaded to the DP_L.	
	MDPH X L	Move Immediate Data to DP_H	1 1 0 0 X3 X2 X1 X0	1	1	DP_H ← X	Immediate data X is loaded to the DP_H.	
Flag manipulation instructions	LHLT	Load Halt Release Flag	1 0 1 0 1 0 1 1	1	1	AC ← (STS2) STS2 ← 0	The STS2 contents are transferred to the AC and then the STS2 is reset.	SCF1-4
	L500	Load AC from STS1	1 0 1 0 1 1 0 0	1	1	AC ← (STS1) SCF0 ← 0	The STS1 contents are transferred to the AC and then the SCF0 is reset.	SCF0
	CSP	Chrono Stop	0 0 0 0 0 1 0 0	1	1	CSTF ← 0	The CSTF is reset.	CSTF
	CST	Chrono Start	0 0 0 0 0 1 0 1	1	1	CSTF ← 1	The CSTF is set.	CSTF
	RC5	Reset HEF0	0 0 0 0 0 1 1 0	1	1	HEF0 ← 0	The HEF0 is reset so that the halt mode release by an overflow from the predivider is inhibited.	HEF0

Instruction	Mnemonic		Instruction code D7 D6 D5 D4 D3 D2 D1 D0	Bytes	Cycles	Function	Description	Status flag to be affected
Prohibition instruction	SC5	Set HEF0	0 0 0 0 0 1 1 1	1	1	HEF0 ← 1	The HEF0 is set so that an overflow signal from the predivider releases the halt mode.	HEF0
Stack pointer manipulation instructions	ISP	Increment SP	1 0 0 1 1 1 1 0	1	1	SP ← (SP)+1	The SP contents are incremented +1.	
	DSP	Decrement SP	1 0 0 1 1 1 1 1	1	1	SP ← (SP)−1	The SP contents are decremented −1.	
	LSP	Load AC from SP	1 0 1 0 1 0 1 0	1	1	AC ← (SP)	The SP contents are loaded to the AC.	
	SSP	Store AC to SP	1 0 1 0 1 1 1 0	1	1	SP ← (AC)	The AC contents are loaded to the SP.	
	MSP X	Move Immediate data to SP	1 1 1 0 X3 X2 X1 X0	1	1	SP ← X	Immediate data X is loaded to the SP.	
Load/store instructions	LDA	Load AC from [M(DP)]	1 0 1 0 1 0 0 1	1	1	AC ← [M(DP)]	The memory [M(DP)] contents are loaded to the AC.	
	STA	Store AC to [M(DP)]	1 0 1 0 1 1 0 1	1	1	M(DP) ← (AC)	The AC contents are loaded to the memory M(DP).	
	MVI X	Move Immediate data to M(DP)	0 0 1 0 X3 X2 X1 X0	1	1	M(DP) ← X	Immediate data X is loaded to the memory M(DP).	
	LDI X	Load AC with Immediate data	0 0 1 1 X3 X2 X1 X0	1	1	AC ← X	Immediate data X is loaded to the AC.	
CPU control instructions	HALT	HALT	0 0 0 0 0 0 0 0	1	1	The operation of CPU is stopped. The following condition causes the halt mode to be released. ● The halt release condition specified by the SIC and SC5 instruction is met.		
	SIC X	Set/Reset HALT Release Enable Flag	1 1 0 1 X3 X2 X1 X0	1	1	X0 – X3: Operation X0=1: The HEF1 is set so that the signal from the predivider releases the halt mode. X1=1: The HEF2 is set so that the rising of signal at input port S releases the halt mode. X2=1: The HEF3 is set so that the rising of signal at input port M releases the halt mode. X3=1: The HEF4 is set so that the 1/10-second pulse releases the halt mode.		HEF1 to 4
	NOP	No Operation	1 1 1 1 1 1 1 1	1	1			
	RBAK	Reset Back-up Mode	1 1 1 1 1 0 0 0	1	1	BCF ← 0	The backup mode is released.	
	SBAK	Set Back-up Mode	1 1 1 1 1 0 0 1	1	1	BCF ← 1	When powered from Li battery, VSS2 is applied to the logic unit. When powered from Ag. Li battery, EXT-V, the OSC circuit is doubled in inverter size.	
Input/output instructions	IPS	Input Port-S to AC	1 0 1 0 1 1 1 1	1	1	AC ← [P(S)]	The input data at input port S is loaded to the AC.	
	IPM	Input Port-M to AC	1 0 1 0 1 0 0 0	1	1	AC ← [P(M)]	The input data at input port M is loaded to the AC.	
	RLGT	Reset Light	1 1 1 1 0 0 1 0	1	1	LIGHT ← 0	The light output is set to "L" level.	
	SLGT	Set Light	1 1 1 1 0 0 1 1	1	1	LIGHT ← 1	The light output is set to "H" level.	
	SAS X	Set Alarm Sound	1 1 1 1 1 0 1 0 X7 X6 X5 X4 X3 X2 X1 X0	2	2	Waveforms specified by X7 to X0 are delivered at the ALM1, ALM2. X7 – X0: Control contents; X7 X6: Alarm tone/melody select signal; X5 X4: Octave Control; X3 X2 X1 X0: Musical Scal Control		

Alarm OFF at X3 to X0 = 1

Instruction	Mnemonic		Instruction code D7 D6 D5 D4 D3 D2 D1 D0	Bytes	Cycles	Function	Description	Status flag to be affected
Input/output instructions	RAS	Reset Alarm Sound	1 1 1 1 1 0 1 0 1 1 1 1 1 1 1 1	2	2	=SAS FF	The ALM1, 2 outputs are set to "L" level	
	SPDR X	Set/Reset PDF-Registor	1 1 1 1 0 1 X1 X0	1	1	PDF ← X	The pull-down MOS Tr at the corresponding input port is turned ON/OFF.	PDF
						Bit contents	Operation	
						X0=0	S-Terminal Pull down Tr OFF	
						X0=1	S-Terminal Pull down Tr ON	
						X1=0	M-Terminal Pull down Tr OFF	
						X1=1	M-Terminal Pull down Tr ON	
	OUT	Write AC & M(DP) to LCD Latch L(SP) (SP=#0 to C)	1 1 1 1 1 1 0 0	1	1		The AC, memory [M(DP)] contents are loaded to the LCD latch L(SP) directly addressed by the SP.	
		SP=#D Move AC to CTL3				CTL3←(AC)	The AC contents are loaded to the CTL3.	
		SP=#E Write AC to P(P00-03)				P(P0)←(AC)	The AC contents are loaded to the port P0.	
		SP=#F Write AC to P(P10-13)				P(P1)←(AC)	The AC contents are loaded to the port P1.	
	IN	SP=#D Load AC from STS3				AC←(STS3)	The STS3 content is loaded to the AC.	
		SP=#E Input Port-P0 to AC				AC←[P(P0)]	The input data at port P0 is loaded to the AC.	
		SP=#F Input Port-P1 to AC				AC←[P(P1)]	The input data at port P1 is loaded to the AC.	
	TWRT	Read Table data from program ROM & Write Table data to LCD Latch (SP) (SP=#0 to C)	0 0 0 0 0 0 1 0	1	2	The data of ROM, on current page, addressed by the AC, M(DP) contents is loaded to the LCD latch L(SP) addressed by the SP.		
		SP=#D Read Table data from Program ROM & Write Table data to CTL3				The contents of the ROM on current page addressed by the PC whose low-order 8 bits are replaced with the contents of the AC and M(DP) are loaded to the CTL3.		
		SP=#E Read Table data from Program ROM & Write Table data to P (P00 to 03)				The contents of the ROM on current page addressed by the PC whose low-order 8 bits are replaced with the contents of the AC and M(DP) are loaded to the port P0.		
		SP=#F Read Table data from Program ROM & Write Table data to P (P10 to 13)				The contents of the ROM on current page addressed by the PC whose low-order 8 bits are replaced with the contents of the AC and M(DP) are loaded to the port P1.		
	TMEL	Set Table data to Alarm Sound data	0 0 0 0 0 0 1 1	1	2	The data of ROM, on current page, addressed by the AC, M(DP) contents is set to alarm sound data and waveforms specified by the table data are delivered at ALM1, 2. (Same as SAS instruction)		
Jump instructions	JMP X	Jump	0 0 0 0 1 X10 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0	2	2	PC10–PC0←X10–X0	The data specified by X10 to X0 is loaded to the PC to cause an unconditional jump.	
	BAB0 X	Branch on AC bit 0 High	0 1 0 0 1 X10 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0	2	2	PC10–PC0←X10–X0 if AC0=[1]	If bit 0 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BAB1 X	Branch on AC bit 1 High	0 1 0 1 1 X10 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0	2	2	PC10–PC0←X10–X0 if AC1=[1]	If bit 1 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BAB2 X	Branch on AC bit 2 High	0 1 1 0 1 X10 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0	2	2	PC10–PC0←X10–X0 if AC2=[1]	If bit 2 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BAB3 X	Branch on AC bit 3 High	0 1 1 1 1 X10 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0	2	2	PC10–PC0←X10–X0 if AC3=[1]	If bit 3 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BANZ X	Branch on AC not Zero	0 1 0 1 0 X10 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0	2	2	PC10–PC0←X10–X0 if AC≠0	If the AC is not "0", a jump occurs. If "0", the PC is incremented +1.	
	BAZ X	Branch on AC zero	0 1 0 0 0 X10 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0	2	2	PC10–PC0←X10–X0 if AC=0	If the AC is "0", a jump occurs. If not "0", the PC is incremented +1.	
	BCNH X	Branch on CF not High	0 1 1 0 0 X10 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0	2	2	PC10–PC0←X10–X0 if CF≠1	If the CF is "0", a jump occurs. If "1", the PC is incremented +1.	
	BCH X	Branch on CF High	0 1 1 1 0 X10 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0	2	2	PC10–PC0←X10–X0 if CF=1	If the CF is "1", a jump occurs. If "0", the PC is incremented +1.	

Instruction	Mnemonic		Instruction code D7 D6 D5 D4 D3 D2 D1 D0	Bytes	Cycles	Function	Description	Status flag to be affected
Jump instructions	PAGE	Page Set	0 0 0 1 0 0 0 1	1	1	PAGE ← [M(DP)]	The memory [M(DP)] contents are loaded to the PAGE latch.	
	JMP*	Jump to the Address modified by PAGE AC and M(DP)	0 0 0 1 0 0 0 0	1	1	PC_{10}–PC_8←(PAGE) PC_7–PC_4←(AC) PC_3–PC_0←[M(DP)]	An unconditional jump occurs to a page specified by the PAGE and an address low-order 8 bits of the PC which are loaded with the AC and memory M(DP) contents.	
Subroutine instructions	JSR X	Jump Subroutine	1 0 1 0 0 X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	2	2	STACK ← PC+2 PC_{10}–PC_0←X_{10}–X_0	A subroutine is called.	
	RTS	Return from Subroutine	0 0 0 1 0 0 1 1	1	1	PC ← (STACK)	A return from a subroutine occurs.	
Other instructions	MPCL	Move PC_0 – PC_3 to M(DP)	0 0 0 1 0 1 0 0	1	1	M(DP)–PC_3–PC_0	The contents of the low-order 4 bits of the PC are stored in the memory M(DP).	
	MPCM	Move PC_4 – PC_7 to M(DP)	0 0 0 1 0 1 0 1	1	1	M(DP)–PC_7–PC_4	The contents of the medium-order 4 bits of the PC are stored in the memory M(DP).	
	MPCH	Move PC_8 – PC_{10} to M(DP)	0 0 0 1 0 1 1 0	1	1	M(DP)–PC_{10}–PC_8	The contents of the high-order 3 bits of the PC are stored in the memory M(DP).	
	CSEC	Clear SEC Counter	1 1 1 1 1 0 1 1	1	1		The high-order 5 bits of the predivider are reset and the SCF0, SCF1, SCF4 are reset.	SCF0 SCF1 SCF4

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